300mm Large Scale eWLB(embedded Wafer Level BGA) : Cost Effective Solution with Performance

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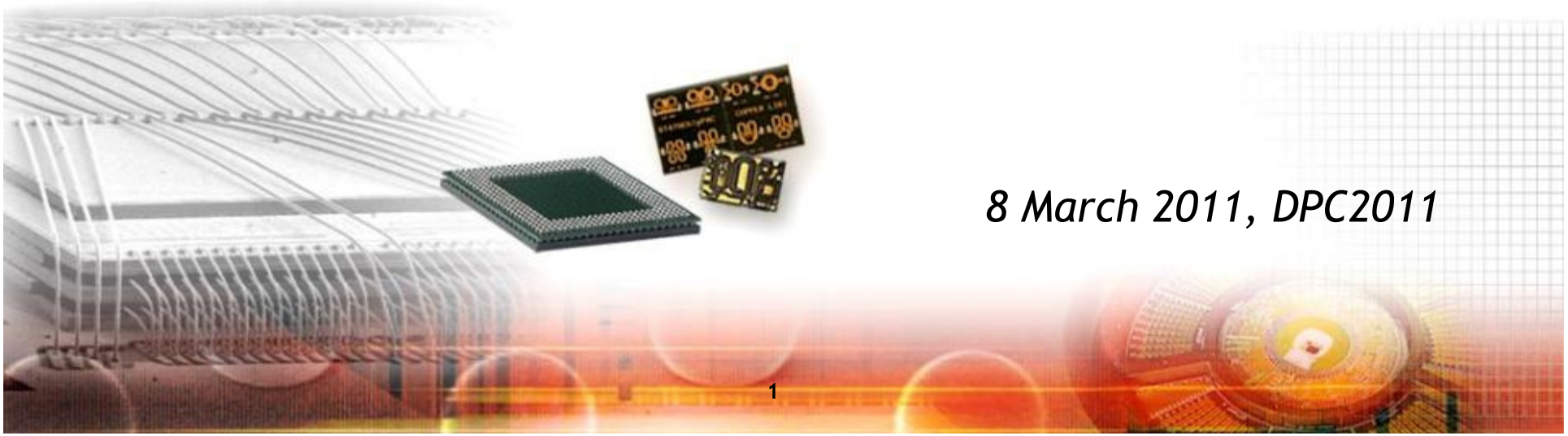
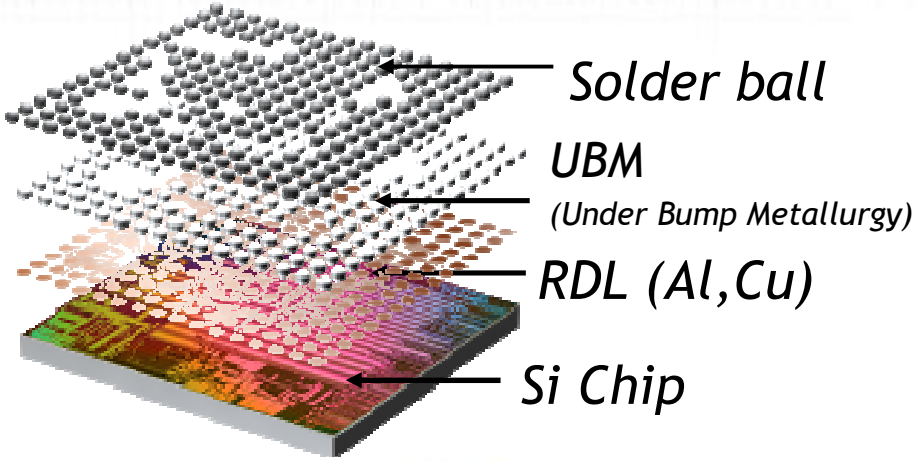


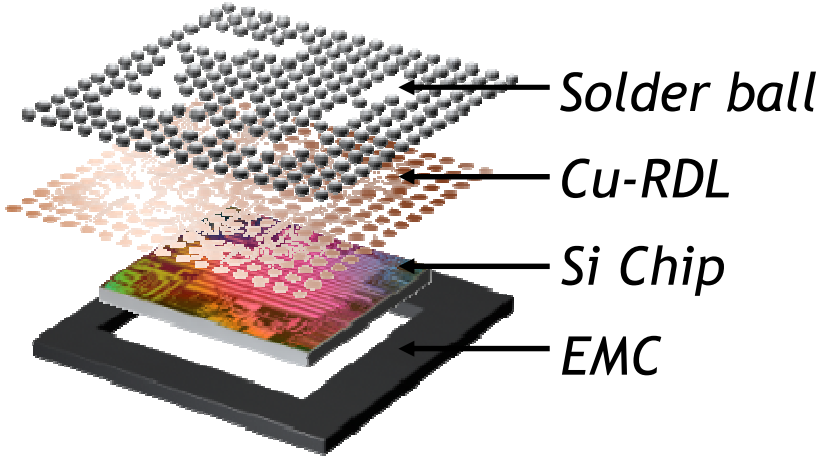
8 March 2011, DPC2011

Contents

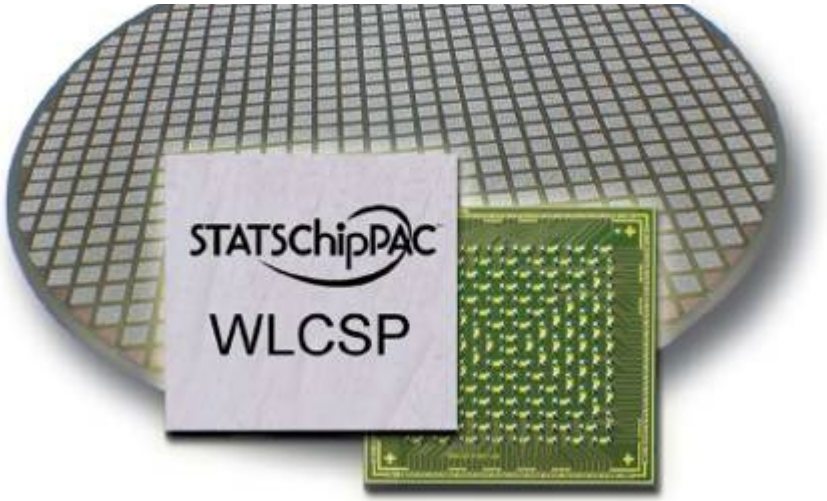
1. eWLB Configuration

- Comparison between fan-in vs fan-out WLP
- eWLB extends the application space of wafer level packages

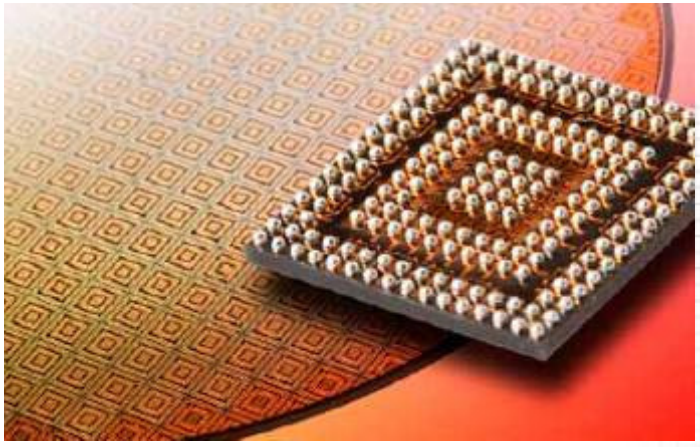




Conventional WLP (fan-in)

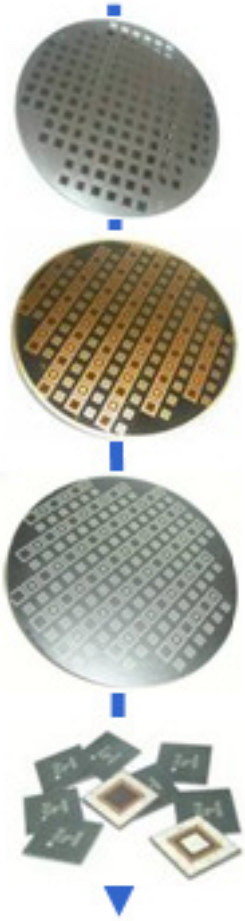


eWLB (fan-out) – footprint larger than die



2. eWLB Process Flow

eWLB – Process Flow



1) Reconstitution of dies to „artificial" wafer
- ⇨ Single die or several (different) dies, actives and passives
- ⇨ Usage of FE-tested-good-dies (yield)
- ⇨ Materials well-known in BE technology
- ⇨ Molded artificial wafer is starting point for thin film technology

FRONT-END

2) Redistribution
- ⇨ Using thin-film-technologies
- ⇨ Using standard thin-film equipment
- ⇨ Using commercially available materials

RDL

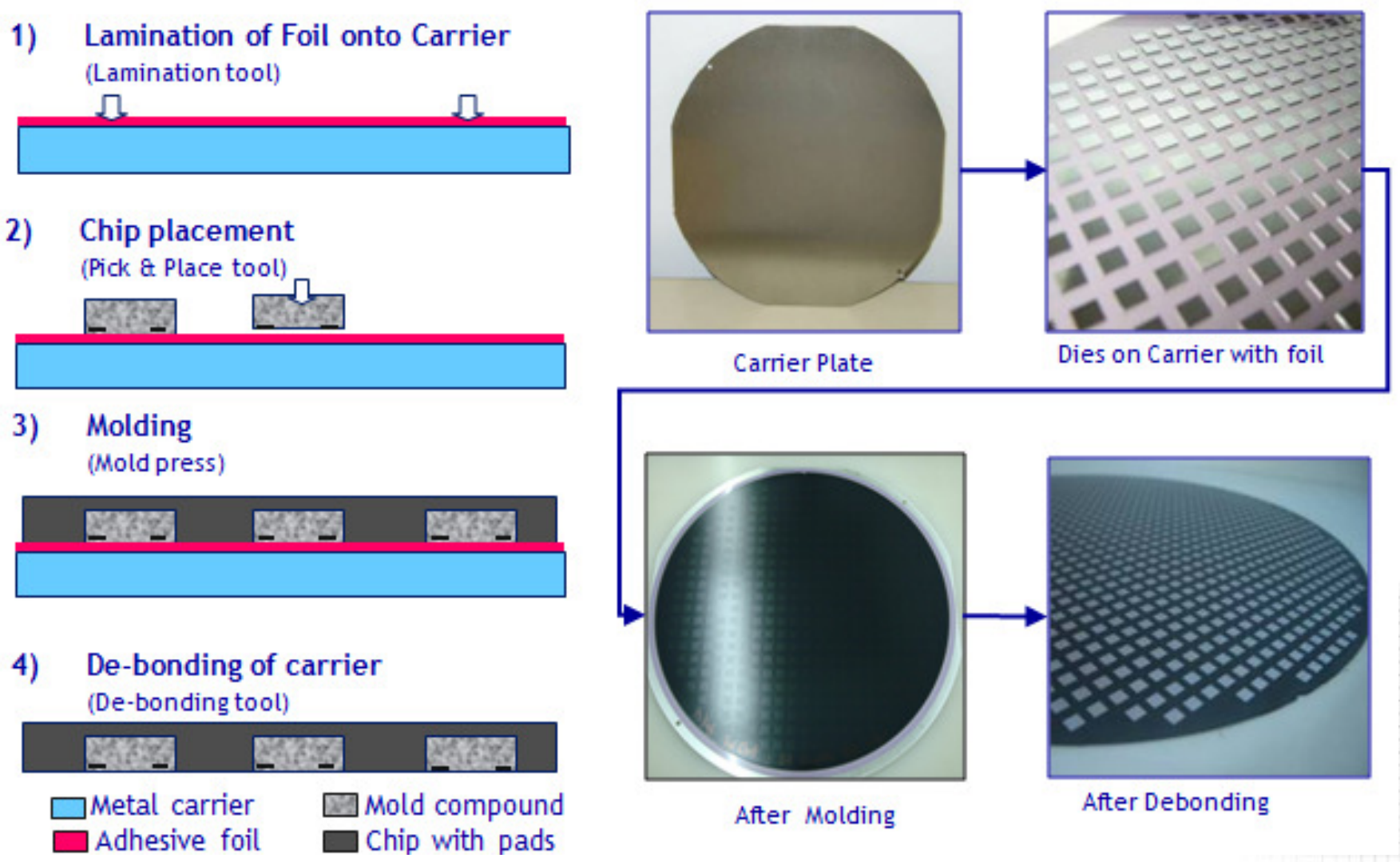
3) Ball Apply and Singulation
- ⇨ Standard backend assembly flow (and equipment)

4) Test, Mark, Scan, Pack
- ⇨ Standard or wafer level based test flow
- ⇨ Standard assembly

BACK-END

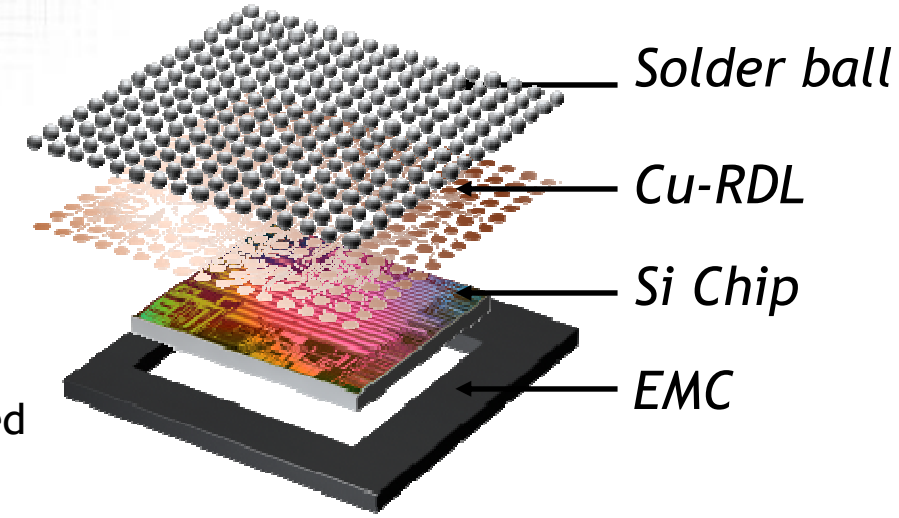
eWLB Schematic

eWLB Reconstitution Process



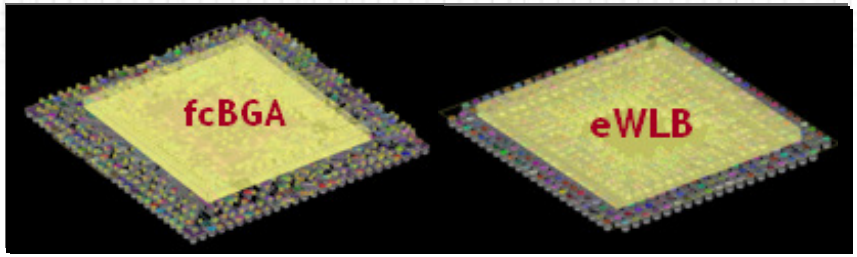
3. eWLB Value Proposition

- eWLB expands the WLP application space and provides the smallest and thinnest package option
- Excellent electrical and thermal performance
  - Great for high frequency application
  - Excellent for RF and mixed signal due to low parasitics compared to laminate-based packages
  - The lowest thermal resistance
  - High density routing is easily implemented in RDL
- No ELK damage issues for advanced Si node devices
- Proven low cost path using a batch process & simple supply chain
- Path to the flexible 3D packages – any array patterns on the top
- Scalable technology to larger panel production – Lower cost



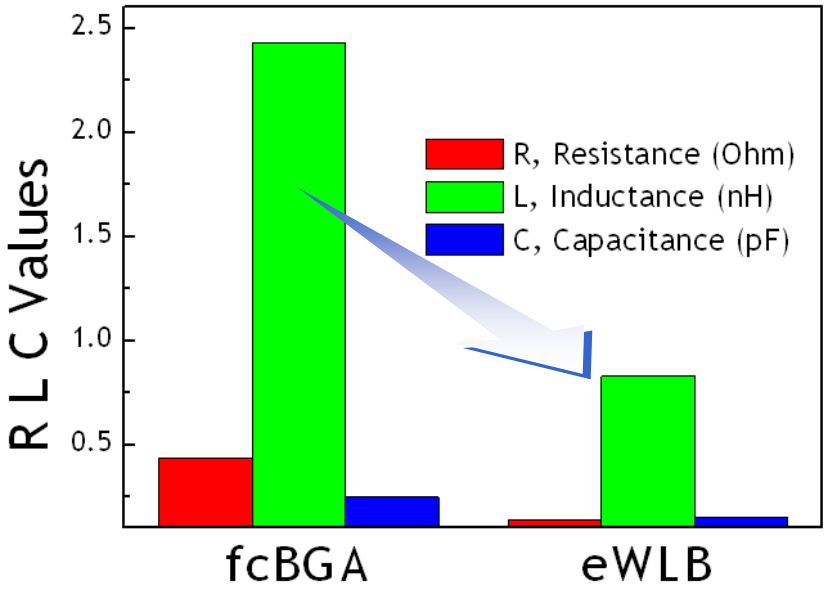
4. Performance Advantages of eWLB

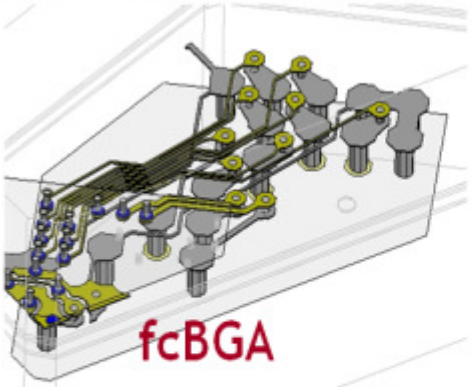
High Performance Electrical Solution



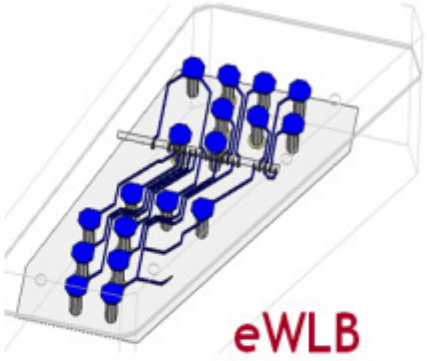
	FcBGA	eWLB
PKG size (mm2)	11x11	10x9
Die Size (mm2)	7.5x7.0	7.5x7.0
Substrate Thickness/Layer	0.18mm / 2-layer	1-layer RDL
Ball Count	477 I/O	508 I/O
Ball Pitch	0.50 mm	0.40 mm

Electrical Characterization





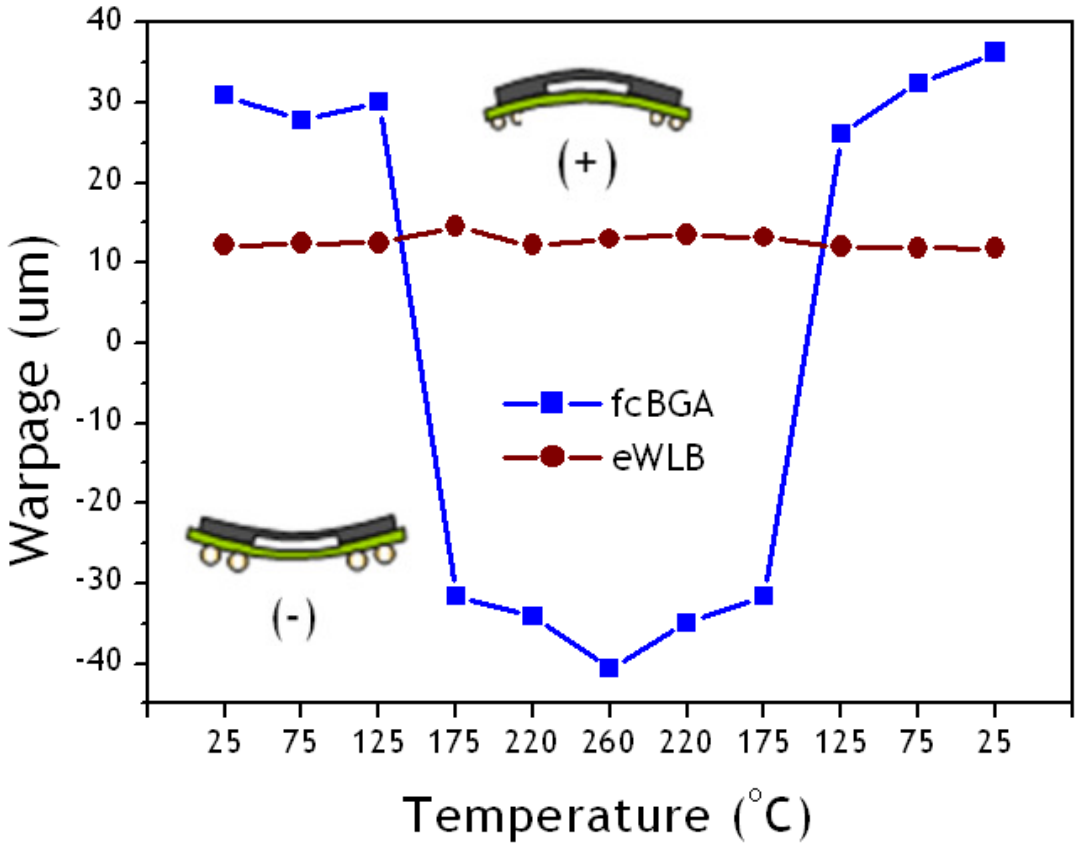
Solder bump + substrate metal line + substrate via + Solder ball

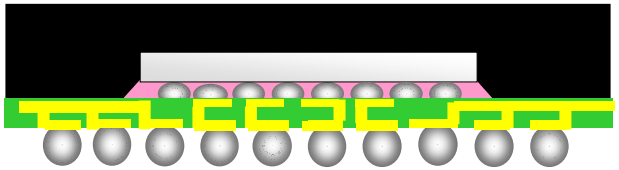


RDL metal line + Solder ball

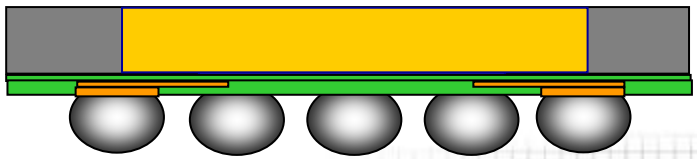
eWLB shows less values of RLC electrical parasitic compared to fcBGA, due to short/removed interconnection .

High Temperature Warpage Behavior Supports Improved Board Assembly Yield





fcVFBGA,7x7mm, 191LD NSP
PKG height 0.95 mm
Die 4.46 x 5.65 x 0.19 mm

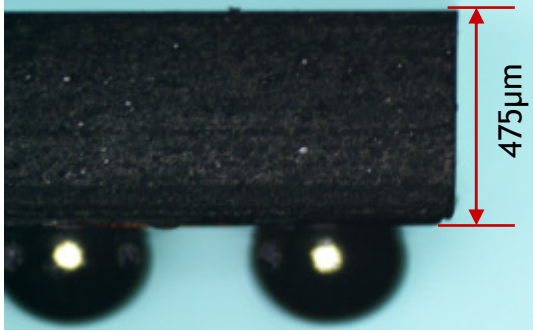


eWLB 8x8mm, 182I/O
PKG height 0.7 mm
Die 5 x 5 x 0.45 mm

Thin eWLB Solution Enables Further Improvement

- Easily achieved by conventional back-grinding process
- No backside chipping, crack issue because it is molded, plastic wafer
- Improved Form Factor for thin applications
- Improved Board Level Reliability due to mechanical flexibility

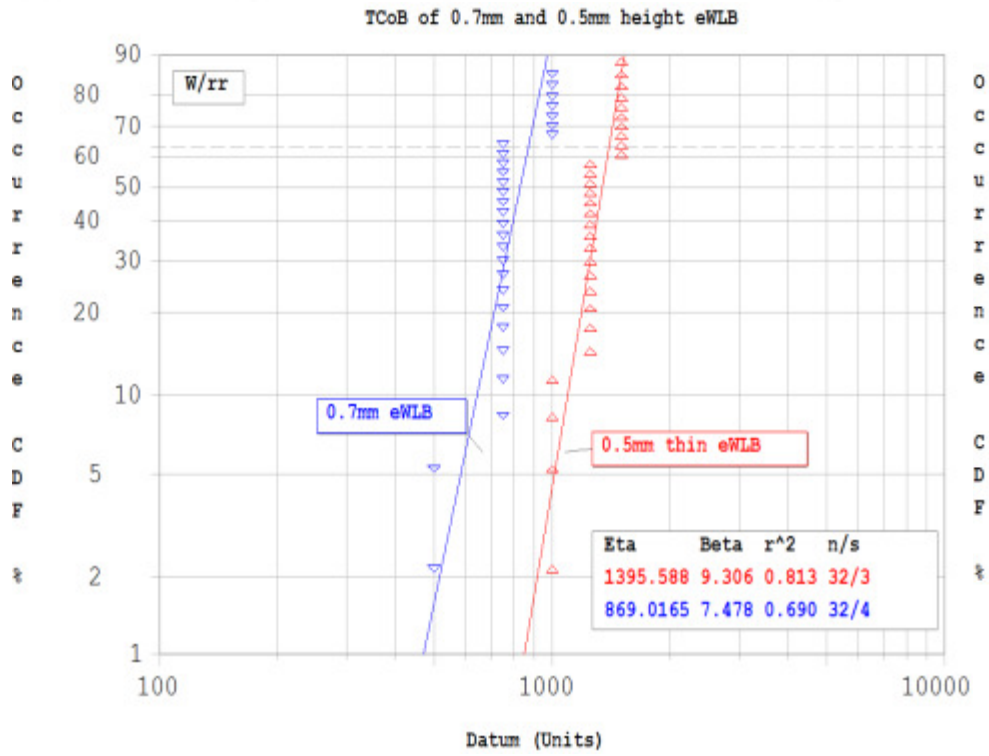
Standard eWLB - 475um body thickness



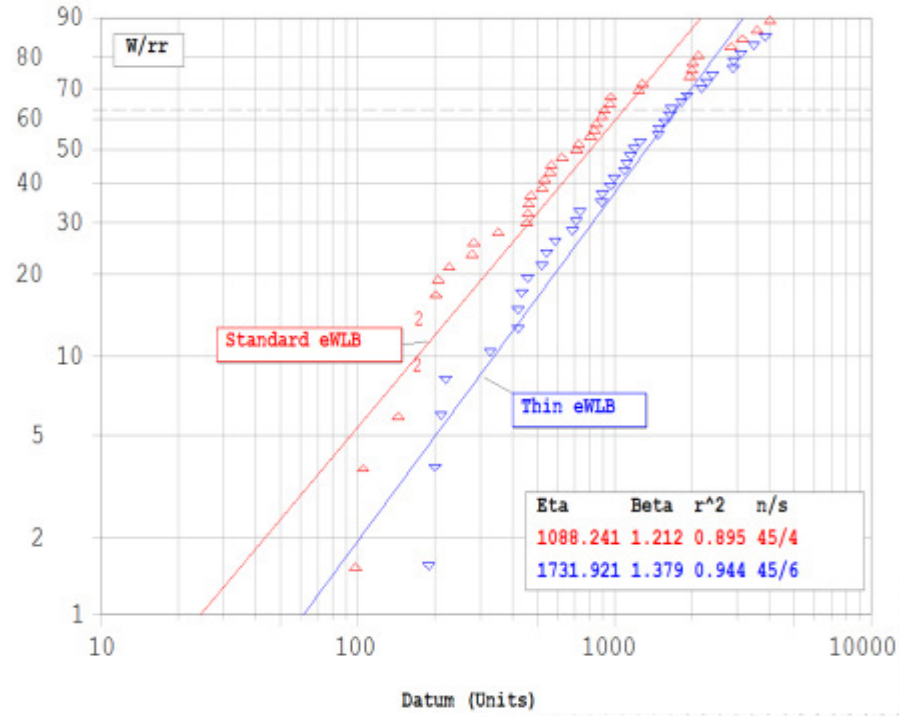
Thin eWLB - 250um body thickness

Improved Board Level Reliability with Thin eWLB

TCoB



Drop Test

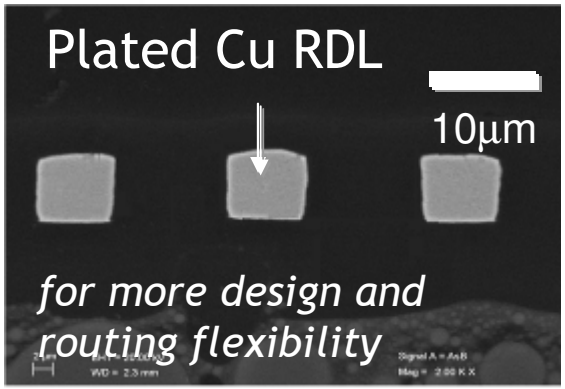


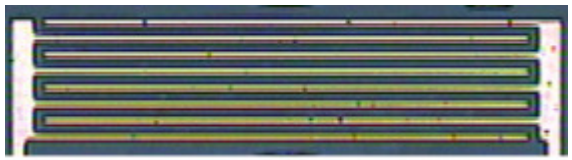
50~80% TCoB Reliability performance improved

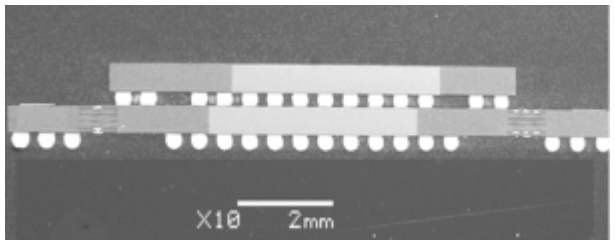
50~70% Drop Reliability performance improved

Next Generation eWLB

10µm/10µm line width and line spacing

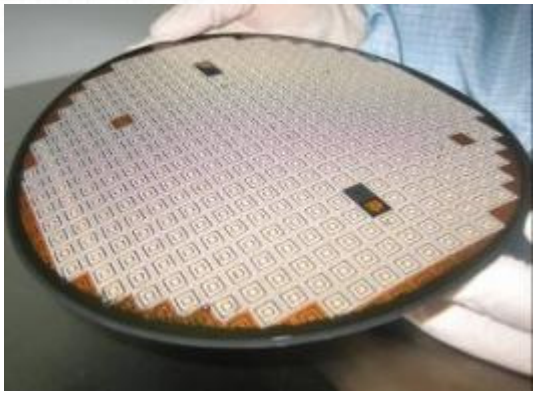


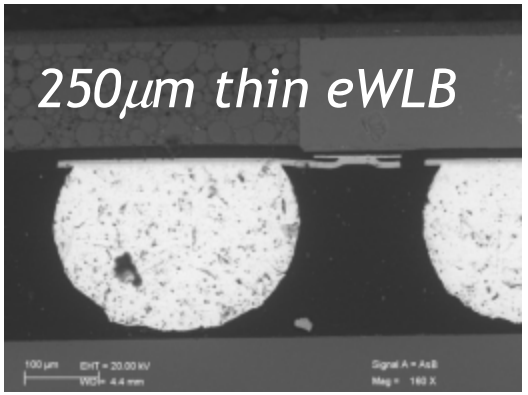


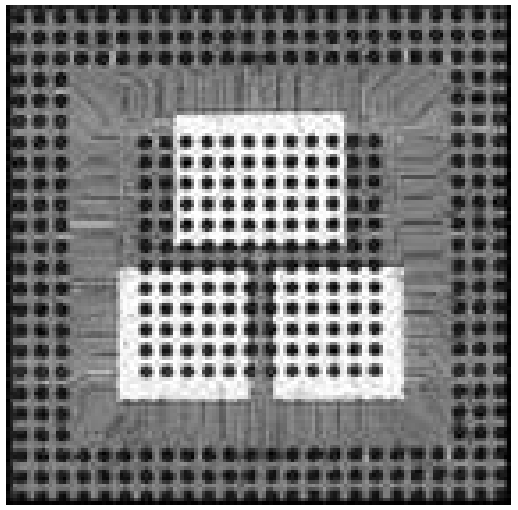


3D (double-side) eWLB

Thin packaging solution (<0.5mm)

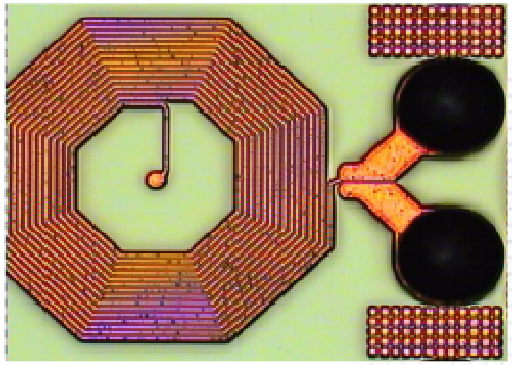






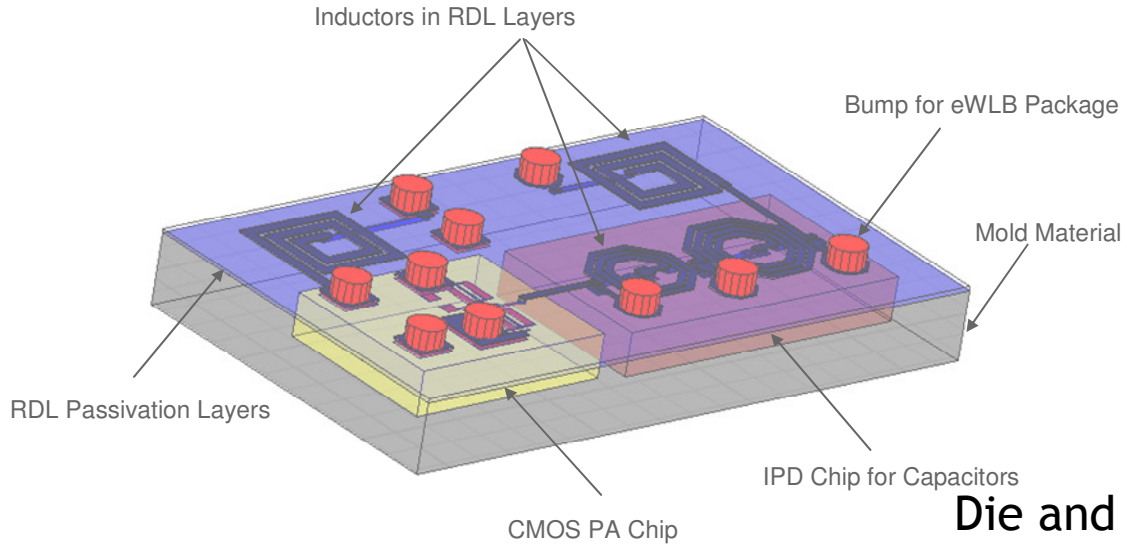
Multi-die eWLB

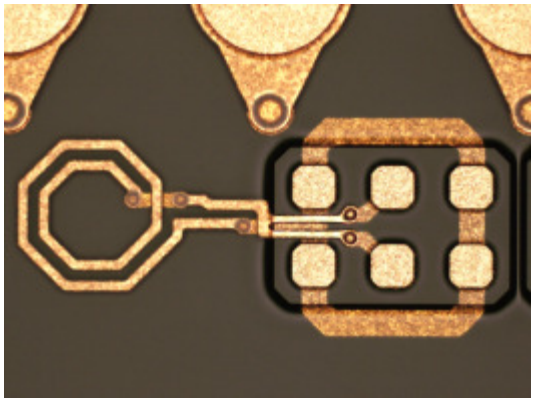
Embedded Passives



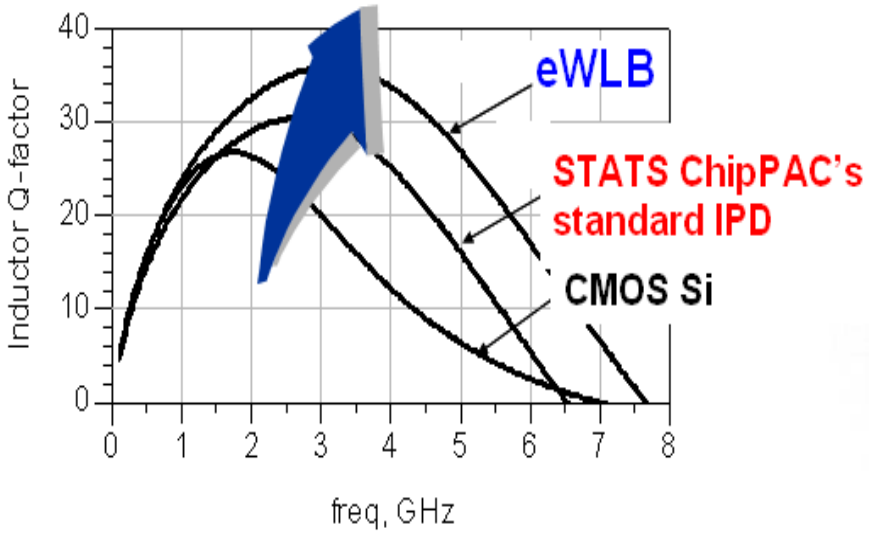
Courtesy of STATS ChipPAC - ST - Infineon 3D eWLB Alliance

High Q Inductor Solution for RF Applications



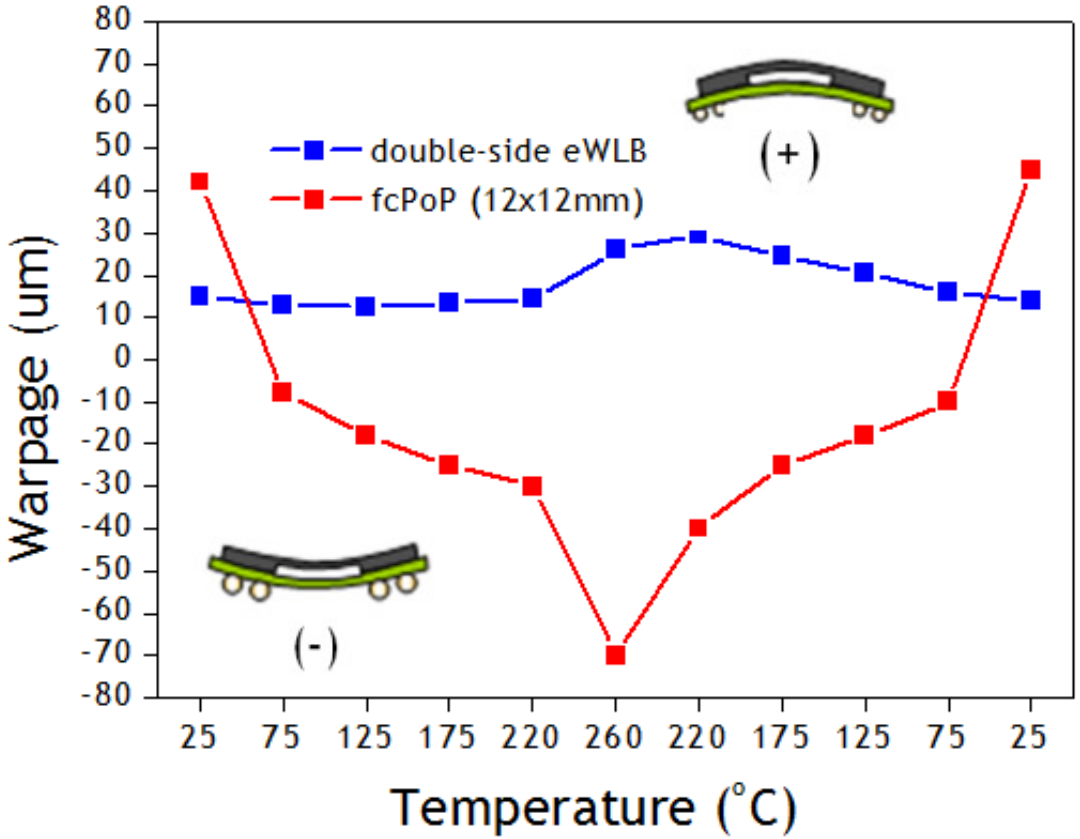


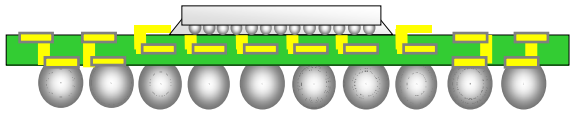
Die and a silicon IPD die embedded in mold substrate (eWLB)



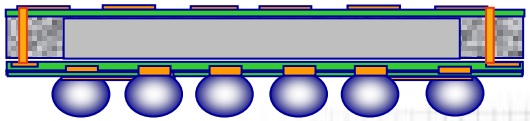
- Inductor on mold material (eWLB) has the best Q.
- Inductors can be made in RDL process, using eWLB mold compound as supporting substrate for best performance.
- High-integration and high-performance can be achieved through eWLB package.

Warpage Control for Double-side eWLB
- High Temperature Warpage Measurement



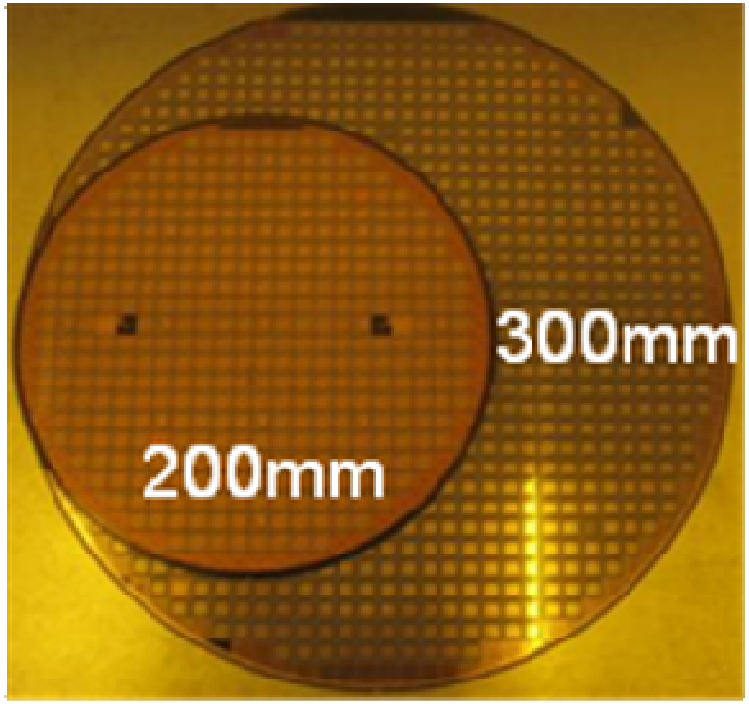


fcFBGA-PoP-b,12x12mm, 516I/O
Substrate thickness 0.43 mm
Die 8x8 mm



eWLB 12x12mm, 396I/O
PKG height 0.7 mm

5. 300mm Large Scale eWLB



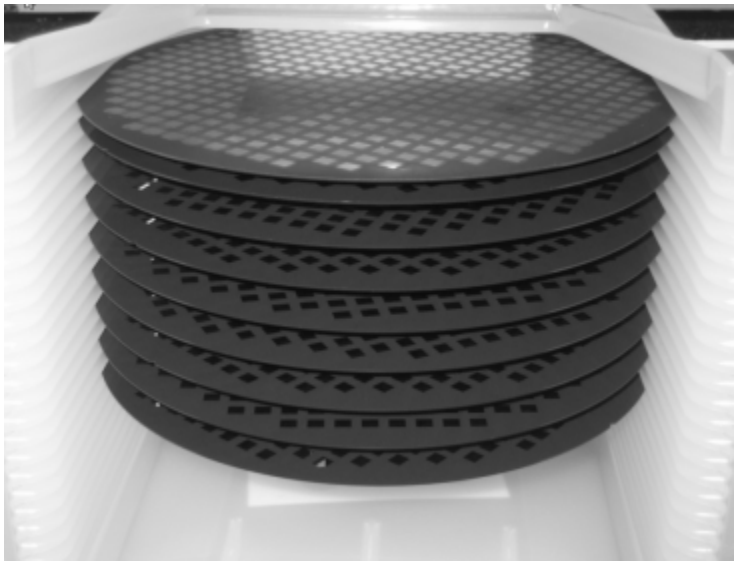
Wafer size difference between 200mm and 300mm eWLB wafers

Significant cost and productivity advantages can be achieved with the larger scale reconstituted wafer;

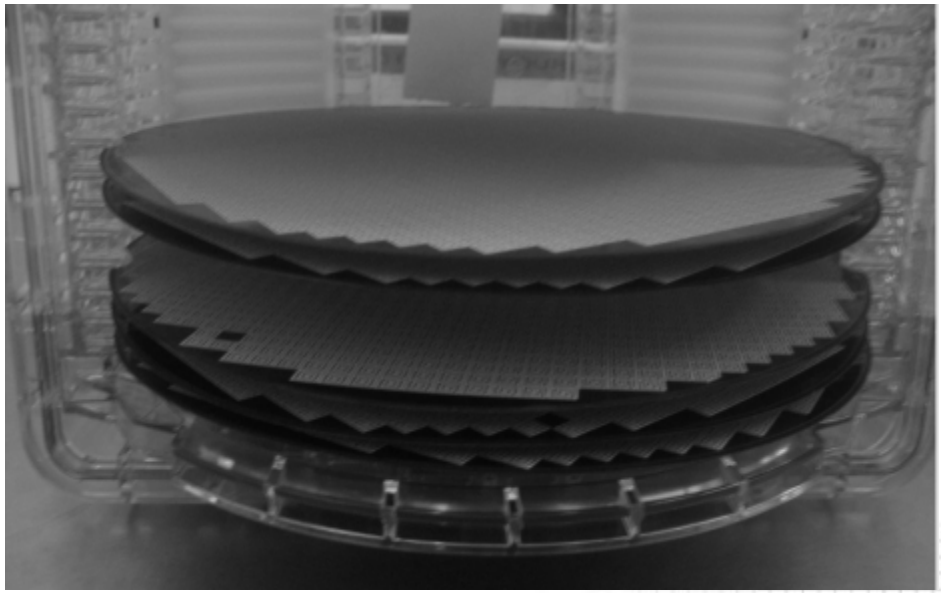
- *Economics of Scale*
- *Higher throughput*

eWLB Carrier Warpage Challenge

200mm



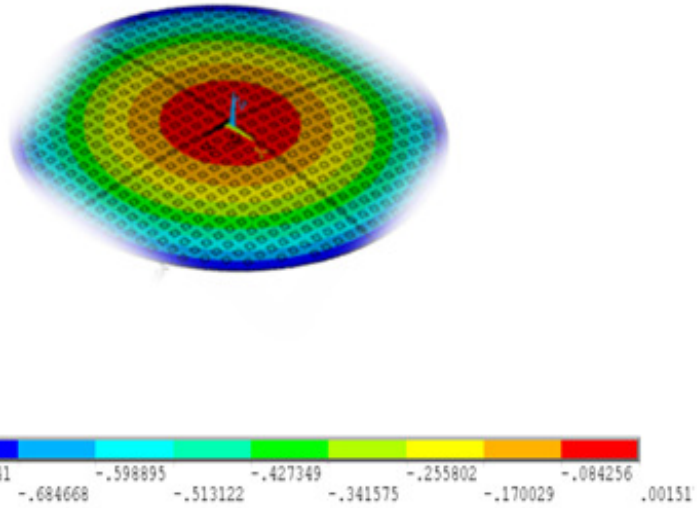
300mm



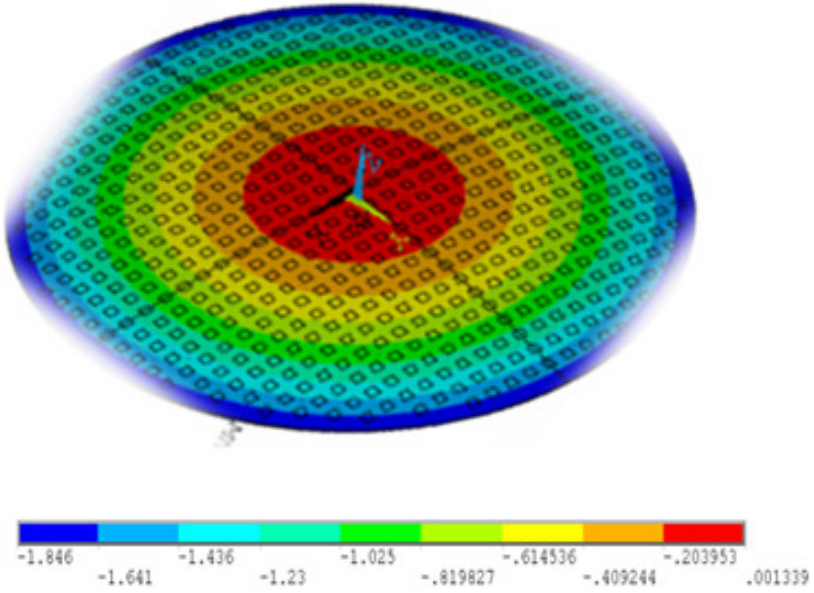
300mm eWLB carrier has more warpage than 200mm due to the wafer's large size (more than 2x) and higher mass.

eWLB Warpage Challenge

200mm



300mm



- Warpage affects wafer handling, process stability and yield, as well as wafer throughput and yield.
- It is important to optimize and control warpage behavior on larger carriers.
- This has been a critical factor in the transition to 300mm and will be an important factor in the transition to larger panels.

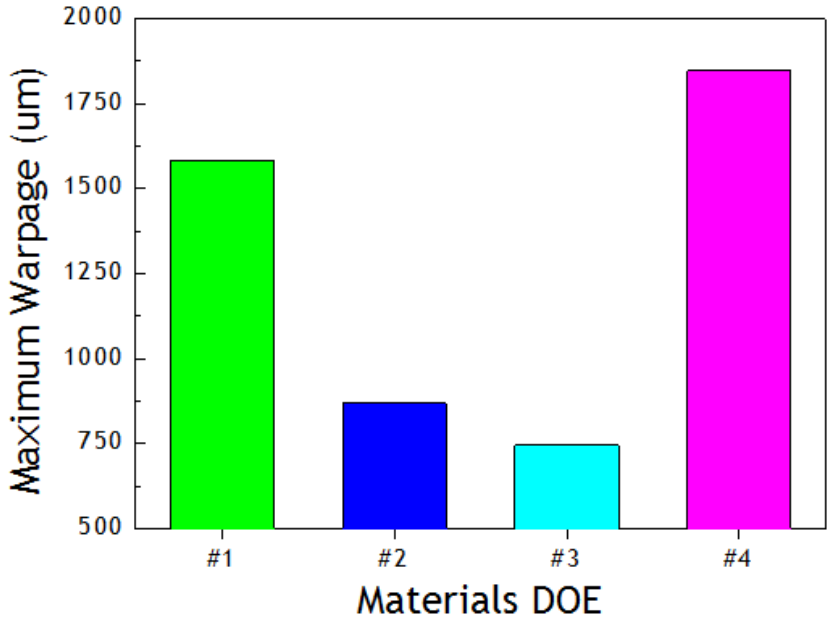
eWLB Warpage Optimization

To optimize warpage behavior, various material and process parameters were studied.

- CTE (coefficient of thermal expansion)
- Young's modulus
- Poison ratio

After basic thermal-mechanical simulation study with several DOE (Design of Experiment), key parameters were identified and investigated to optimize warpage.

- Dielectric materials
- Dielectric thickness
- Mold compound thickness



Computational mechanical warpage simulation data with different material DOE of 300mm eWLB.

300mm eWLB Process Characterization

Die Displacement of 200mm and 300mm eWLB

Die Displacement (12 points per wafer)	X-axis Mean (um)	Std Dev	Y-axis Mean (um)	Std Dev
12”	0	5.7	-0.9	5.6
8”	0.4	4.5	0.3	4.2

Cu plating thickness of 200mm and 300mm eWLB

Cu plating thickness (um)	Mean	Std Dev
12”	7.54	0.24
8”	7.50	0.23

300mm eWLB Process Characterization

Dielectric Thickness of 200mm and 300mm eWLB

Dielectrics thickness (um)	Mean	Std Dev
12”	7.60	0.08
8”	7.57	0.05

Ball shear strength of 200mm and 300mm eWLB

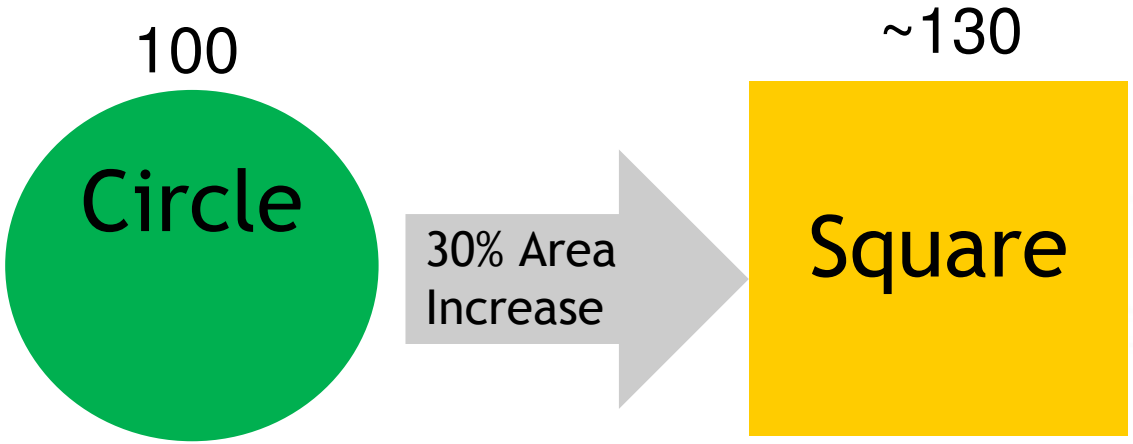
Ball shear strength (gf)	Mean	Std Dev
12”	410	30
8”	417	32

Summary of eWLB Component Level and Board Level Reliability Test Results

Moisture Sensitivity Level	MSL1 @ lead free condition (260°C)
Temperature Cycling	-40°C/125°C, 850 cycles -25°C/100°C, 1000 cycles
High Temperature Storage	150°C, 1000 hrs
Unbiased HAST	130°C/85% RH, 96 hrs
Temperature Humidity Bias Test	85°C/85%/5V, passed 1000 hrs
TC on Board	-40°C/125°C, 2 cycles/hr, passed 500 cycles
Multiple Solder Reflow	5x, 10x and 20x reflows with minimal reduction in bump shear strength
Drop Test	Passed JEDEC drop test for 8 x 8mm, 183 balls (0.5mm pitch)

6. eWLB Move to Larger Scale

- 12”x12” square panel area is increased more than 30% compared to a 12” wafer because the square panel saves corner space.
- Significant cost and productivity advantages can be achieved with the larger scale reconstituted wafer eWLB format due to higher efficiency and economies of scale.



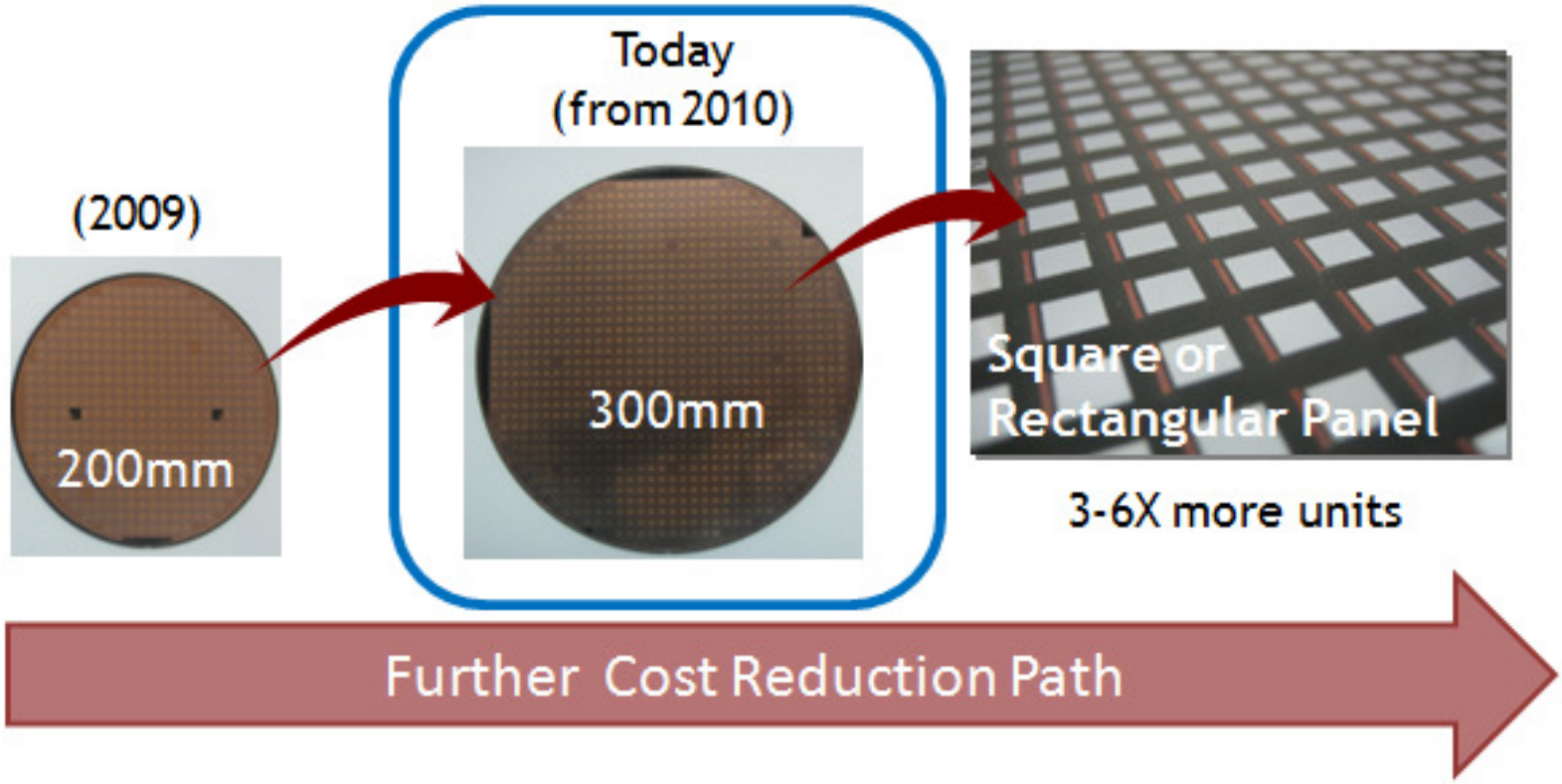
Economies of Scale

Economies of scale arise when the cost per unit falls as output increases. Economies of scale are the main advantage of increasing the scale of production and becoming 'big'.

i) Firstly, because a large business can pass on lower costs to customers through lower prices and increase its share of a market.

ii) Secondly, a business could choose to maintain its current price for its product and accept higher profit margins.

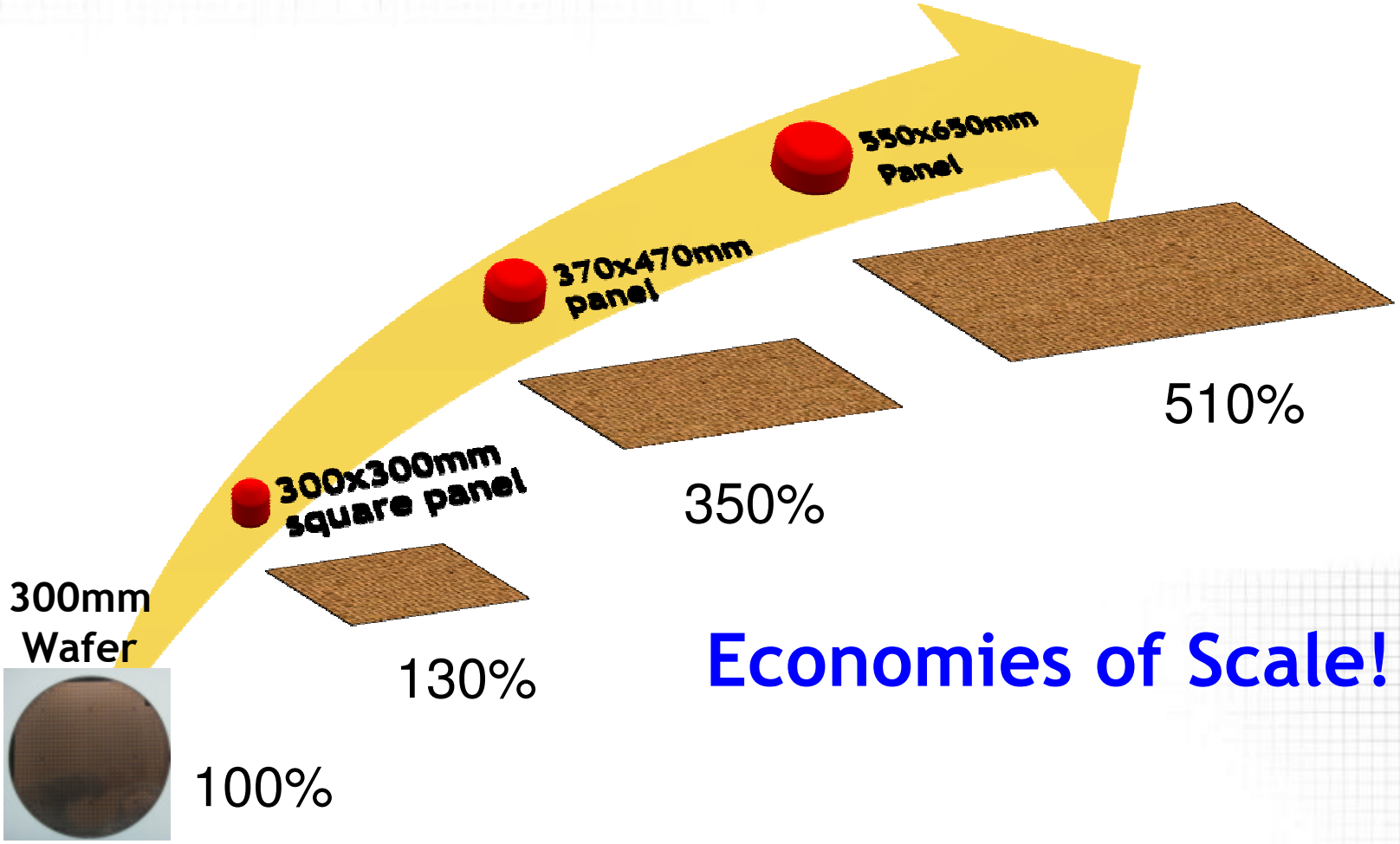
eWLB Moving to Larger Scale



Confidential

Area Increase with Panel Size

More throughput with lower cost



Economies of Scale!

7. Summary & Conclusion

- Wafer level packaging is a key technology enabler for future products and eWLB extends the application space.
- eWLB enables heterogeneous integration with improved electrical performance in a thin package.
- eWLB provides low-cost solution with batch process and larger area utilization.
- 300mm eWLB was successfully developed with warpage optimization and has been in HVM since 2010.
- Economies of scale are the main advantage of increasing the scale of production and becoming ‘big’.
- Further cost reductions after 300mm eWLB can be achieved by scaling-up the panel size. This will be the next significant step in cost reduction.