7th International Conference and Exhibition on Device Packaging

Stacking of Known Good Rebuilt Wafers without TSV – Industrial Applications

Presented by Dr Christian Val
Founder and CEO of 3D Plus/France

Scottsdale Arizona, USA March 8-10, 2011

PLAN

- Introduction
- Technology of the Stacking of Rebuilt Wafers
- Comparison between PoP/W2W and WDoD
- Applications
- Conclusion

Company Highlights

- Spin off from Thales (1996)
- Strong R&D from the 3D Plus launching
- Active patenting policy
- Space certifications from CNES, ESA, NASA, JPL
- ISO 9001
- Revenue 2010: M€ 21 (M$ 29) ; Profit: M€ 5,5 (M$ 7,6)
- Workforce : 115
- R and D : 12 including 6 PhD

PLAN

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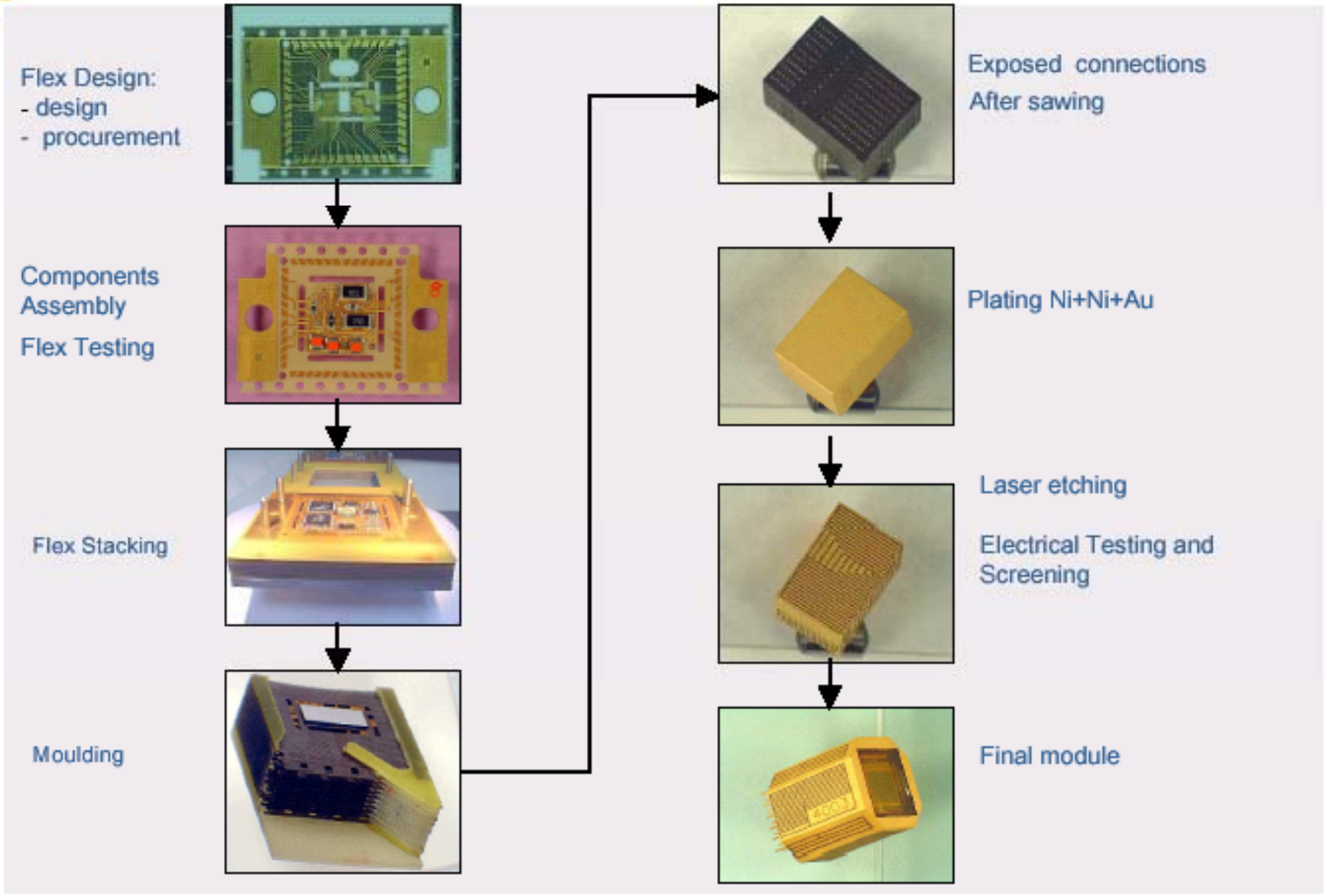
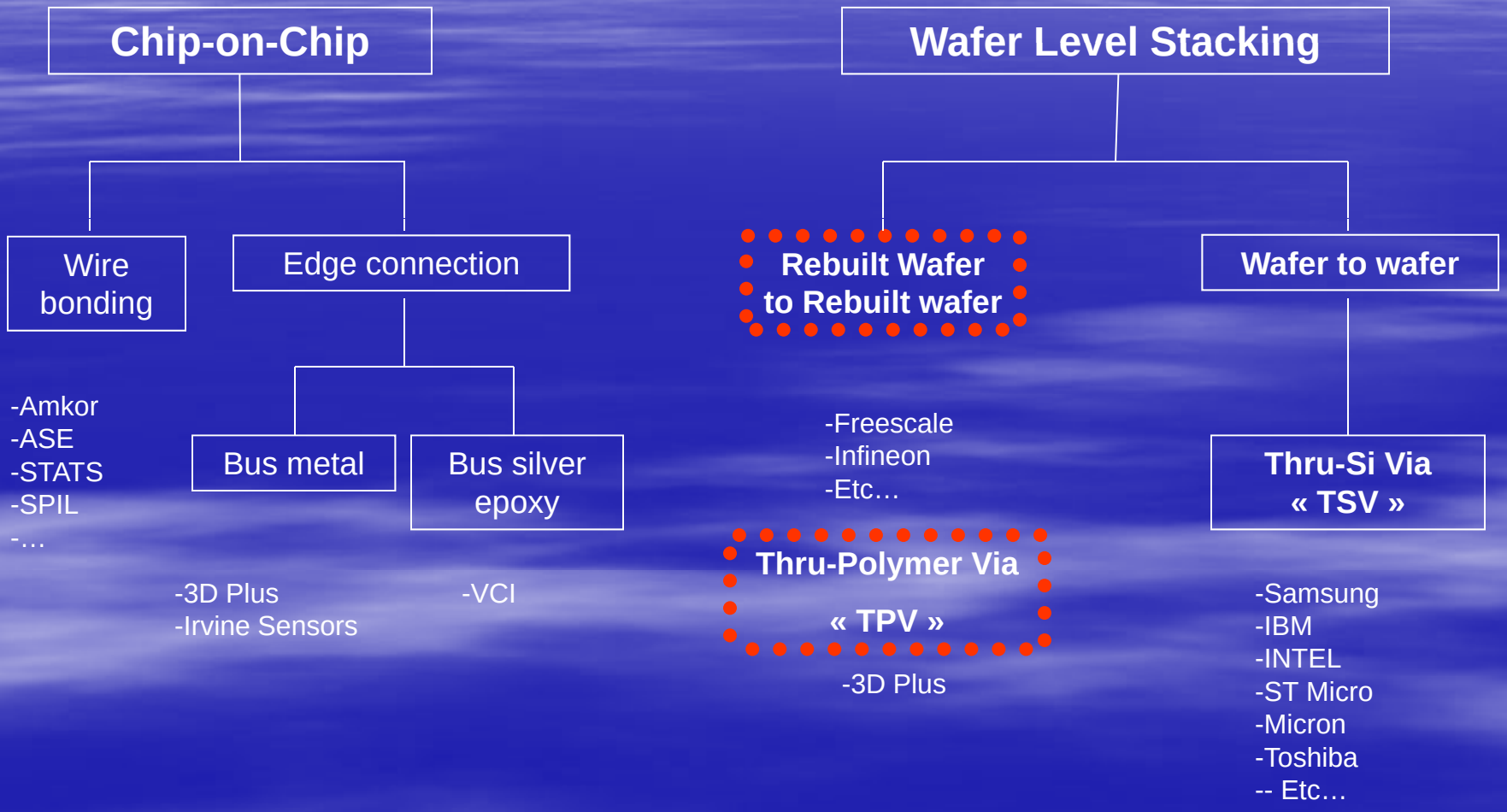
Technology – Flow 2 Chart (Flex stacks)



3D Existing Packaging Technology



Limits of Wafer to Wafer with TSV

- Non multi sourcing wafers
- Need for smallest possible Via (2µm Ø, leads to a thickness of 20 µm or less ➔Yield of these filled via is low (redondancy is expected)
- Difficulties with SiP, since die of different sizes
- TSV stresses (keep out zone between 20 to 200 µm)
- Unfortunately impossible to have 100% good wafer ➔ very low global yield

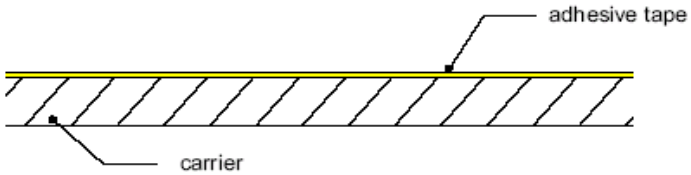
WDoD ™(1) initial criteria

- Use of multi sourcing wafers
- Stacking of 10 levels per mm now, 20 levels/mm in development
- Size: 100µm around the larger Die
- Stacking of Known Good Rebuilt Wafer (KGRW)
- Possibility to stack Known Good Burn-In Rebuilt Wafer
- Parallel processing/Panelization from A to Z

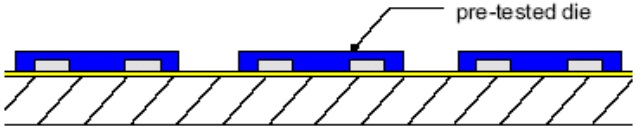
(1) Wirefree Die on Die – Trade Mark from 3D Plus

FLOW 3 " WDoD"

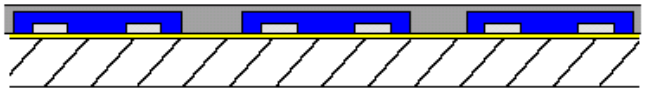
1 - Carrier lamination



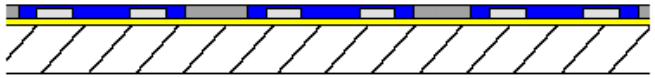
2 - Pick, Flip and place / Die on tape



3 - Compression Molding / Panel encapsulation

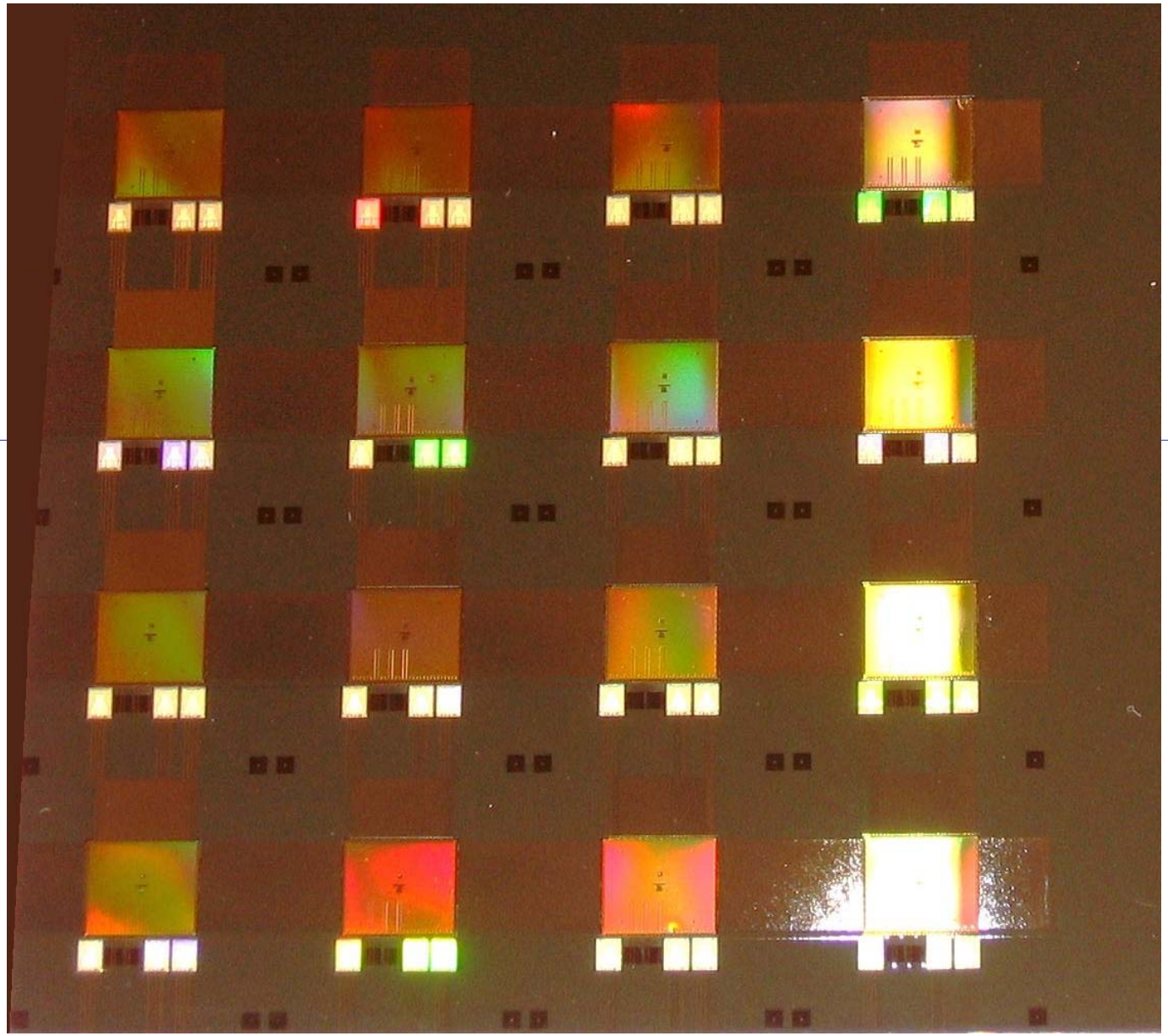


4 - Grinding (optional)



5 - De-taping

6 - Redistribution layer "RDL"

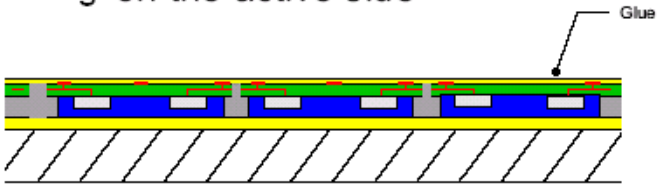


History of the development of "Rebuilt Wafers"

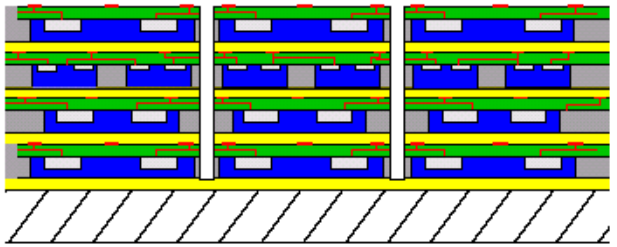
- 2002- WALPACK/3D Plus, ST Micro, CEA/LETI, AXALTO …
- 2005 – Freescale launched a 200 mm "RCP" Line in Austin (USA)
- 2007- Freescale launched a 300 mm "RCP" Line in Phoenix (USA)
- 2008- Infineon launched a 200 mm "eWLB" Line in Dresden (DE)
- 2008- ASE + STATS ChipPAC launched a 200 mm Line in (Singapour)
- 2009- ASE launched a 300 mm Line in Singapour (Qualif at the end 2010)
- 2009- CASIO + CMK has a 200 mm Line in Japan
- 2009- FUJIKURA launched a 200 mm Line for RF applications in Japan
- 2009- King Dragon Int probably launched a 400 mm panel Line in Taiwan
- 2009- Freescale signed a partnership Agreement with NEPES (Korea) to build a 300 mm Line in Singapour (Qualif at the 3rd quarter of 2010)
- 2010- NANIUM ex Siemens then Infineon, now Independent Company is qualifying a 300 mm Line in Portugal (Qualif at the 3rd quarter 2010)
- 2010- Tong Hsing is building a "RCP" Line at the 2nd semester of 2011 in Taiwan
- In yellow are the companies which ones we have contacts

FLOW 3 " WDoD"

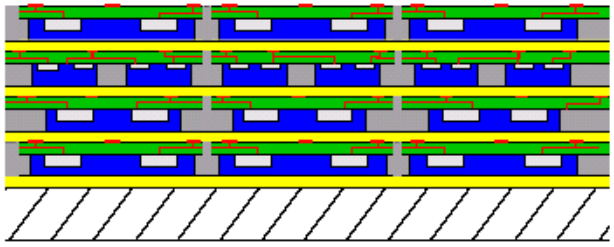
7 - Gluing on the active side



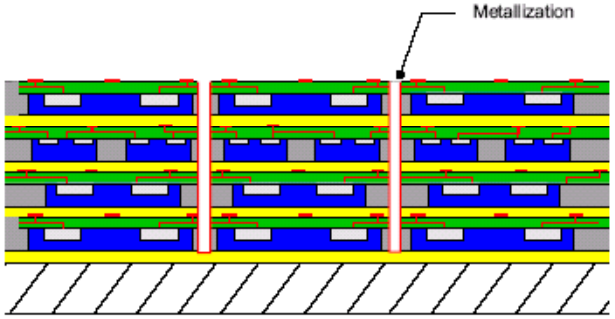
9 - Dicing of the rebuilt and stacked wafers



8 - Stacking of the "Known Good Rebuilt Wafer"

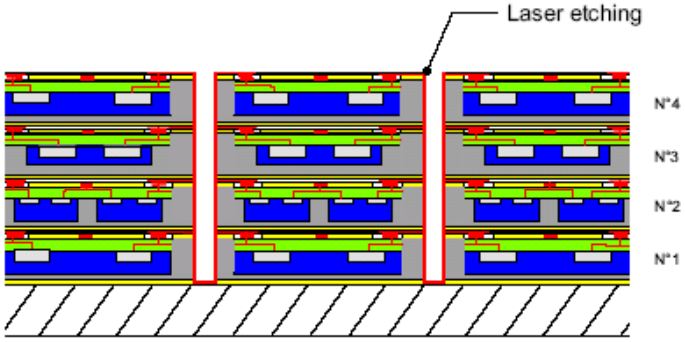


10 - Dicing street edges plating parallel process (electroless Ni + Au)

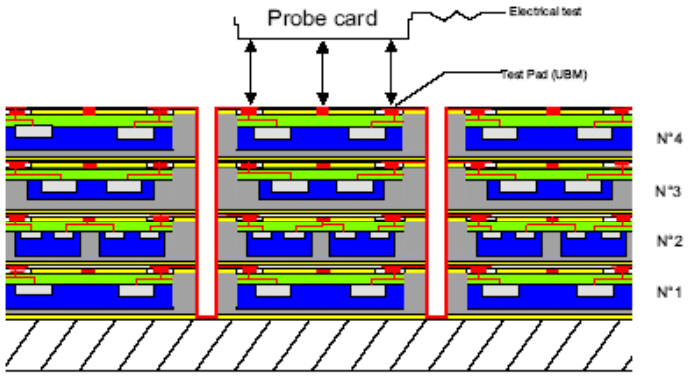


FLOW 3 " WDoD"

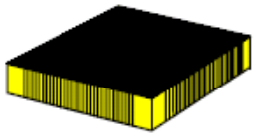
11 - Laser patterning inside the dicing street edges plated



12 - Electrical test at the wafer level
(Before singulation)

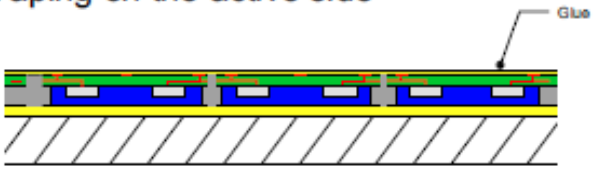


13 - Singulation

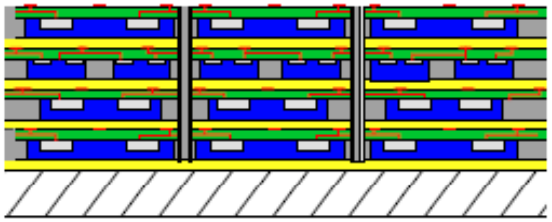


FLOW 3 " WDoD" with TPV

7 - Taping on the active side



9' - Thru - Polymer - Via "TPV"



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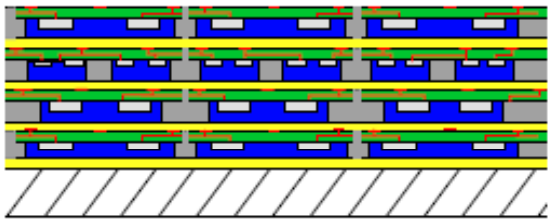
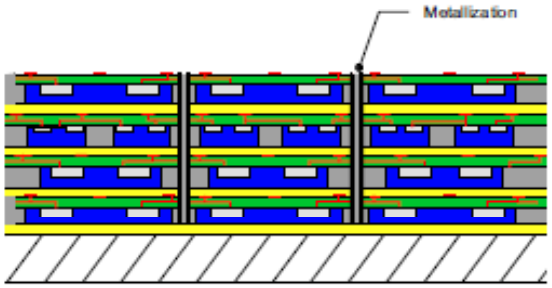
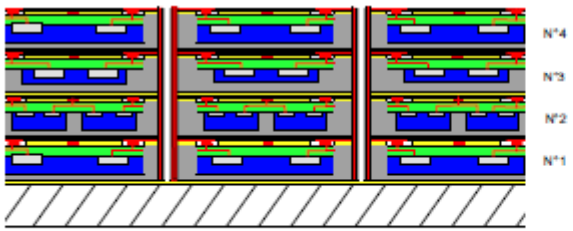


10' - Plating - "TPV"

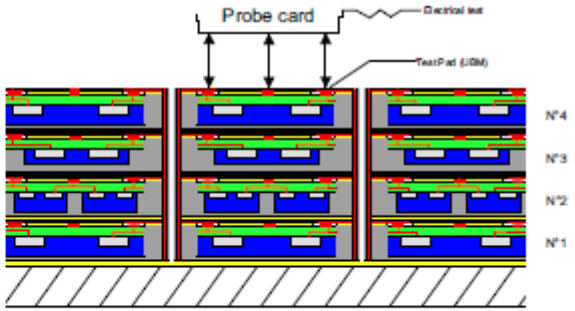


FLOW 3 " WDoD" with TPV

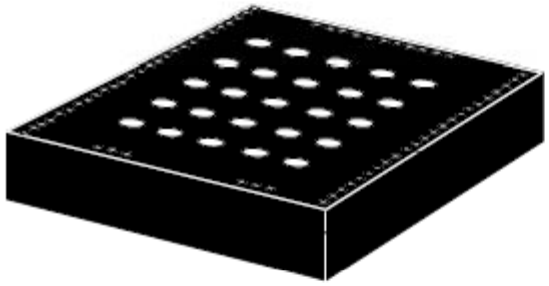
11' - Dicing of the rebuilt and stacked wafers



12' - Electrical test at the wafer level
(Before singulation)



13 - Singulation



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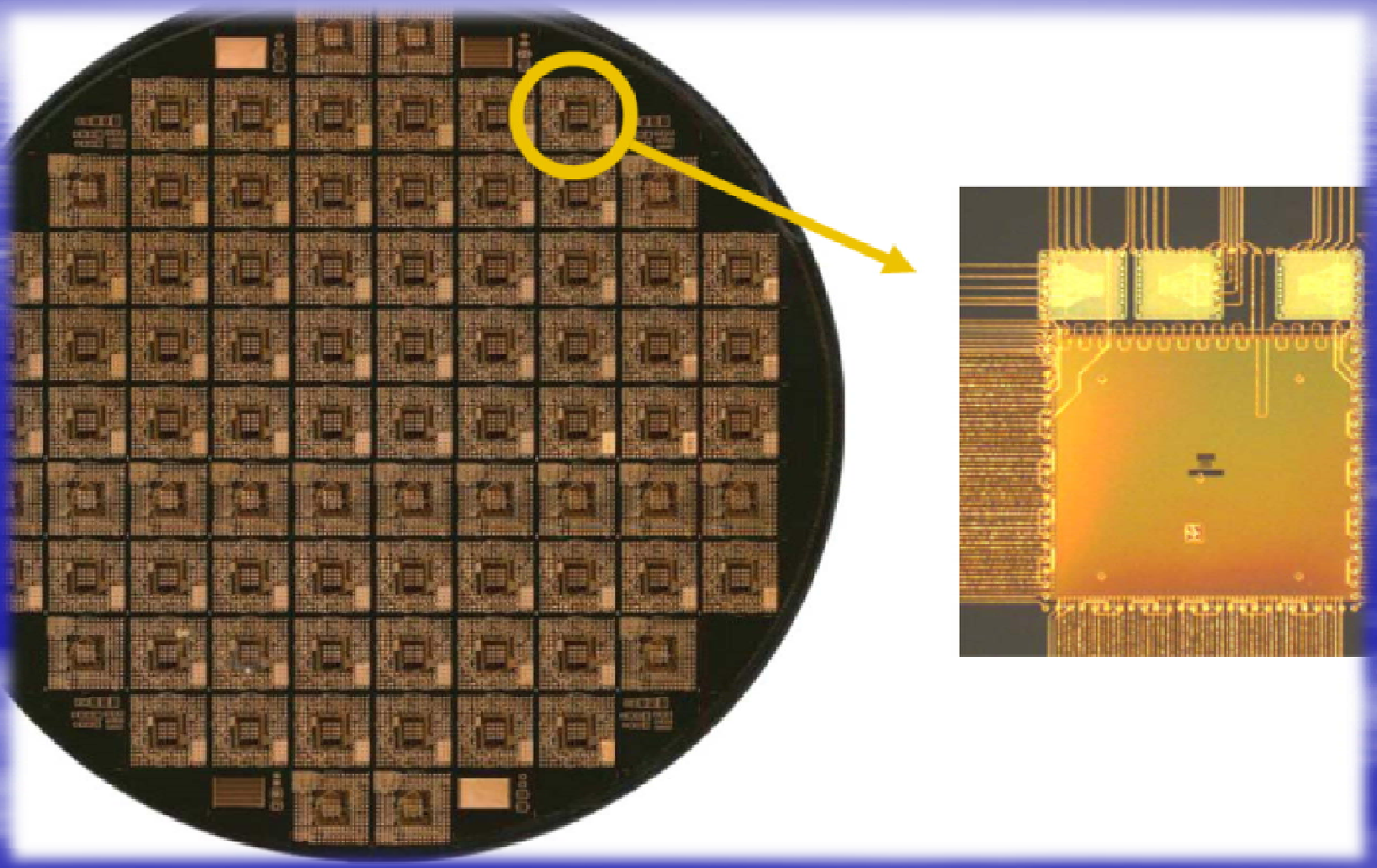
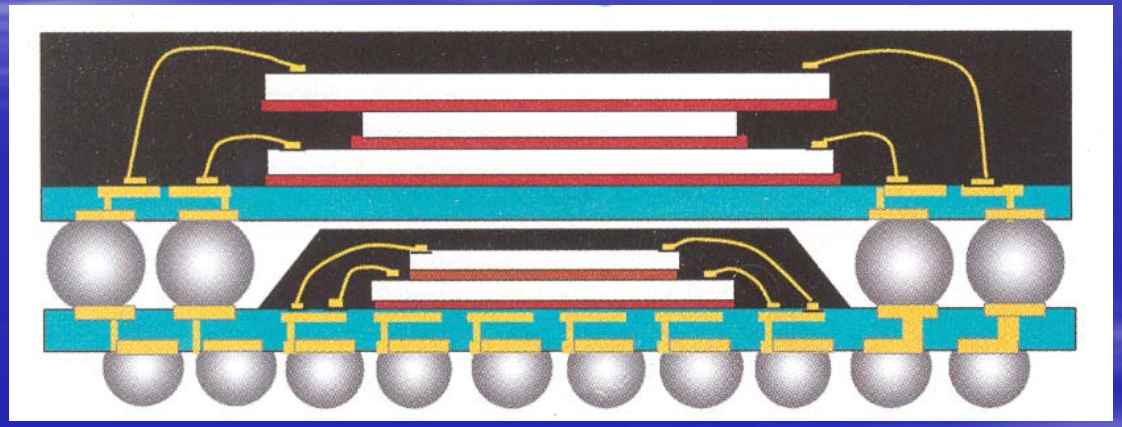
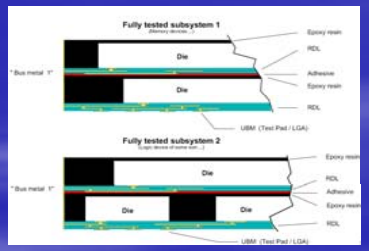


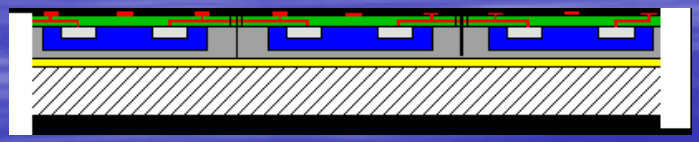




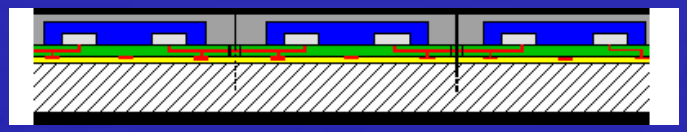
PoP and WDoD package

Flow 3 – « WDoD » with Known Good Burned-in wafer

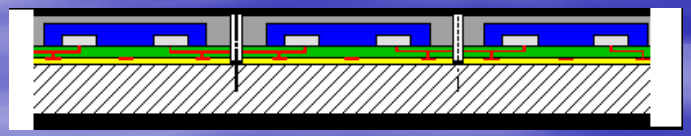
7- Electroless Ni/Au « UBM »



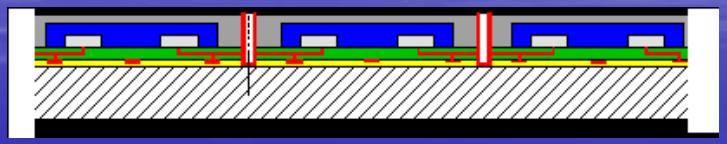
8- Taping



9- Dicing

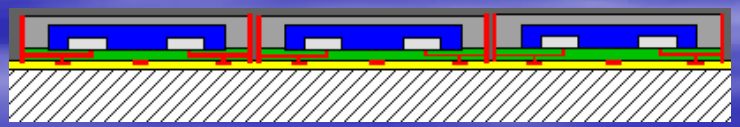


10- Dicing street edges plating (Electroless Ni/Au)



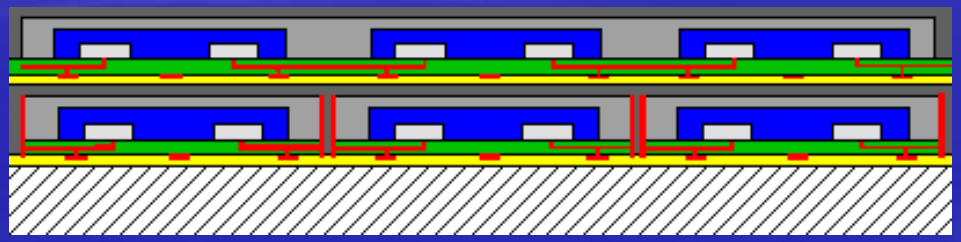
11- Electrical tests and Burn-in (LGA sockets)

12-Pick and Place + second moulding of the moulded Burn-in packages

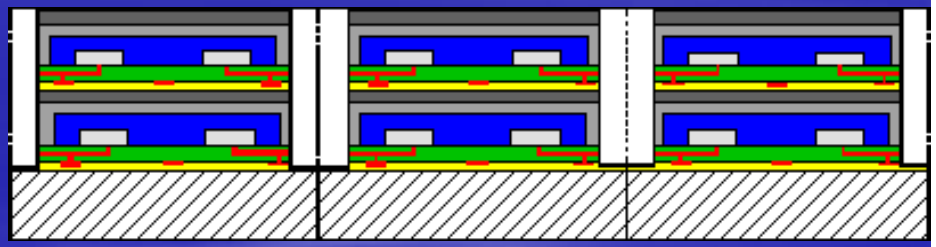


Flow 3 – « WDoD » with Known Good Burned-in Wafer

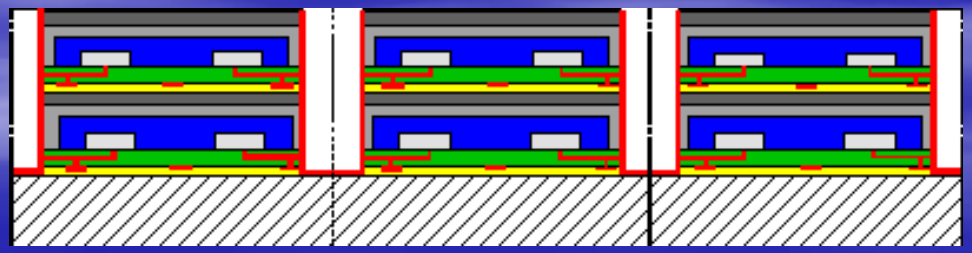
13-Stacking of the Known Good Burned-in Wafers with the other 2,3,n…
.Known Good Wafers



14- Dicing with larger blade



15- Plating (Electrless Ni + Au)



Fan-out / Fan-in / µ-Fan-out

- **Fan-in WLP**: the package is essentially built on top of the wafer using wafer level batch processes
- **Fan-out WLP**: Developed to allow for higher ball count WLP, by extending the package size beyound the area of the chip
- **µ-Fan-out WLP**: 3D Plus uses a µ-RDL on the die and the polymer around it (100 to 300 µm around this die). This approach allows to only have one layer RDL outside the die.

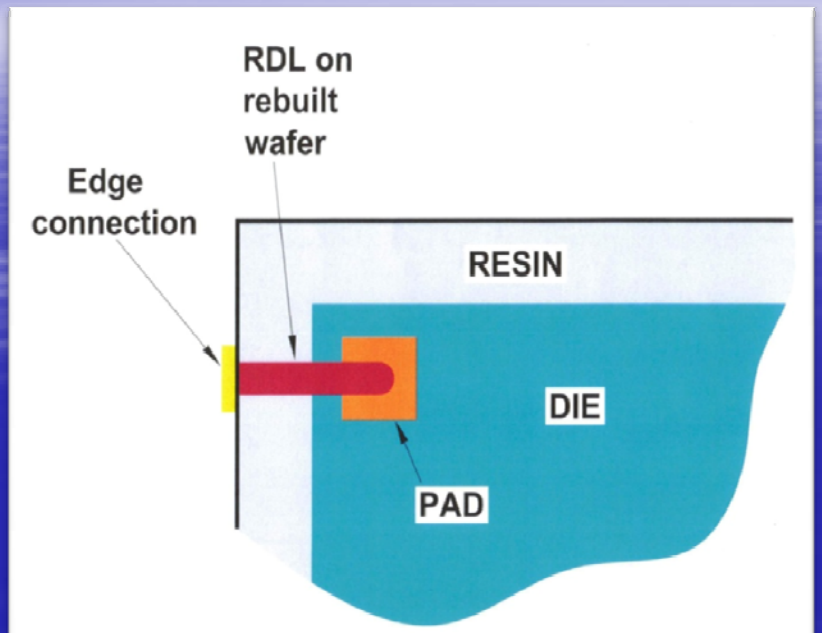


Fig. 3 : µ Fan-out
option 1 : RDL after moulding

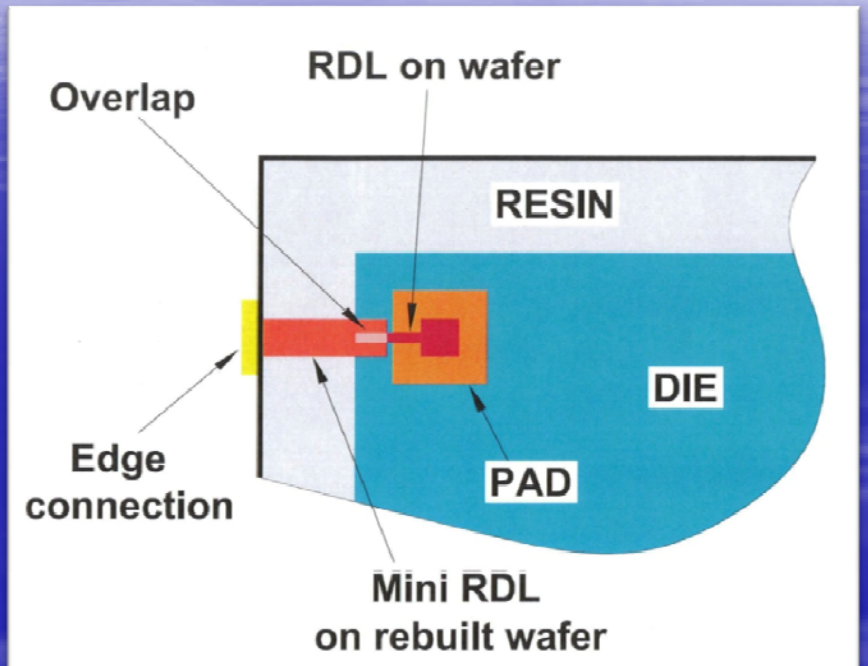


Fig. 4 : µ Fan-out
Option 2 : RDL on the wafer
before Moulding

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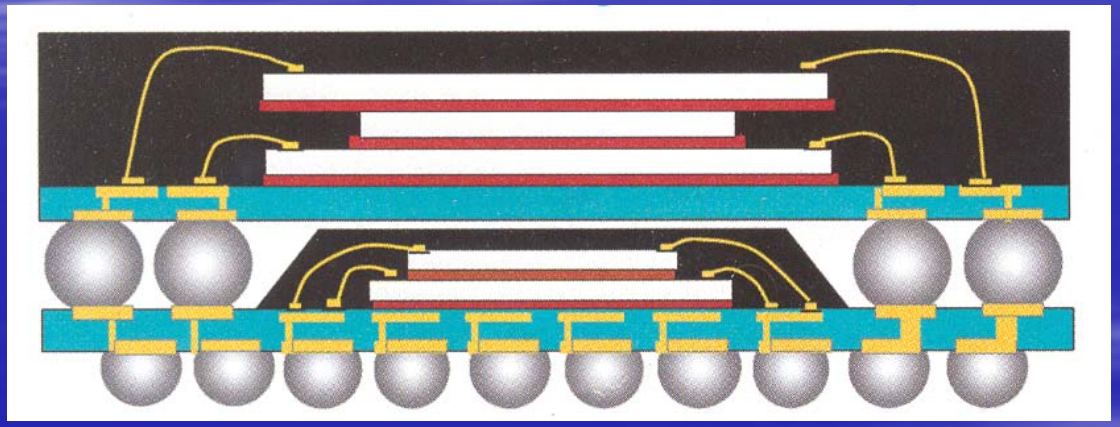

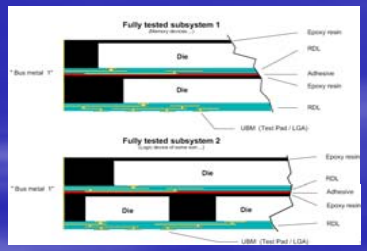

PoP and WDoD package

COMPARISON BETWEEN WAFER LEVEL PACKAGE WITH TSV, WITHOUT TSV AND PoP TECHNOLOGIES

	PoP	WAFER LEVEL PACKAGE	
		Wafer to Wafer with TSV	Rebuilt Wafer to Rebuilt Wafer without TSV
Stacking of different size of the die			
More than 1 Die/Level			
Sourcing flexibility			
Test and / or burned-in before stacking			
Package size			
Package height			
Cost			

Best
Good
OK
Poor

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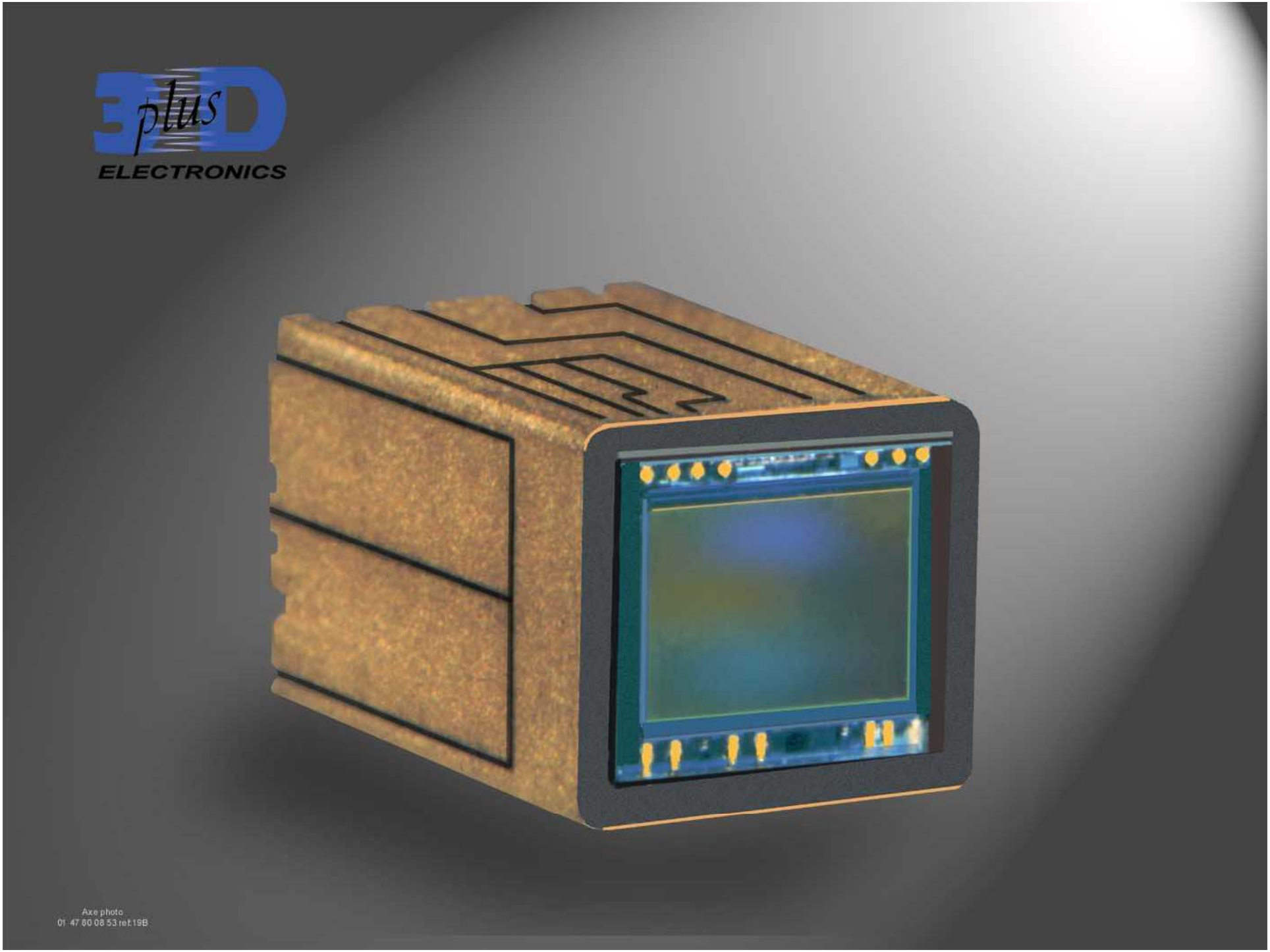
NICHE APPLICATIONS

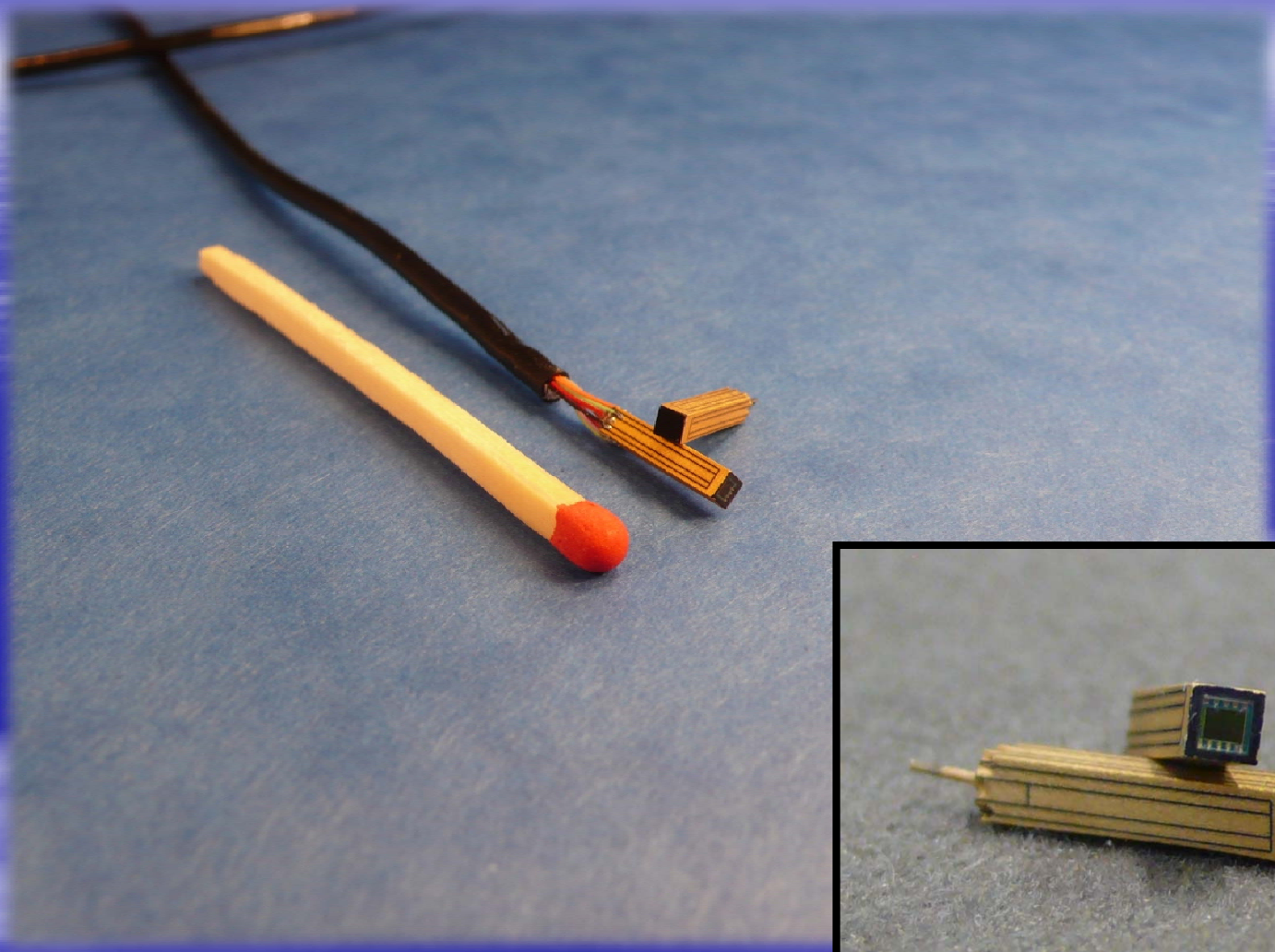
MEDICAL APPLICATIONS:

- Micro camera for Endoscopy (2,6 x 2,6 mm)
- Modules for Pacemaker, Neuro stimulator
- Module for 40 silicon capacitors on 20 levels
- Earing aids
- X Ray camera with Philips/ Germany
- European program/ e-CUBES with pacemaker
- European program/ e-BRAINS with MEMS

INDUSTRIAL APPLICATIONS
"Structural Health Monitoring"

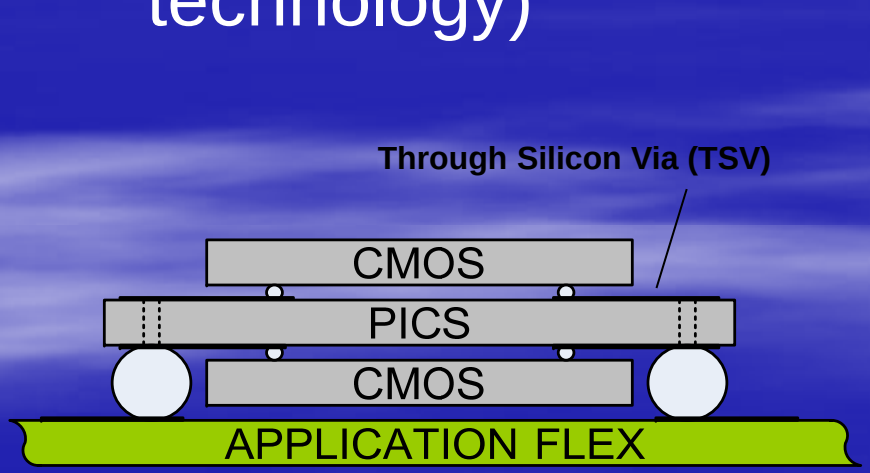
- Abandoned Sensors for avionics
- Stacking of FPGA (bare die) + DDR3 + PROM for military and industrial applications

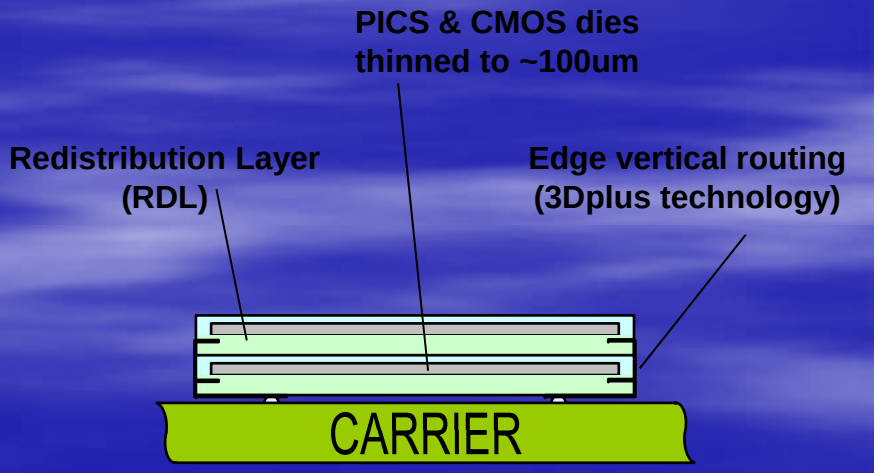


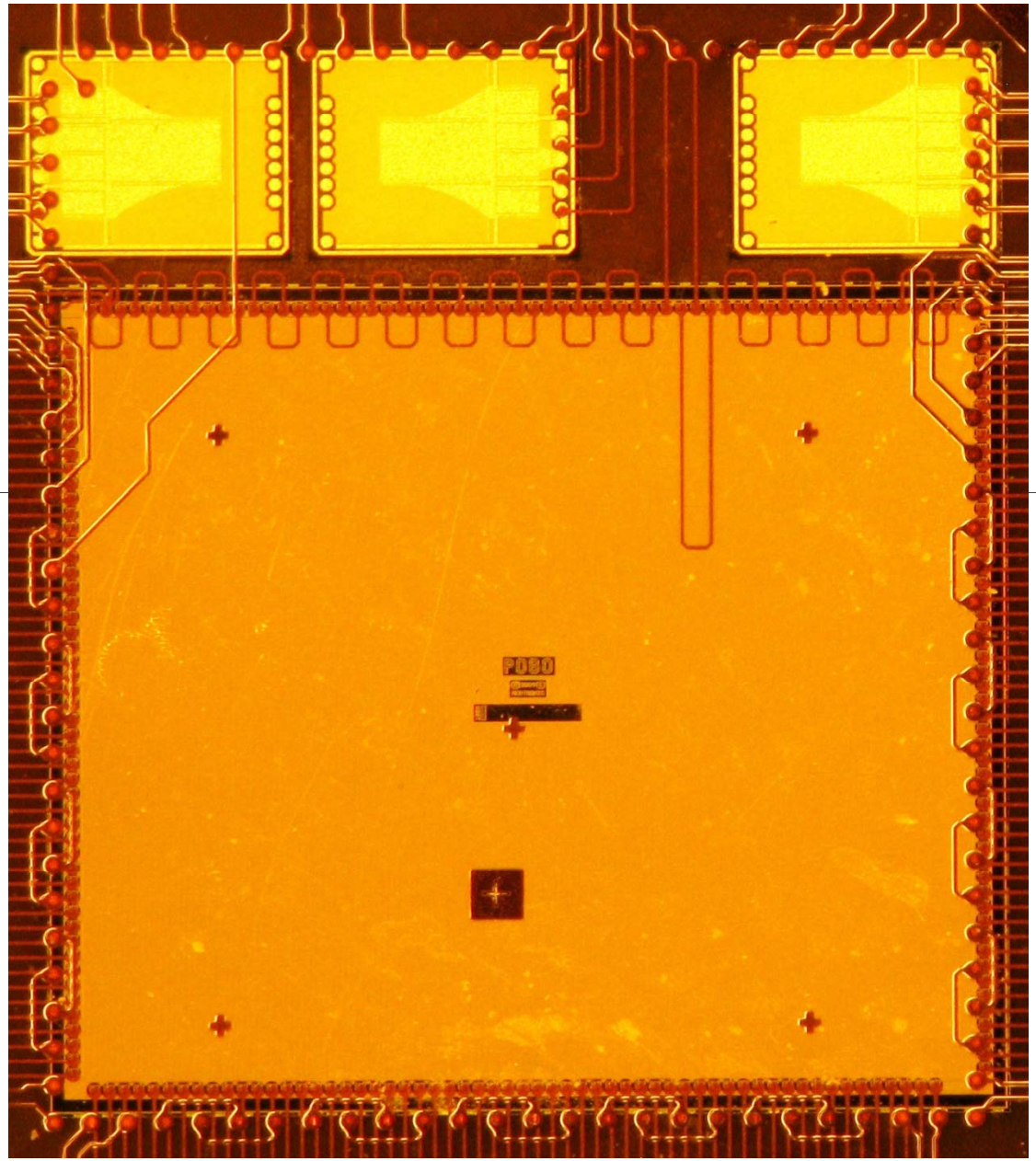


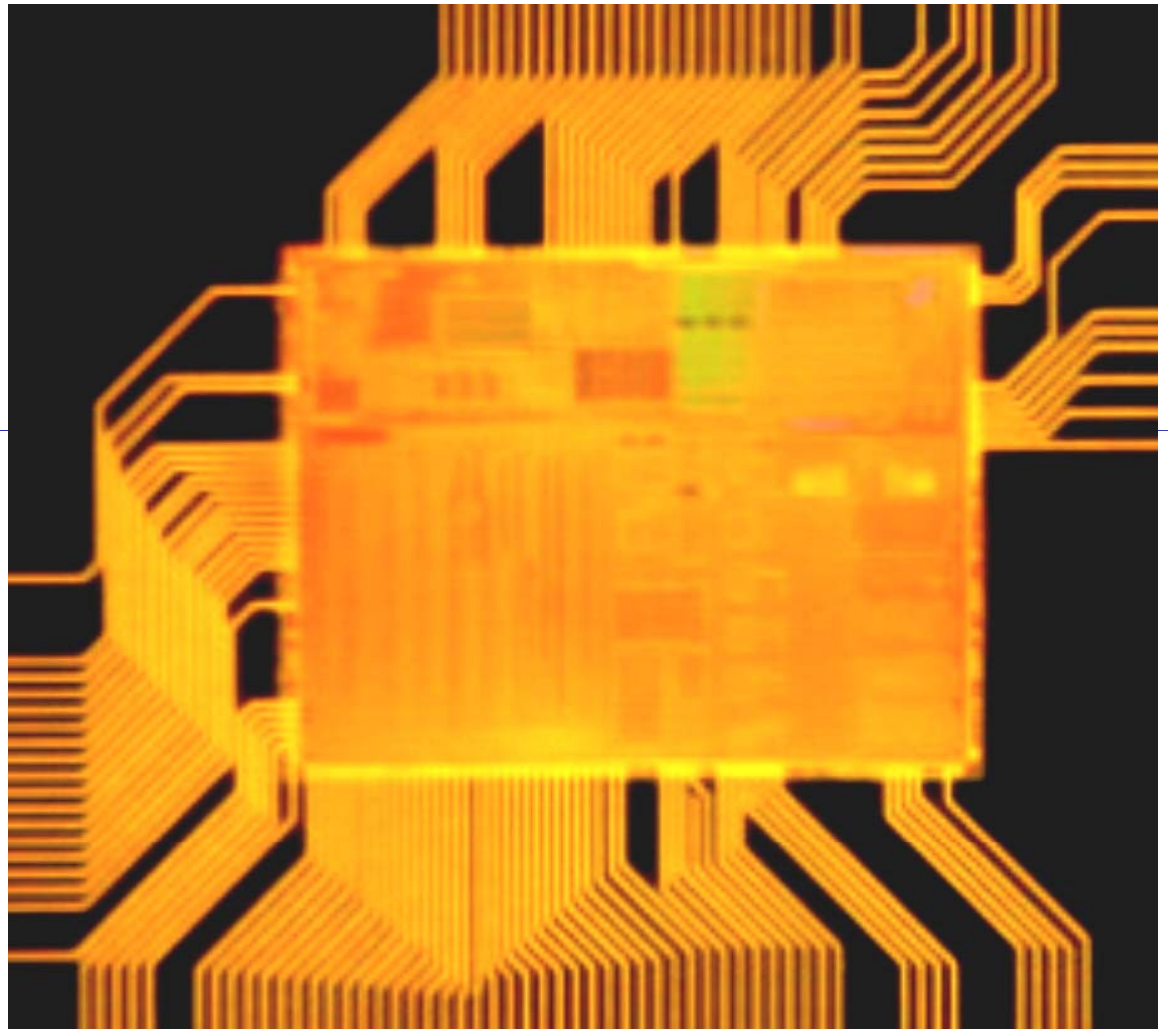
Contribution to e-Cubes – Program
(from NXP Belgium)

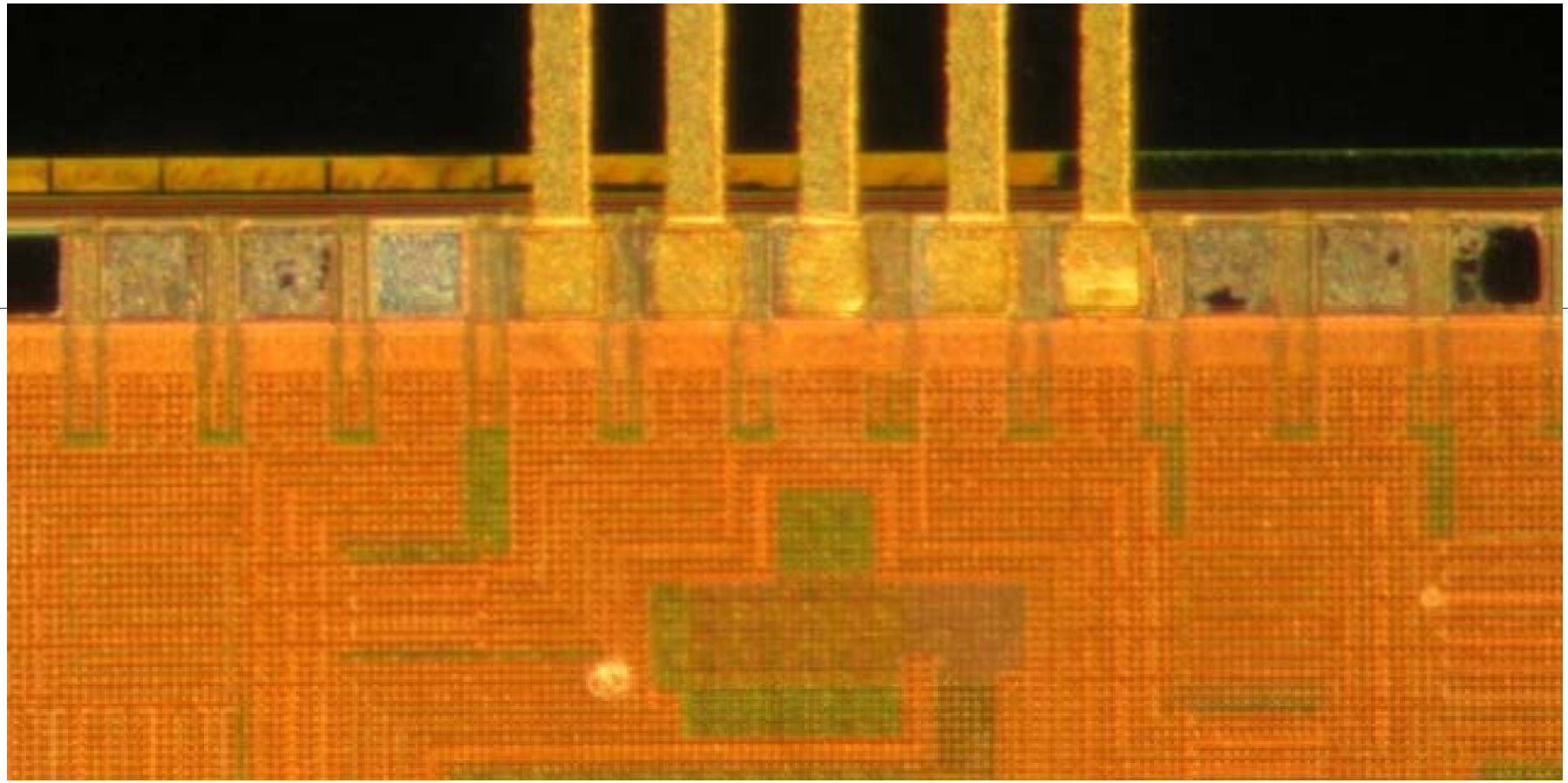
- Going further than flip-chip – 3D SiP integration for hearing aids
  - Through Silicon Vias (TSV)
  - Edge Vertical Routing (Based on 3DPlus technology)

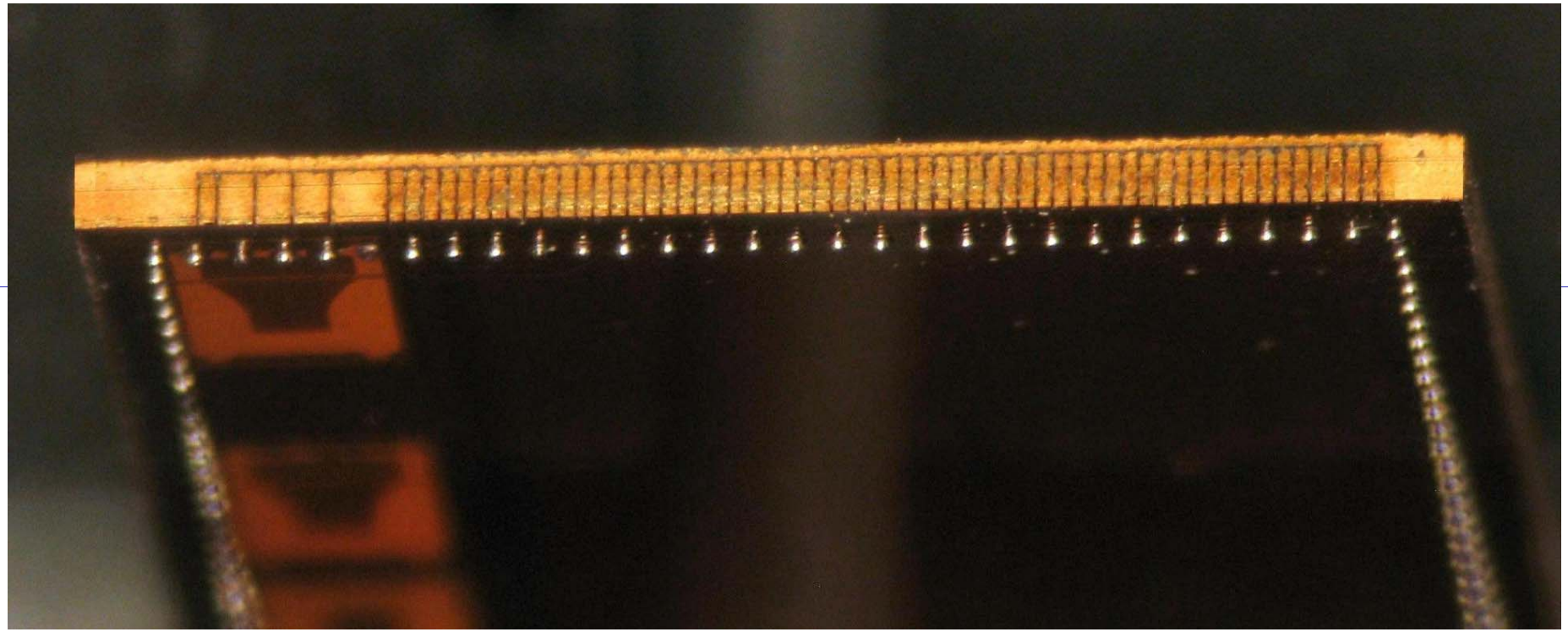






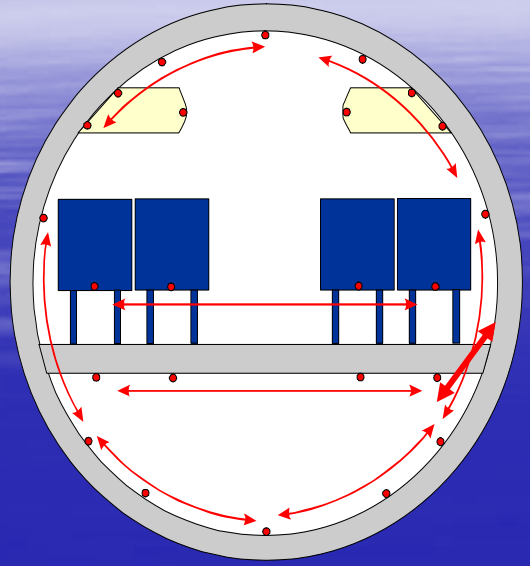


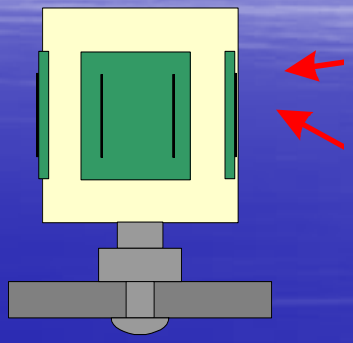


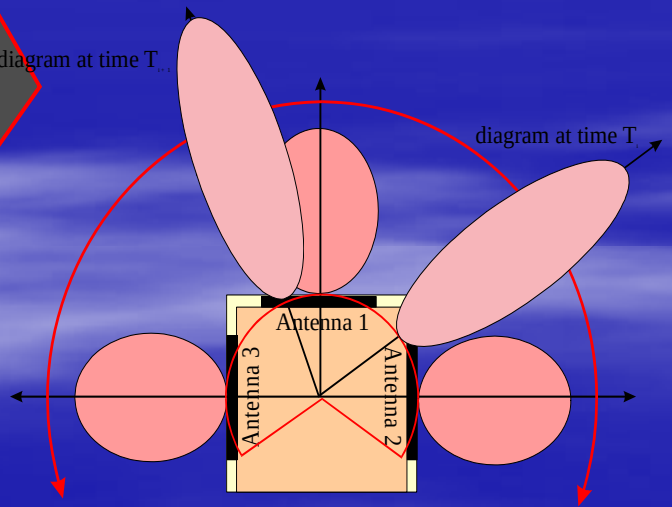


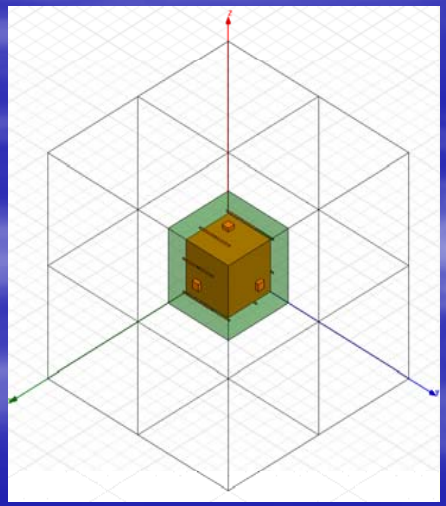
Structural Health Monitoring

Abandoned Sensors

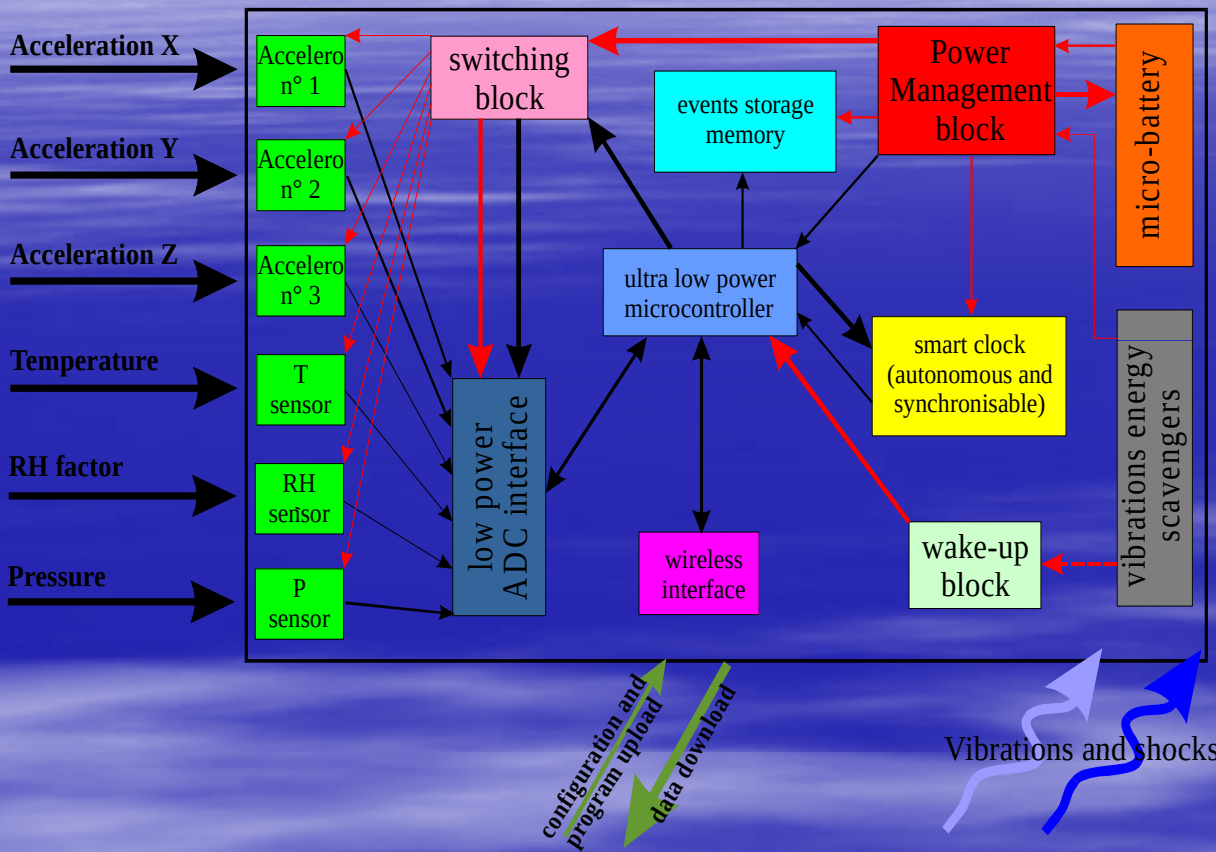


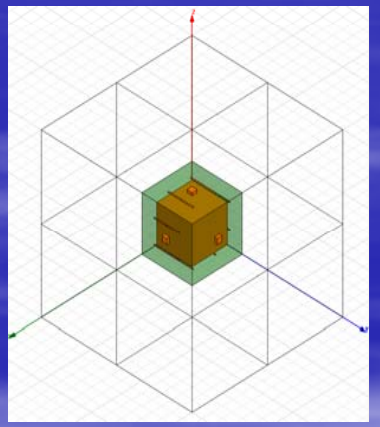






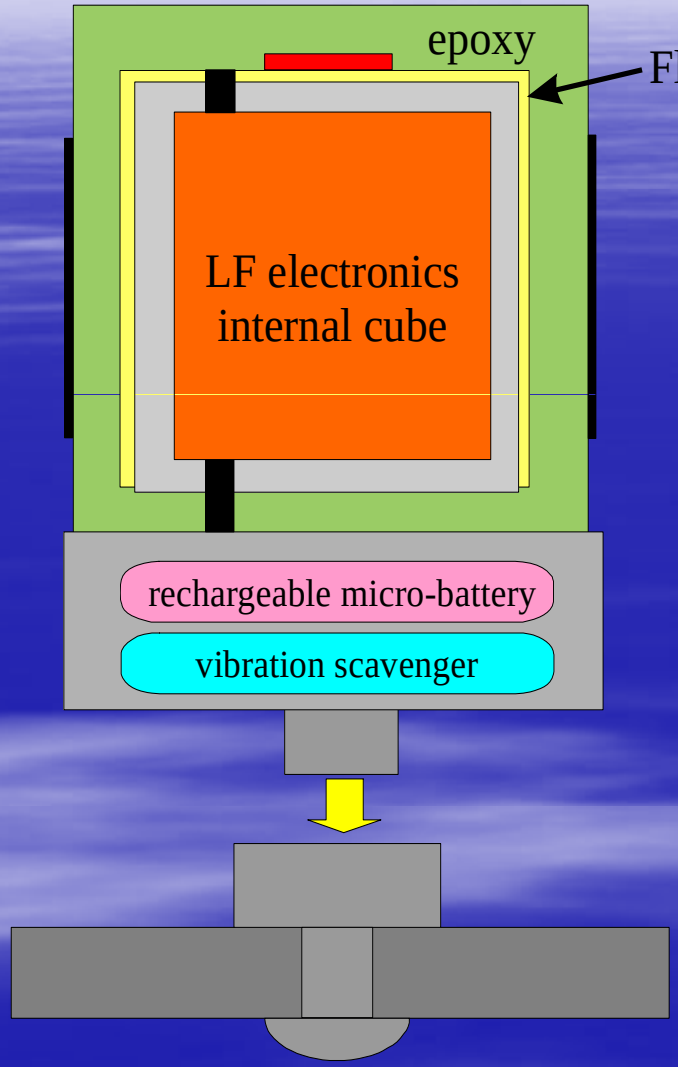
3D PLUS Demonstrator
e-CUBES Program





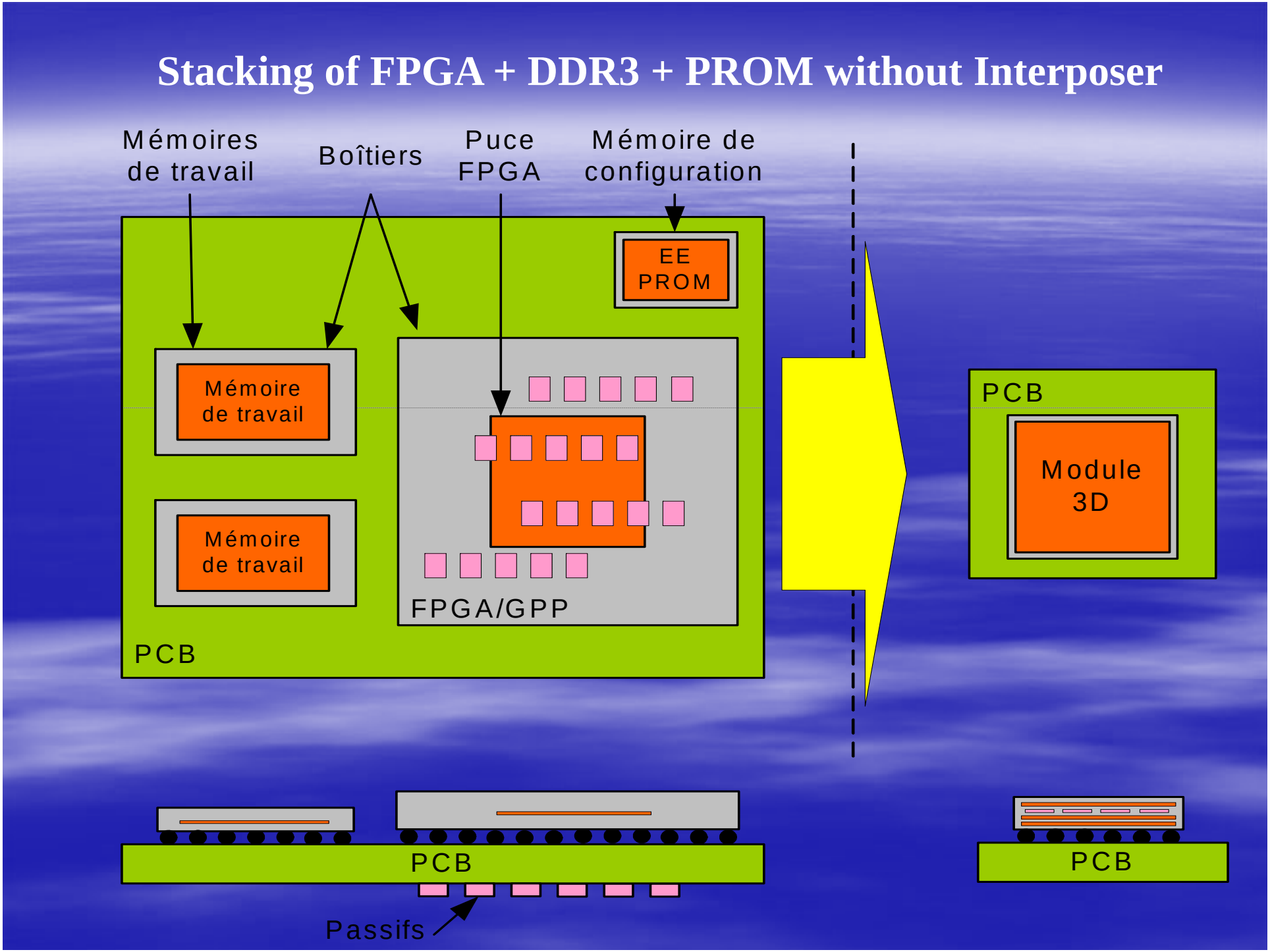
3D PLUS Module

Abandoned Sensors e-CUBES Program



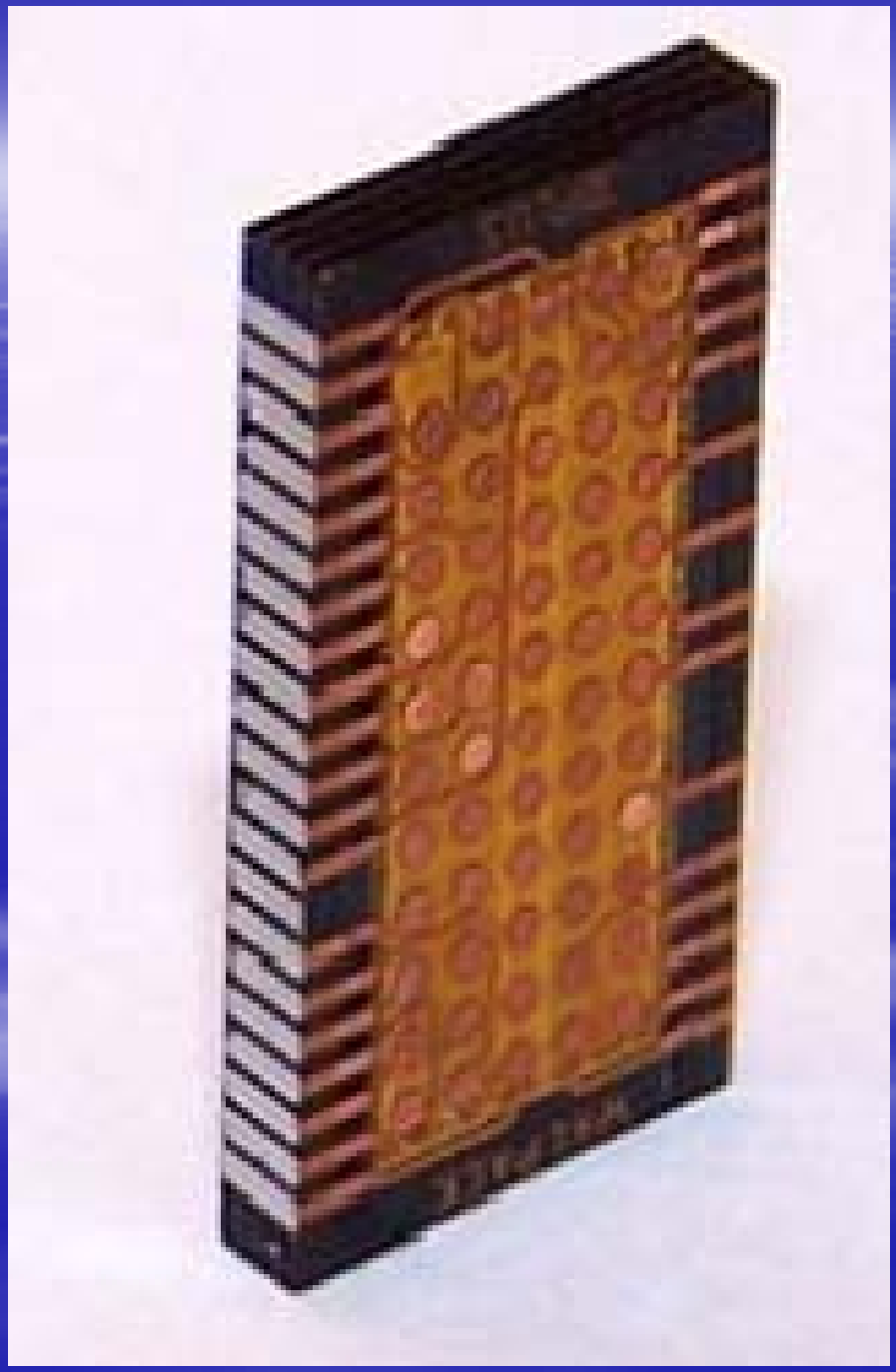
- 1 RH and 1 P transducers on top
- 1 T transducer on each face
- Pads on bottom for connexions to the RF block
- Pads at the top (energy + “rescue operations”)
- Specific anti-screwing fixation
- Internal cube = 8 mm X 8 mm X 14 mm (Target: 6 x 6 x 6 mm/ 0,22 cm3)

Stacking of FPGA + DDR3 + PROM without Interposer



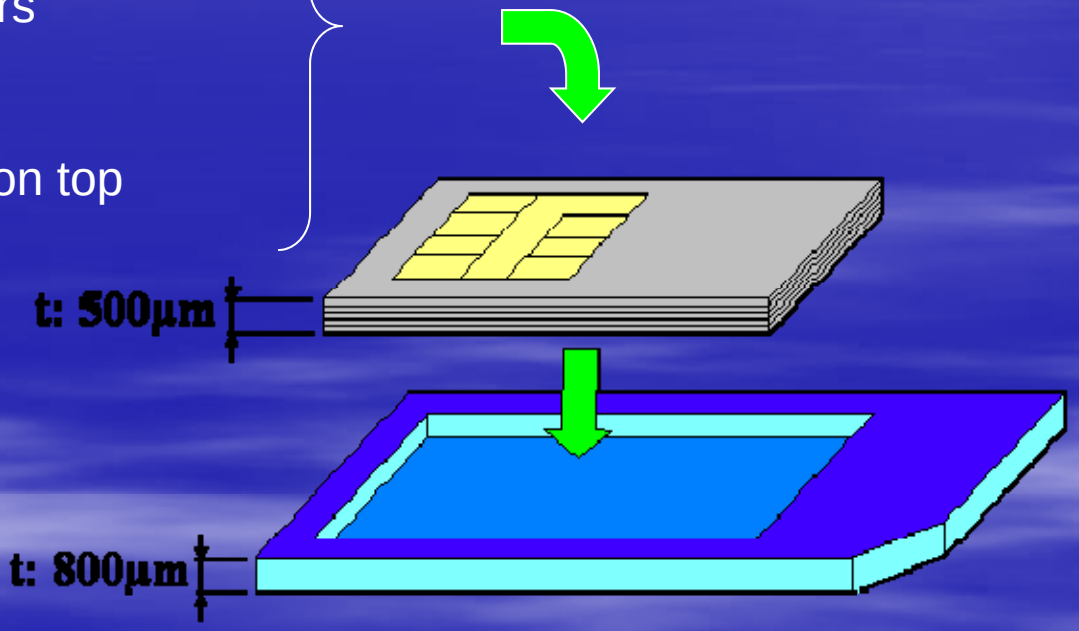
VOLUME APPLICATIONS

- SRAM Modules
  - 8 memories (1mm with balling)
- Mega SIM
  - 5 levels within 500 µm (in a cavity inside the standard 800 µm SIM Card)
- DDR3 stacking for wide Bus (in process with Nanium ex Siemens/Infineon in Europe)



MEGA SIM

- ✓ 4 Flash
- ✓ 1 Microcontroller
- ✓ Silicon Capacitors
- ✓ Oscillator
- ✓ 8 ISO Contacts on top



To be embedded in card or key

Stacking of DDR3

- ✓In development with NANIUM (ex SIEMENS/INFINEON/QIMONDA in Portugal with « e-WLB » 300 mm
- ✓For JEDEC qualification of the WDoD
- ✓Results on the second semester of 2011

WDoD™ Status

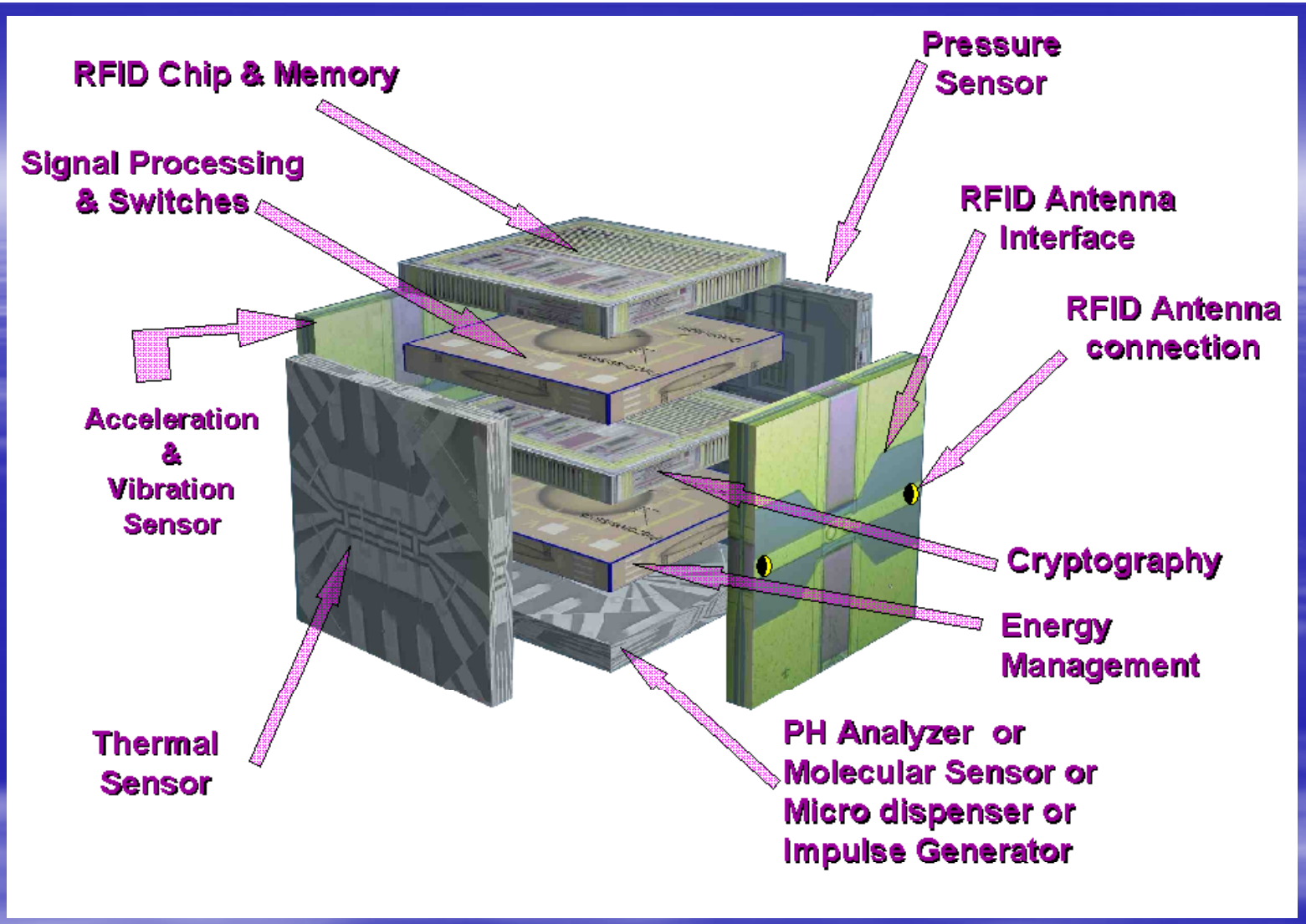
- Proof of Concept – completed (2002-2005)
  - European funding (25 M$) with CEA/LETI, GEMALTO, ST Microelectronics, 3D PLUS, …
- Process Development & Optimization of WDoD (from 2006 up to Feb 2009) with NXP/Philips semiconductor
- From Feb 2009 Prototyping with the RCP Process from Freescale/Phoenix
- Functional Prototypes with DDR3/JEDEC Qualifications (second Semester of 2011)

PLAN

- Introduction
- Stacking of Rebuilt Wafers
- Comparison between PoP/W2W and WDoD Technologies
- Applications
- Conclusion

Conclusion and perspectives

- **Miniaturization for Consumer, Medical and security domains demands very high interconnection densities and low costs . Reconsidering former experiences: Hybrids,Multichip Modules, Wafer Scale Integration (20 years ago), PoP instead of PiP; we learned that the yield constitued an important part of the production costs.**
- **The WDoD process only allows to stack Known Good Rebuilt Wafers .**
- **Several applications in the medical and industrial areas have been presented.**
- **This important densification of 10, soon 20 levels per mm, allows to launch extremely ambitious applications in the field of System in Package and memories.**



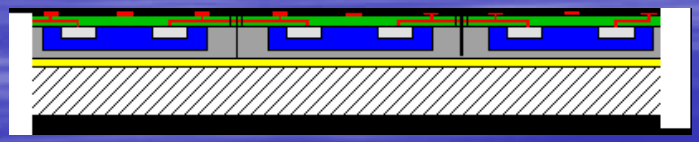
Ultra Dense 3-D Micro system with WDoD

Thank you for your attention

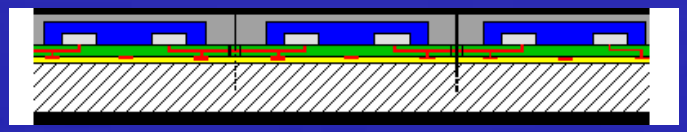
www.3d-plus.com

Flow 3 – « WDoD » with Known Good Burned-in wafer

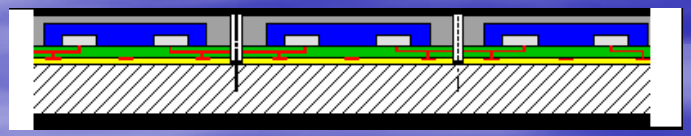
7- Electroless Ni/Au « UBM »



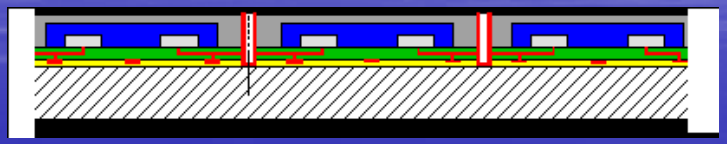
8- Taping



9- Dicing

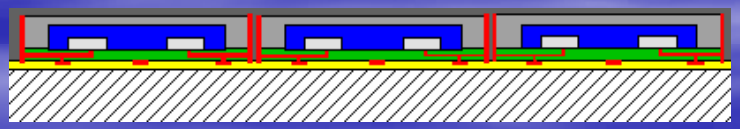


10- Dicing street edges plating (Electroless Ni/Au)



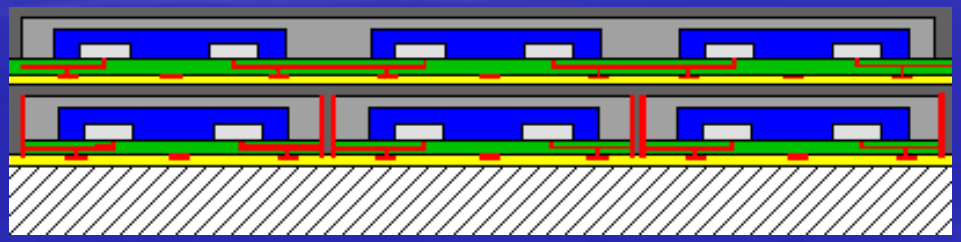
11- Electrical tests and Burn-in (LGA sockets)

12-Pick and Place + second moulding of the moulded Burn-in packages

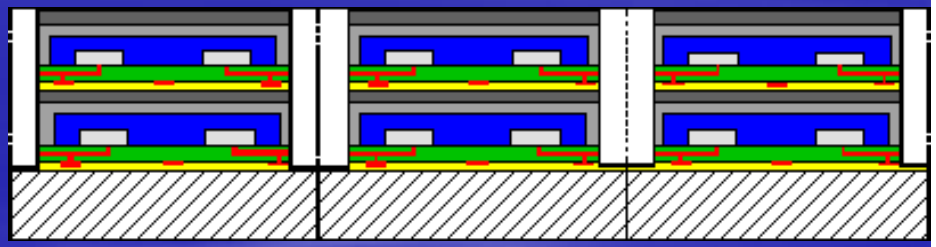


Flow 3 – « WDoD » with Known Good Burned-in Wafer

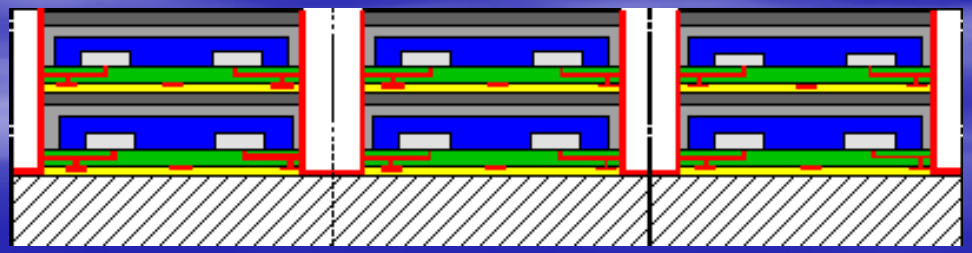
13-Stacking of the Known Good Burned-in Wafers with the other 2,3,n…
.Known Good Wafers



14- Dicing with larger blade



15- Plating (Electrless Ni + Au)



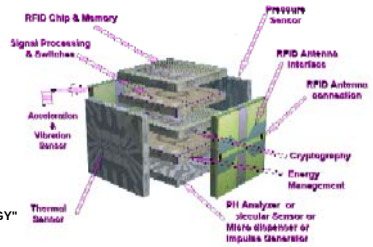
TECHNOLOGY ROADMAP

Function / System Complexity

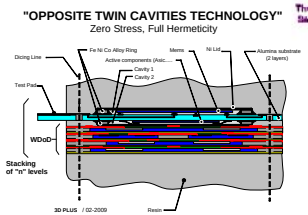
Miniaturization
Volume Flow «0»
Volume Flow «X »

PA BANDONED SENSORS
SIP

Faisability
Evaluation
Qualification
Manufacturing / Aerospace
Manufacturing
(second source)



FLOW 2 to 3.5
+ Antenna

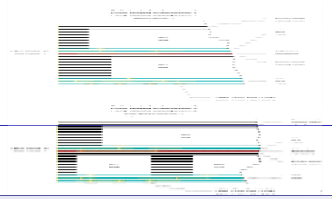


FLOW 2 TO 3.5 + MEMS
«Opposite Twin Cavities Technology»

250 to 400

«WDOD» **FLOW 3.5**
(Thru Polymer via TPV)

-250



MEMORY & SIP

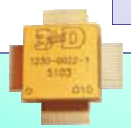
8 Memories
(0,8 mm)

«WDOD» **FLOW3**
(Edge connection)

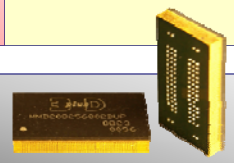
-200

«HIPPIP» - **FLOW 2.5**

-40



Packaged Die / Bare Die - **FLOW 2**



-20

MEMORY

TSOP - **FLOW 1**

- 4

FLOW 0 as a 2D reference : PCB / Surface Mounting Technique

- 1

1997 2002 2003 2004 2005 2006 2007 2008 2009 2010 2011 2012