Processing and Reliability Assessment of Silicon Based, Integrated Ultra High Density Substrates

B.J. Lewis, D.F. Baldwin, P.N. Houston
Engent Inc.

B. Smith, P. Kwok, J. Thompson. A. Mueller, L. Racz
Draper Laboratory

Agenda

- Introduction
- Research Objectives
- Experimental Results
- Summary and Conclusions

Introduction

Introduction

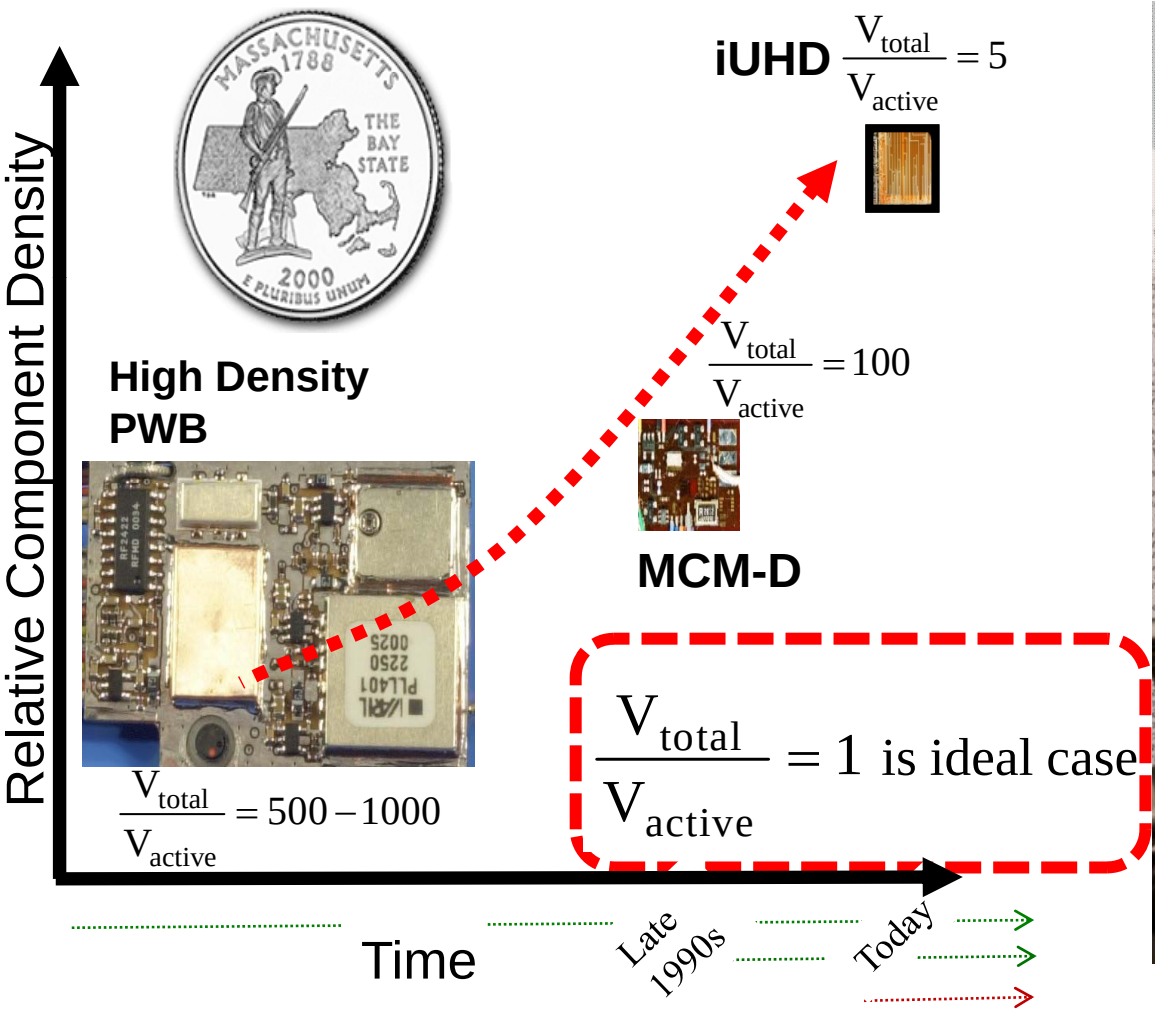
- Standard die packaging of ICs, on traditional organic based substrates, can be 400X the volume of the chip itself

- Using technology that removes the packaging and depositing interconnects directly on the chips can produce 100X size reductions. MCMs incorporating the packaging of multiple ICs and passives together can provide this size level of reduction.

- An approach has now been developed that builds layers off a silicon-based substrate, with cavities etched in the silicon to add buried die. Photo-defined TSV posts then provide connectivity through the layers with lines and spaces that are in line with semiconductor level routing density.

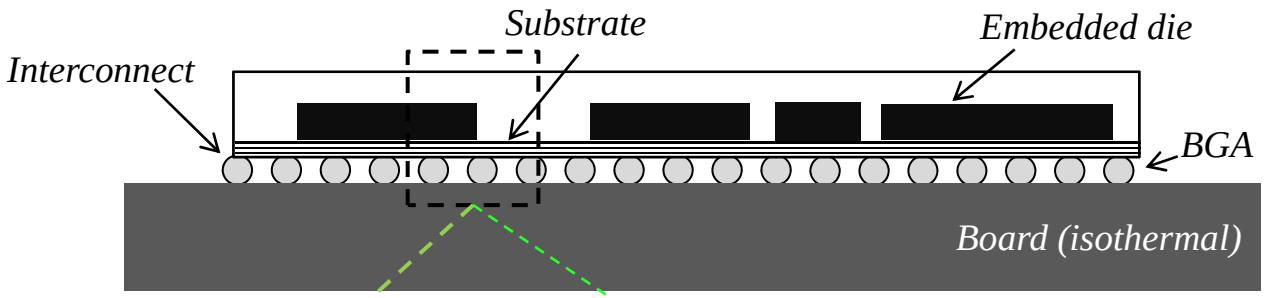
Introduction - Vanishingly Small System (VSS) Concept

- Multi Chip Module – Deposited (MCM-D) ⟹ Multi Chip Module – Integrated (iUHD)

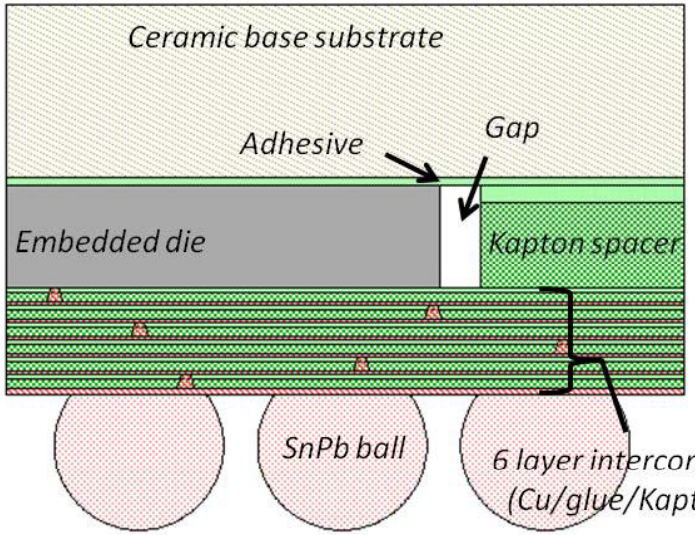


Introduction - Geometric Comparison

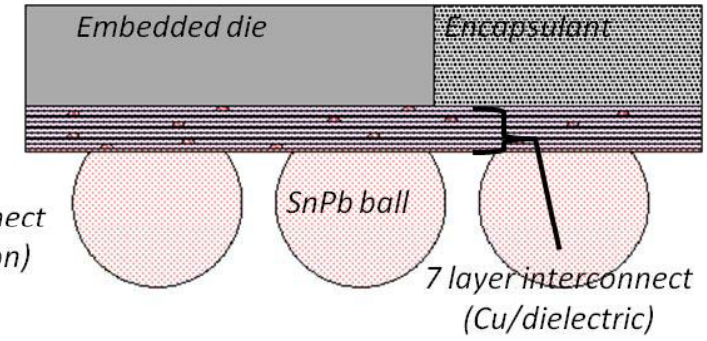
Typical system assembly schematic



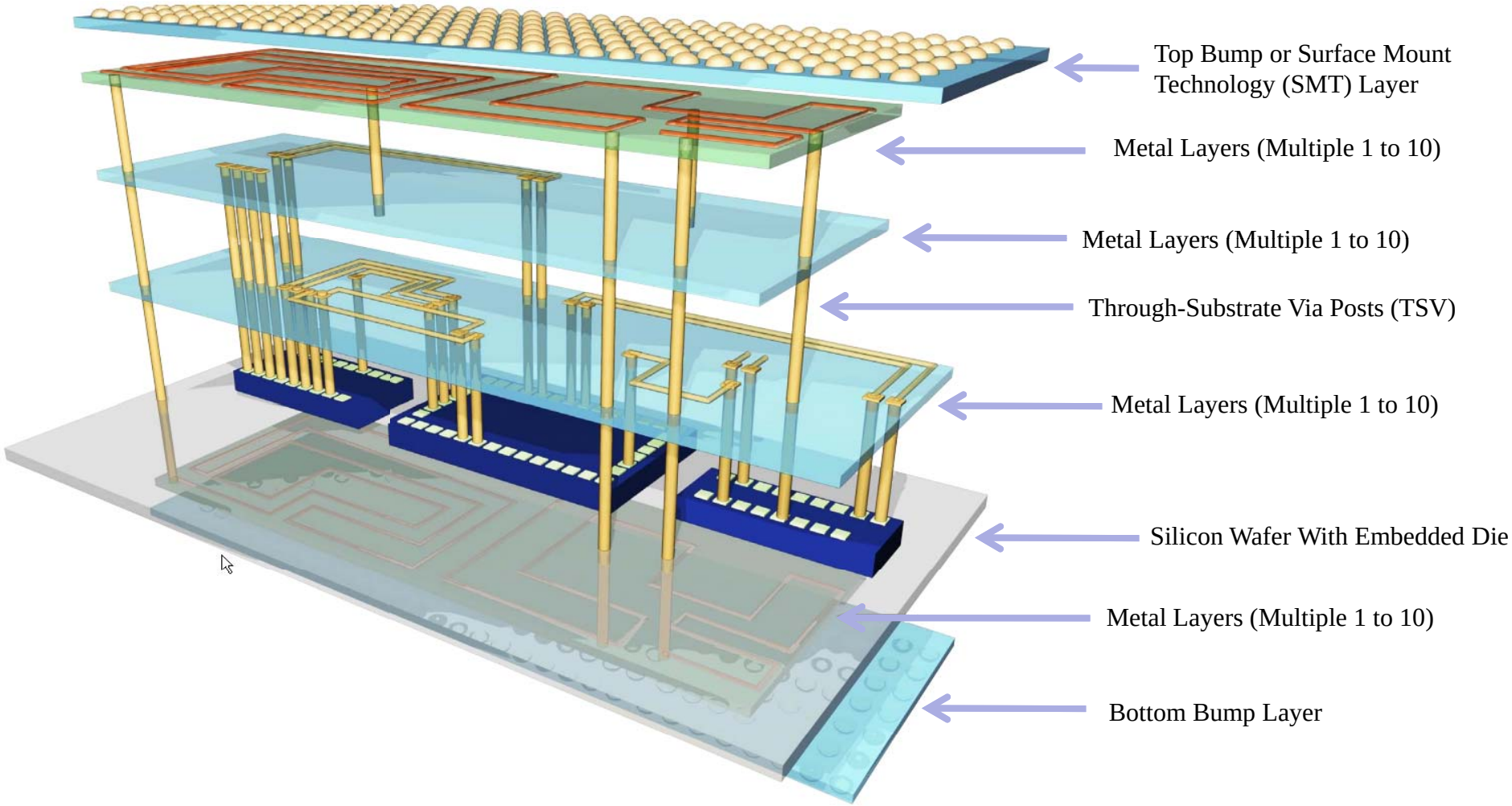
MCM-D



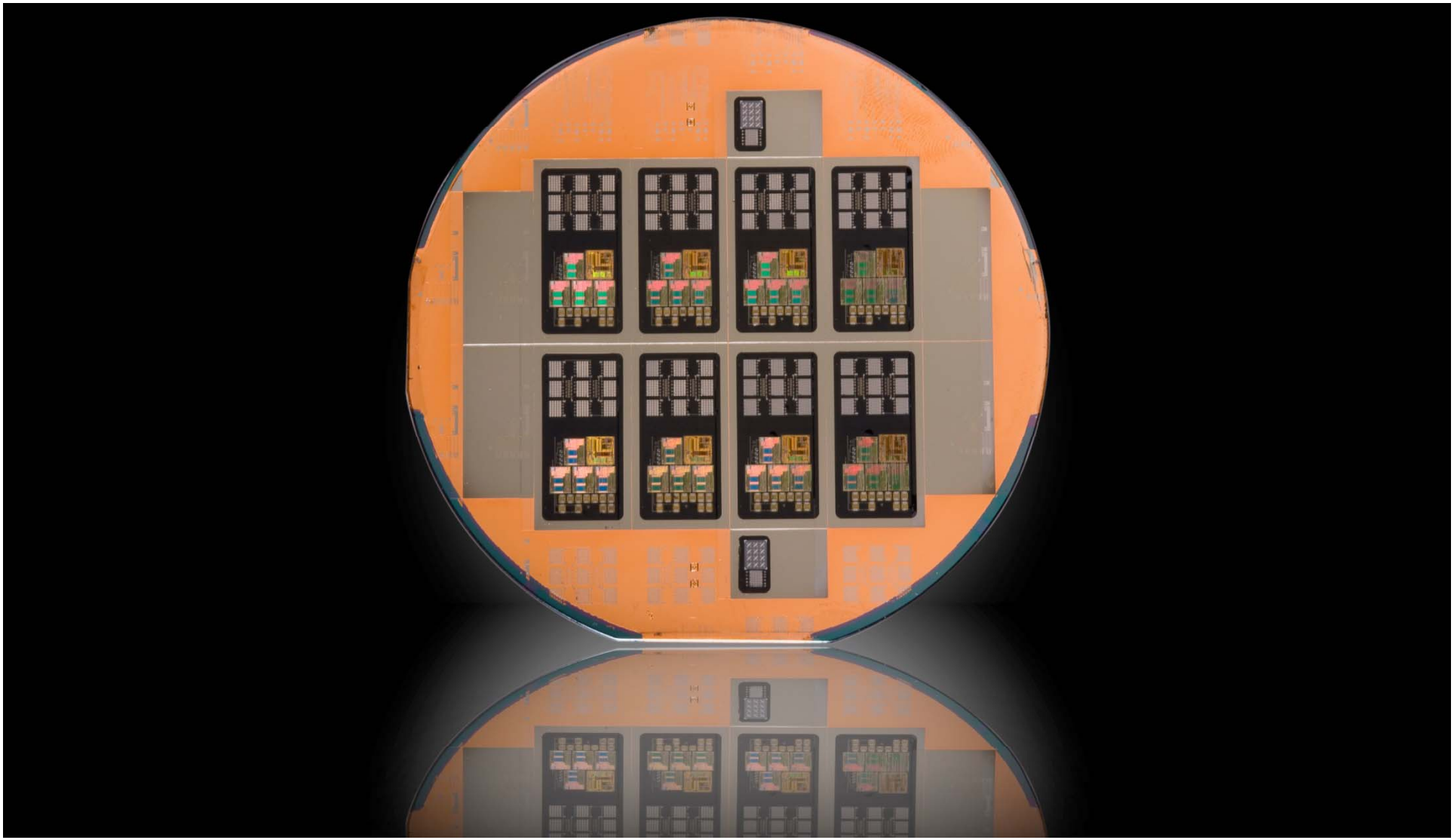
iUHD



I-UHD Module Stack Up



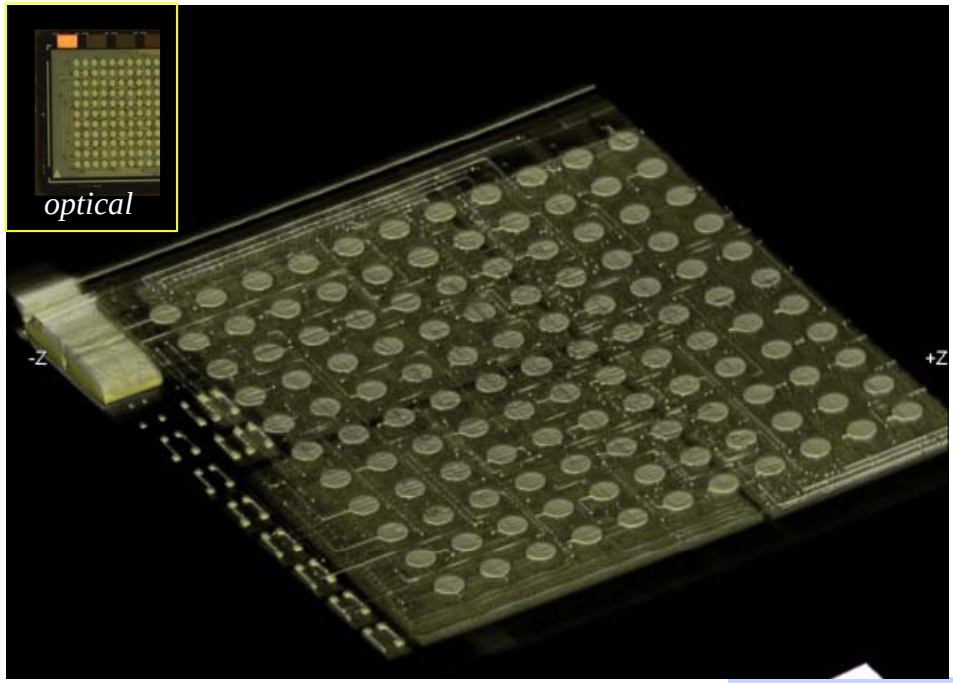
Wafer-based Processing for the iUHD Technology

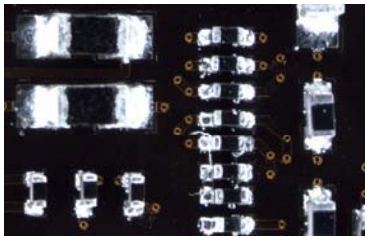


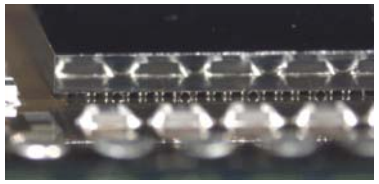
March 27, 2011 **Confidential** Brian J. Lewis

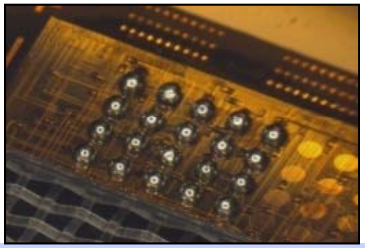
Bottom Line – What is iUHD?

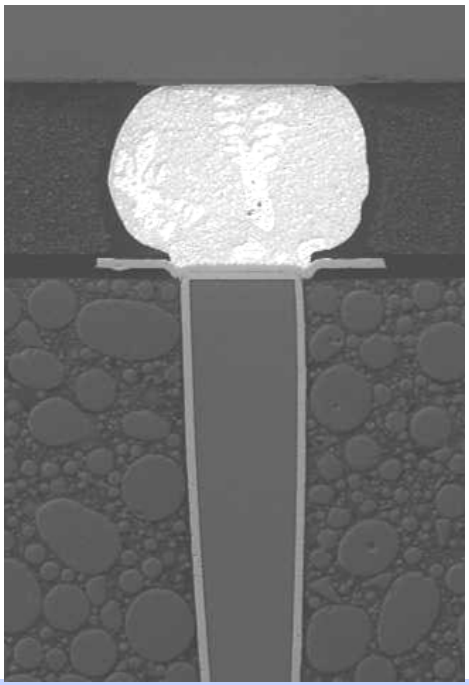
- Embedded active & passive die
- Compatible with SMT and Flip Chip Processing
- Ultra-high density interconnect (<10 um lines/spaces possible)
- Front-to-back interconnect
- Compatible and agnostic with multitude of applications
- More robust than Si-only, more miniature than everything else







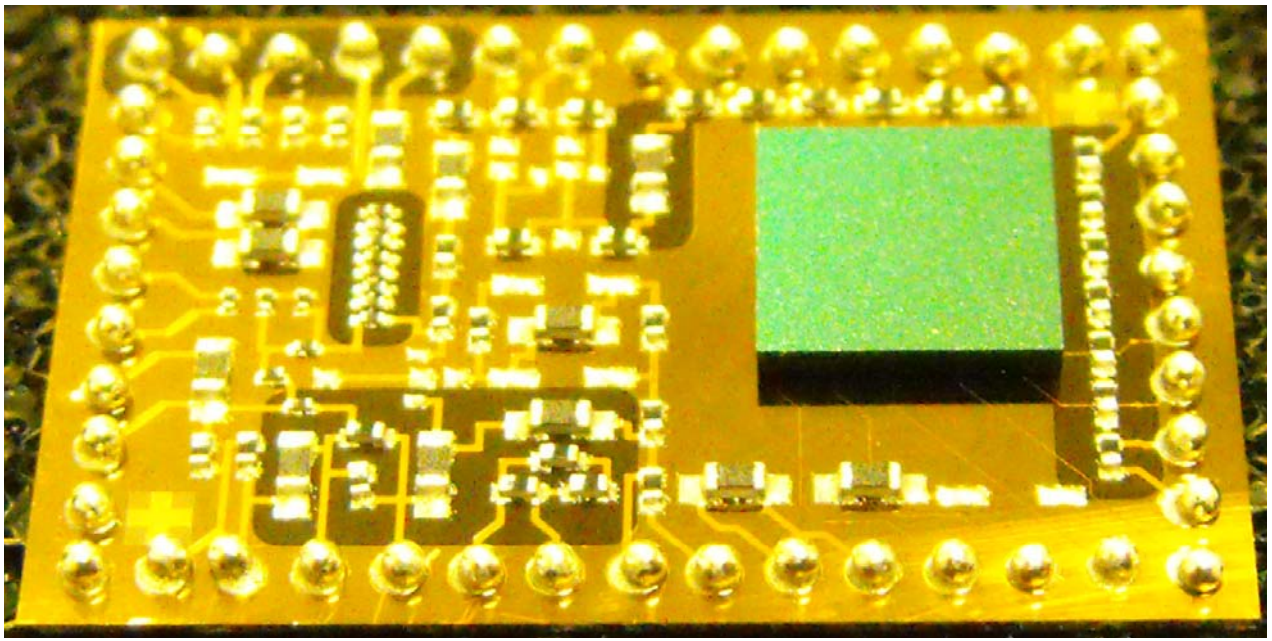




Research Objectives

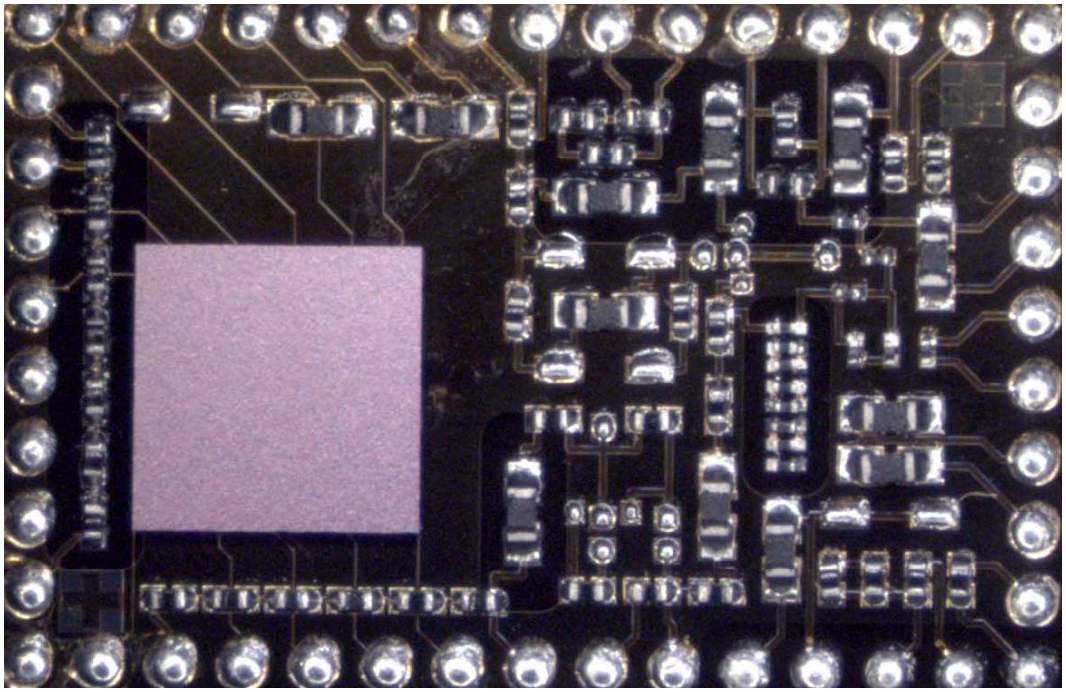
Bluetooth Module iUHD Substrate Used for Processing and Reliability Study

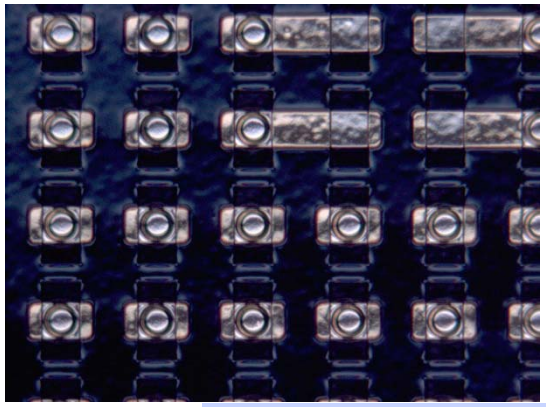
- To characterize the iUHD for processing capability using standard lead free flip chip processing and ultra-small passive processing down to 01005 size
- To do a full reliability assessment on the substrate for MSL, thermal shock and unbiased HAST.
- Characterize shear strengths of the soldered devices and warpage characterization using Moiré analysis



Experimental Results

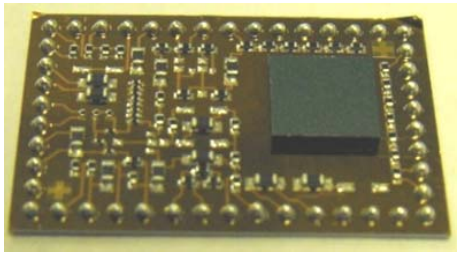
Bluetooth Module design





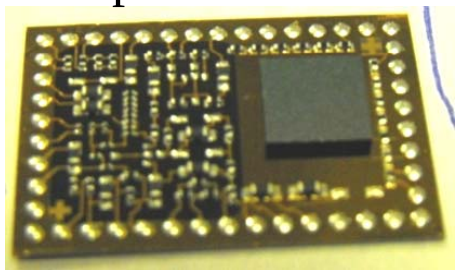
- Substrate contained areas of various passives from 0402 down to 01005
- A 10 mil pitch full area array flip chip
- Design had 7 different patterns of areas with TSV micro-posts embedded in an encapsulate material. Some areas sat over silicon only and some sat over the cavities of encapsulated micro-posts
- Image to the left shows 10 mil spaced TSV posts in the flip chip bond pads

Yield Analysis of Various Layout Structures



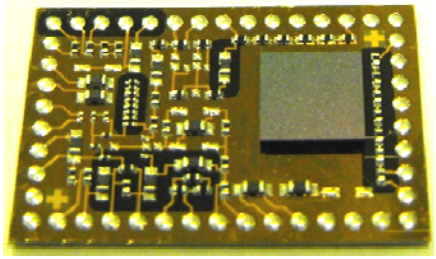
100% yielded

No encapsulate – all silicon top side routing

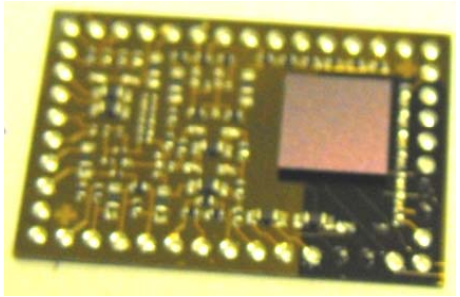


100% yielded

Encapsulate on all passives



Encapsulate under selected passives

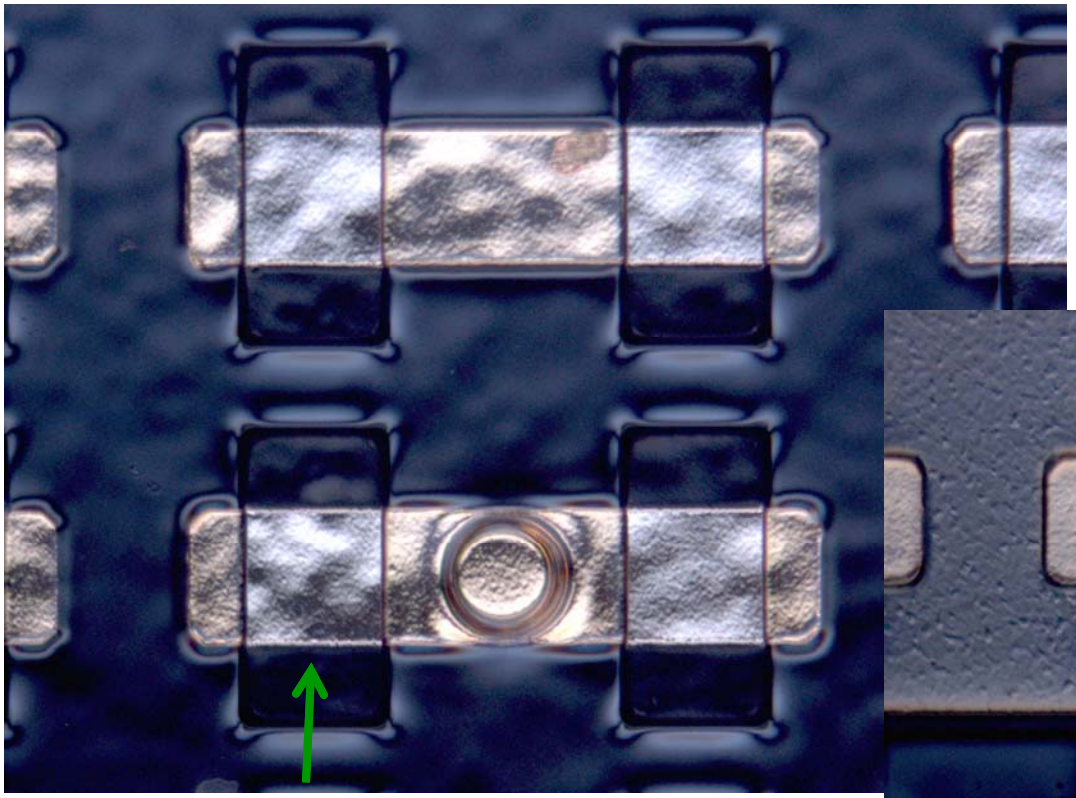


80% yielded

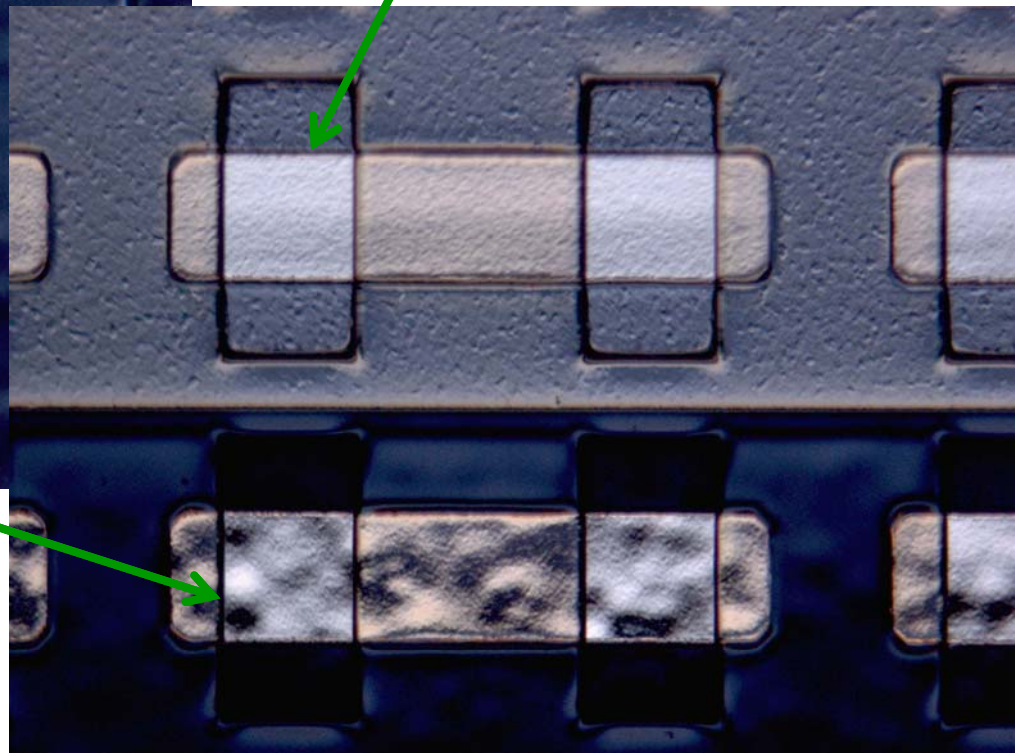
100% yielded

Encapsulate under part of FC

Copper Bond pad topology



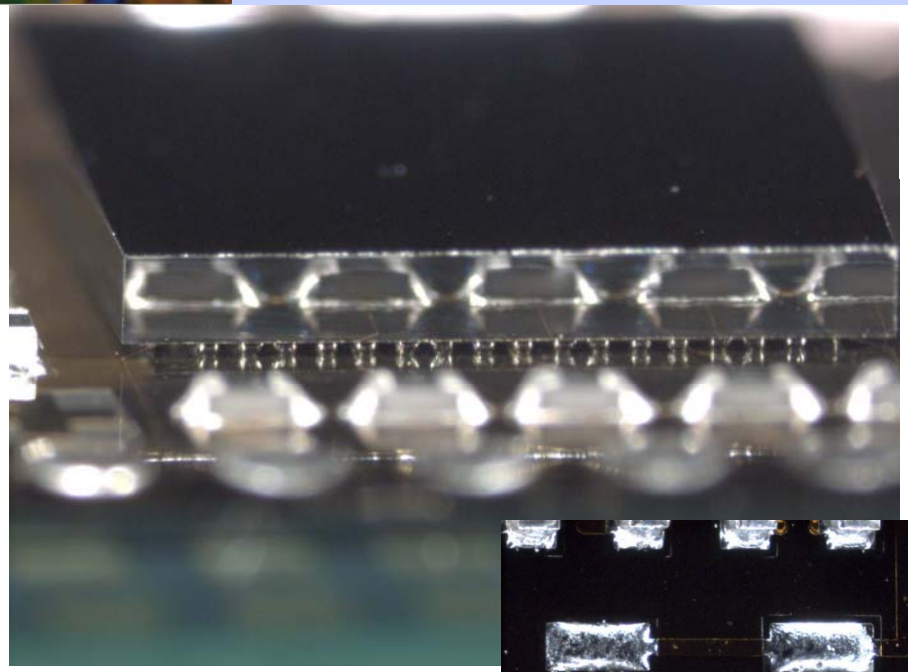
Bond pads over Silicon area

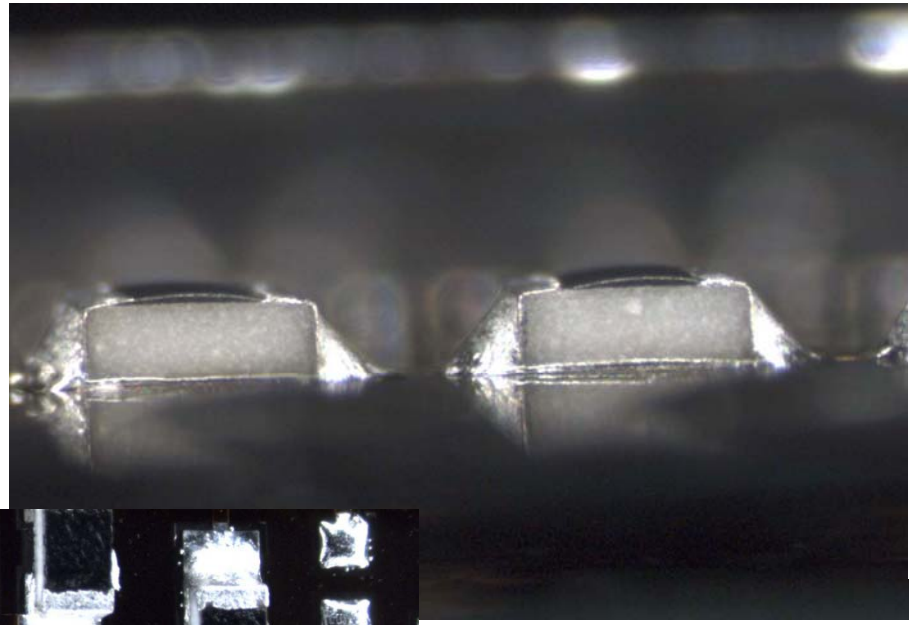


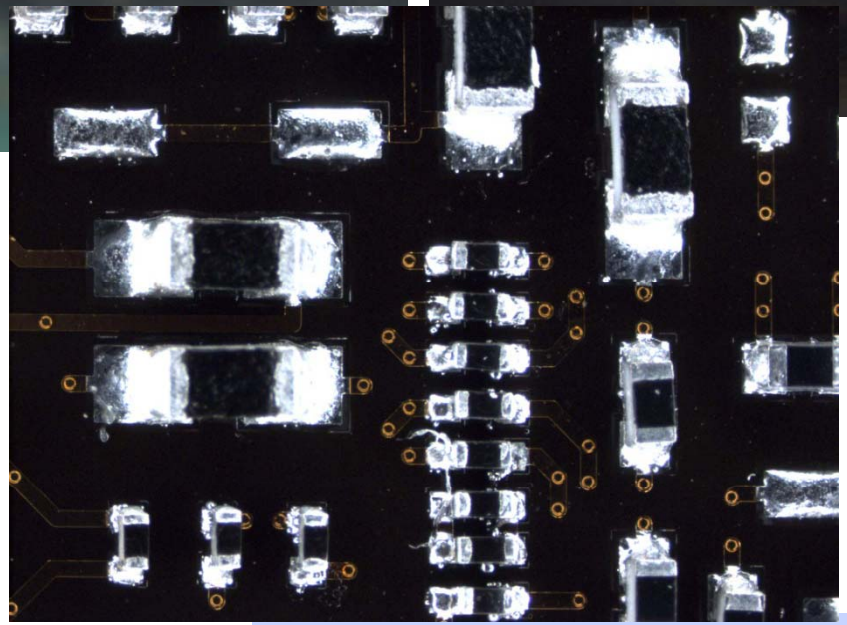
Bond pads over Encapsulated area

Bond pads over both areas are shown in focus, meaning that the heights are close the same.

Optical images of assembled devices





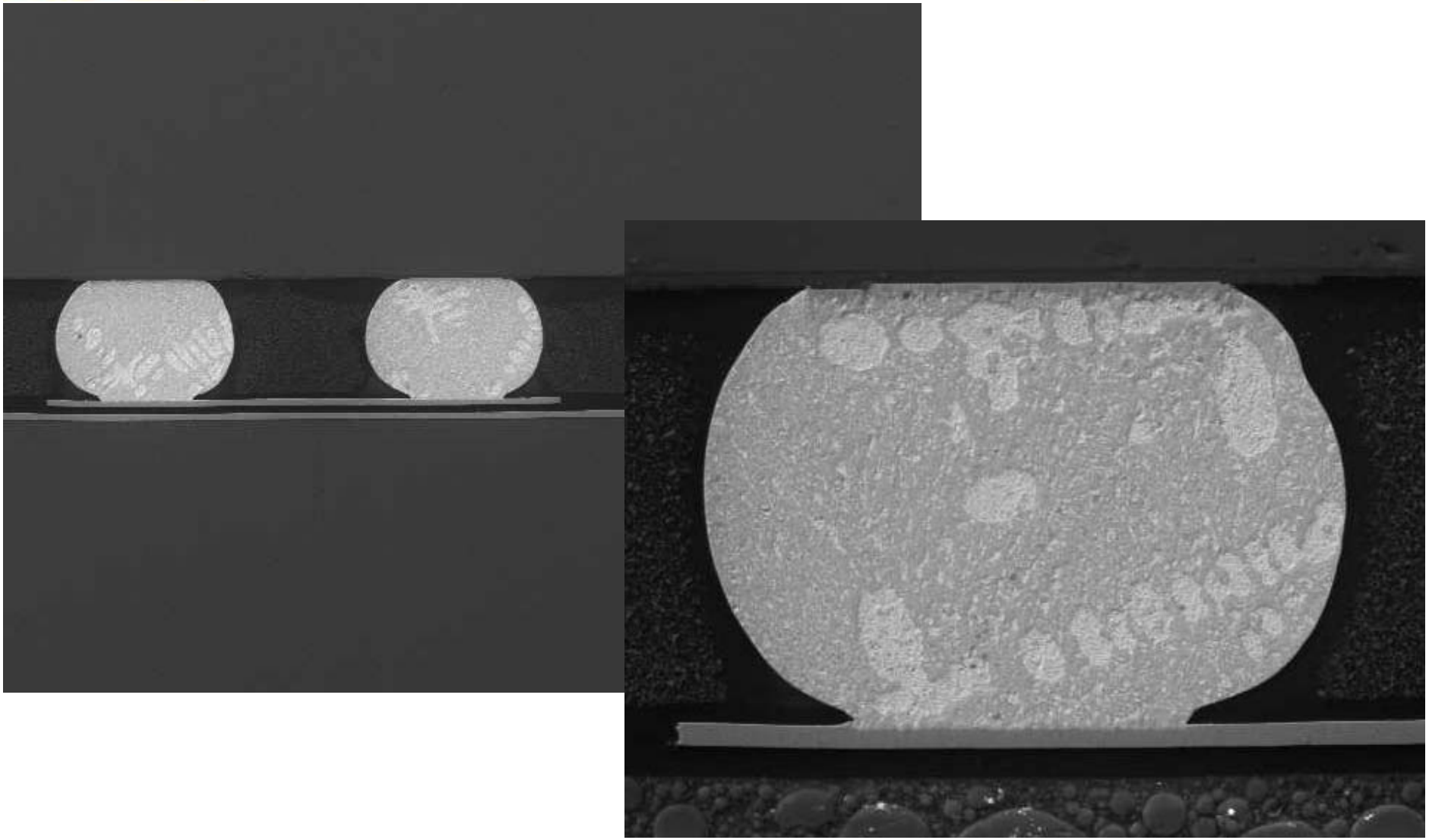


March 27, 2011 **Confidential** Brian J. Lewis

DRAPER LABORATORY

ENGENT
Enabling Next Generation Technologies

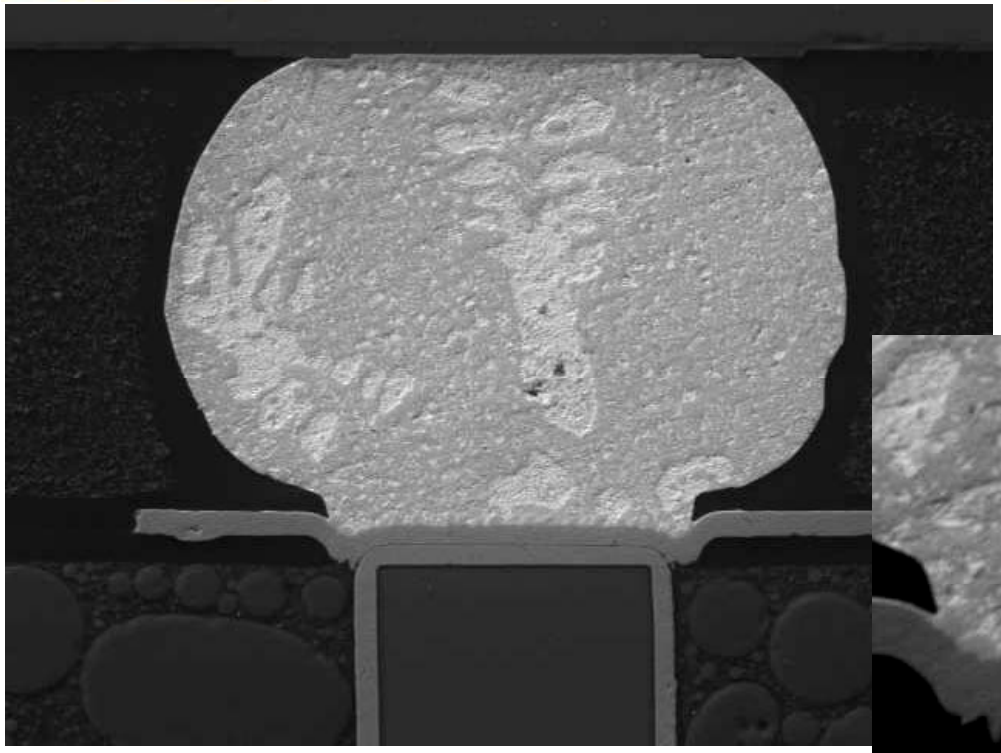
X-section of T(0) units showing flip chip assembly over non encapsulated, silicon-only area

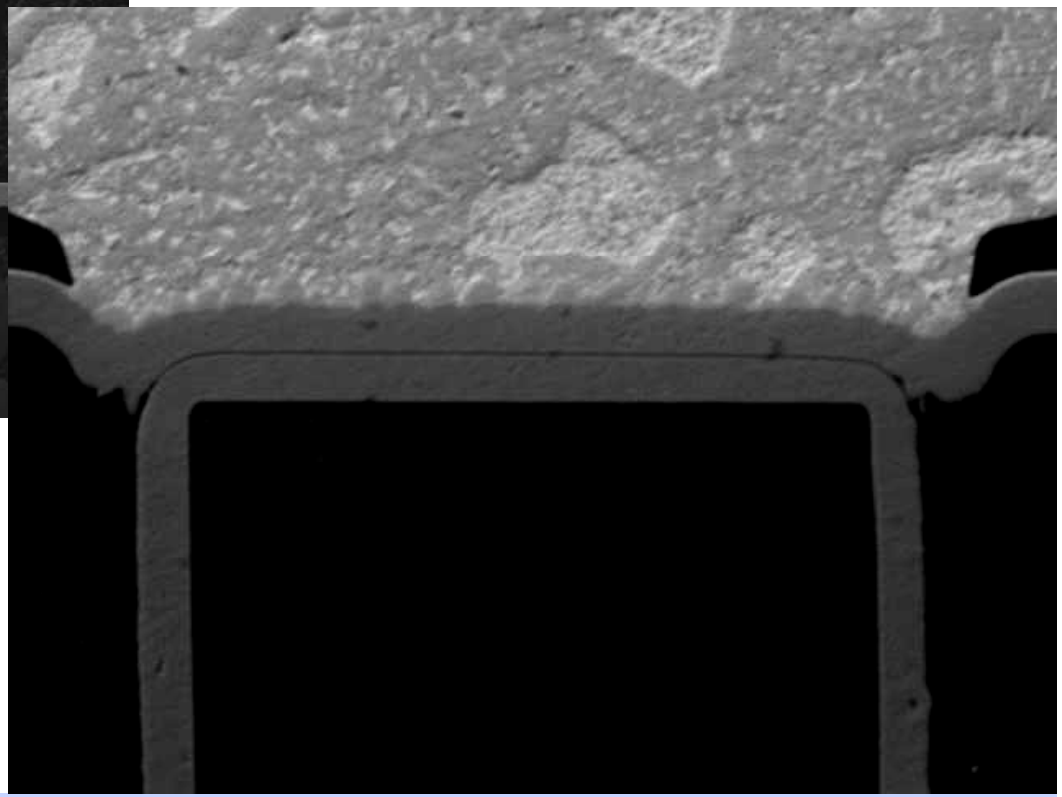


DRAPER LABORATORY

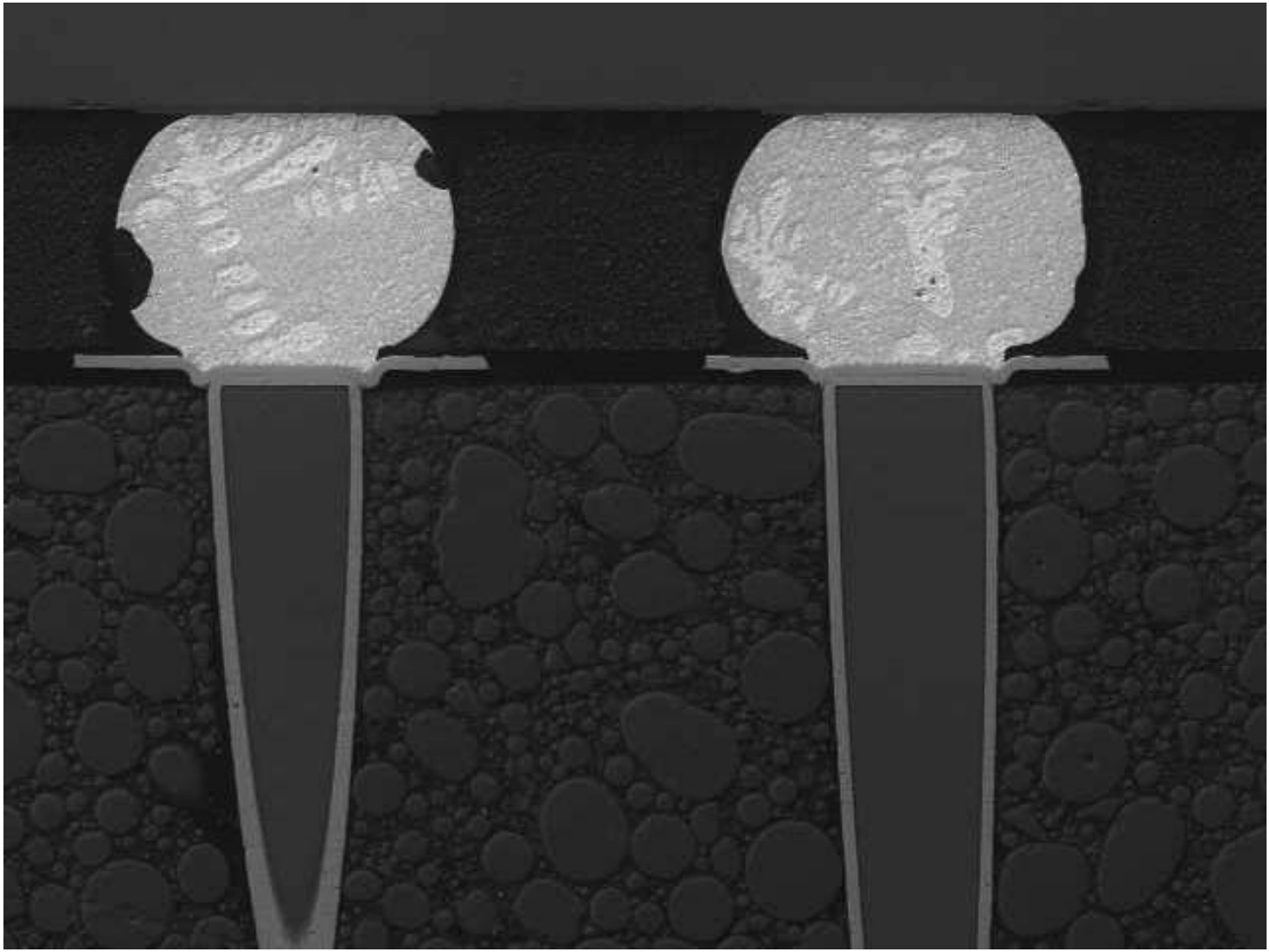
ENGENT Enabling Next Generation Technologies

X-section of T(0) units showing flip chip assembly over encapsulated area and micro post

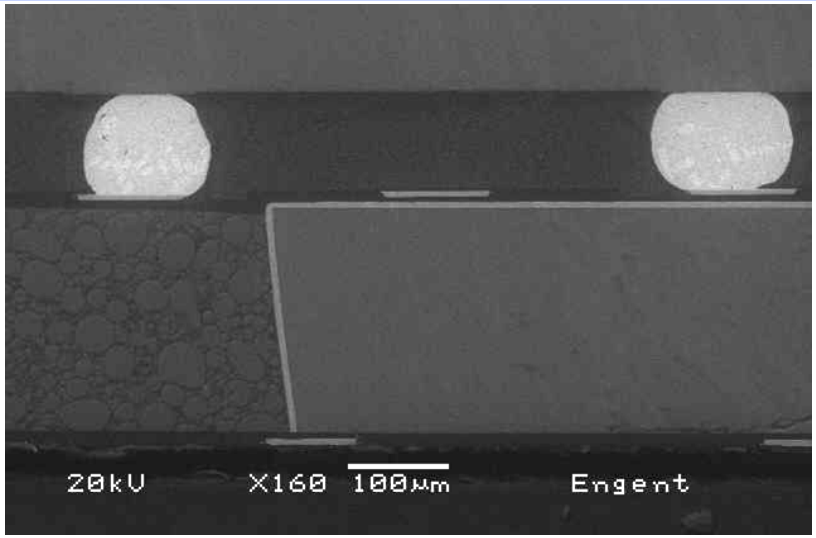


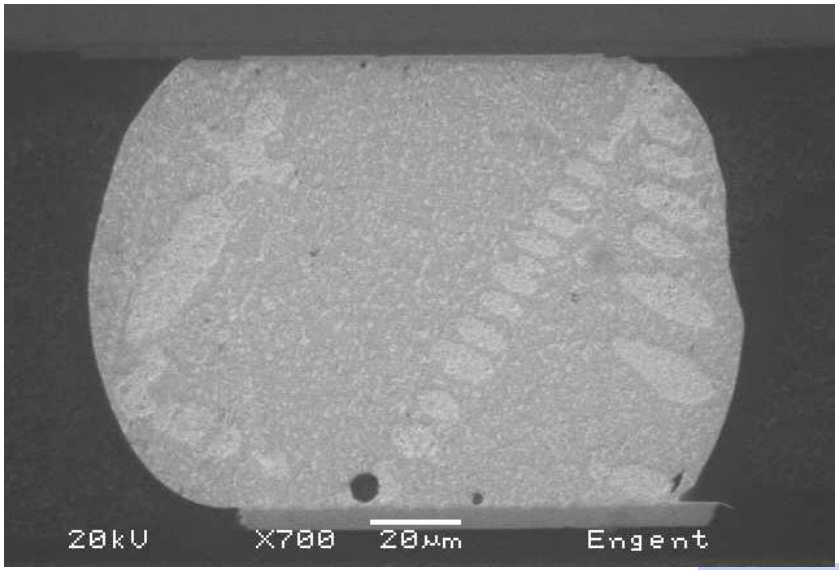


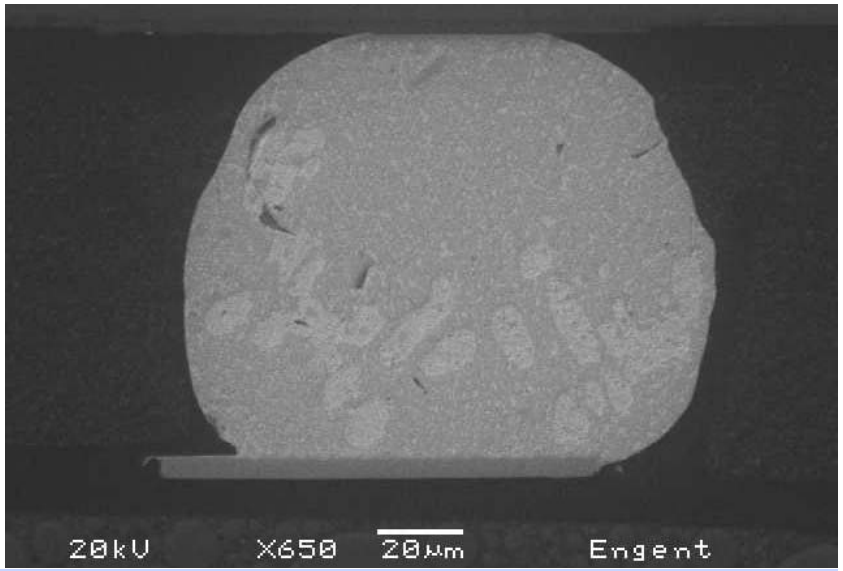
X-section of bumps soldered above two posts



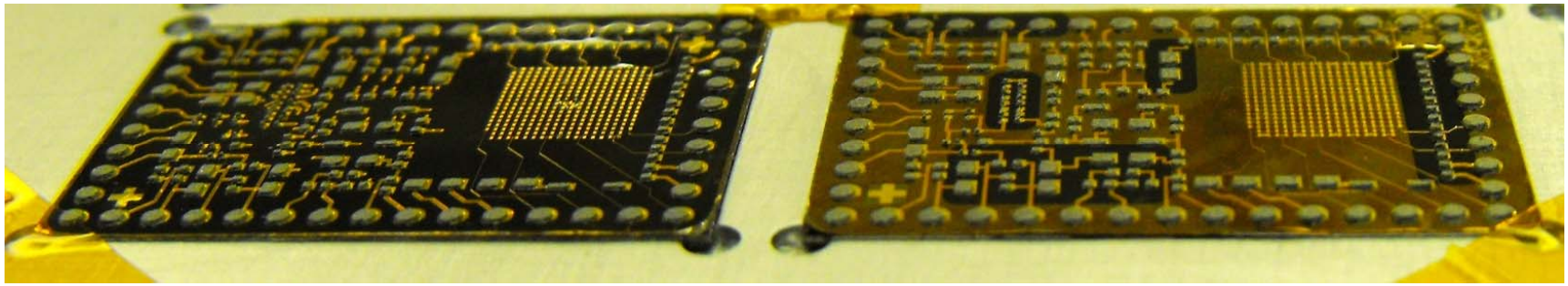
X-section images of flip chip bumps over encapsulated and non-encapsulated locations







Before/After Process Images of Encapsulated and no Encapsulated samples showing level of process related warpage



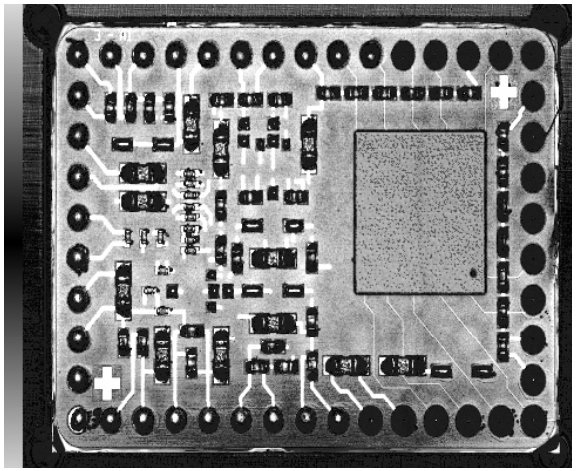
Both Samples before processing shown placed in the fixture. Samples showed little warpage before going through reflow.

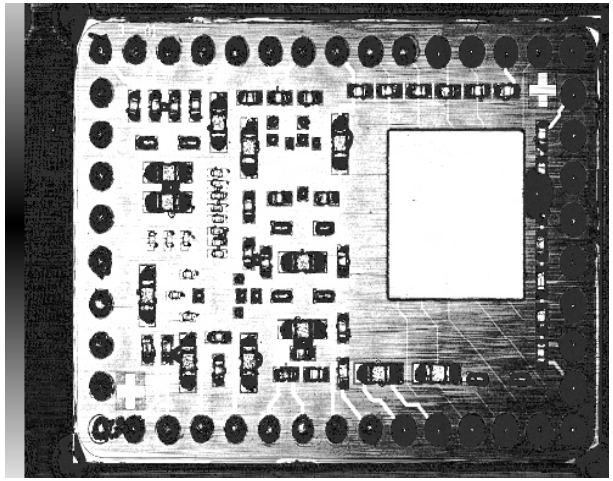
Image above shows same two samples after reflow. Total Encapsulated sample on left showed a high level of warpage, however substrates that had mixed areas of Silicon and Encapsulate areas, on the right, showed very stable warpage results.

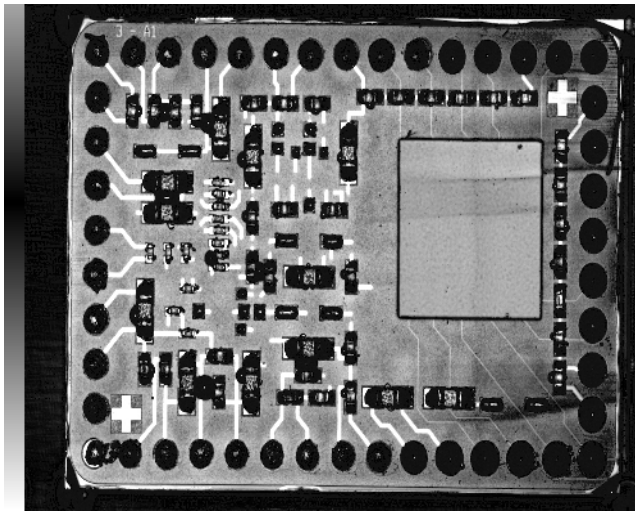
Liquid-Liquid Thermal Shock

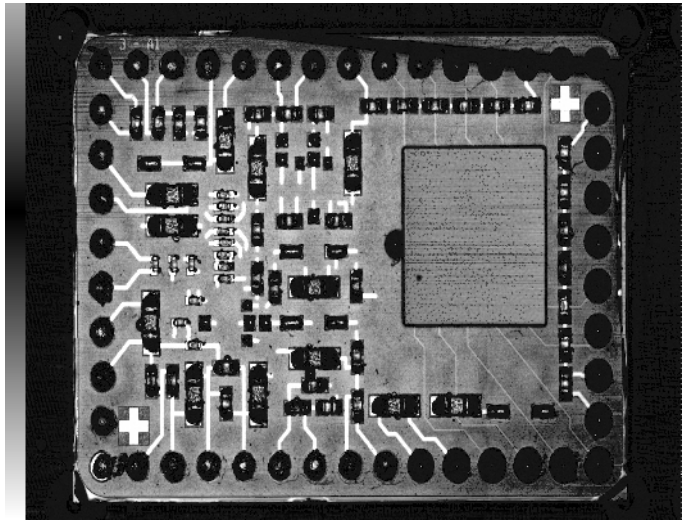
-55C to 125C => 5 minute dwells

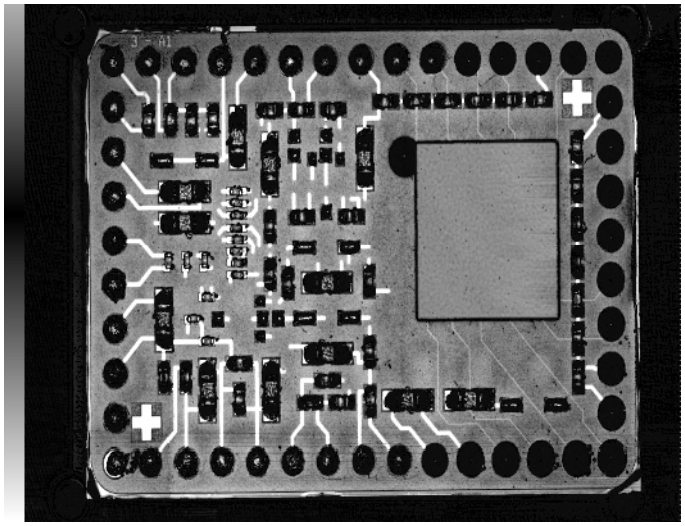
C-SAM Images of Sample 2 from LLTS shown at 0, 250, 500, 750, and 1000 cycles



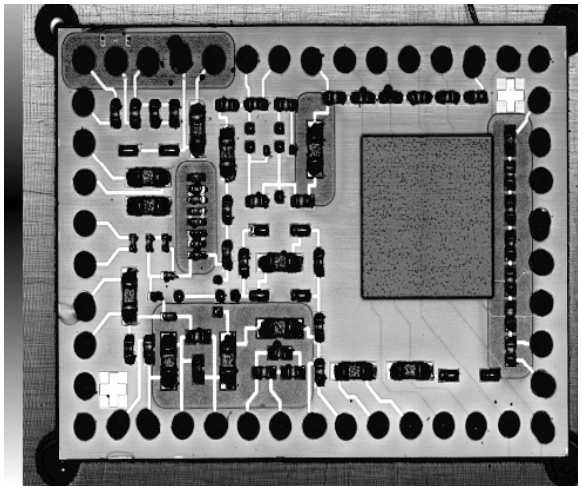


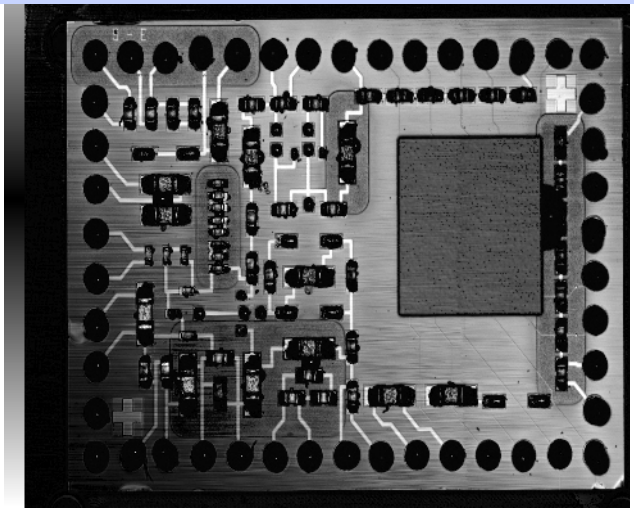


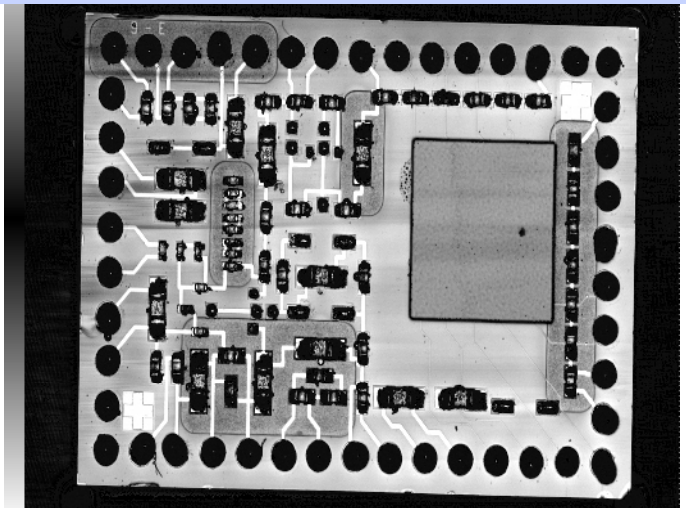


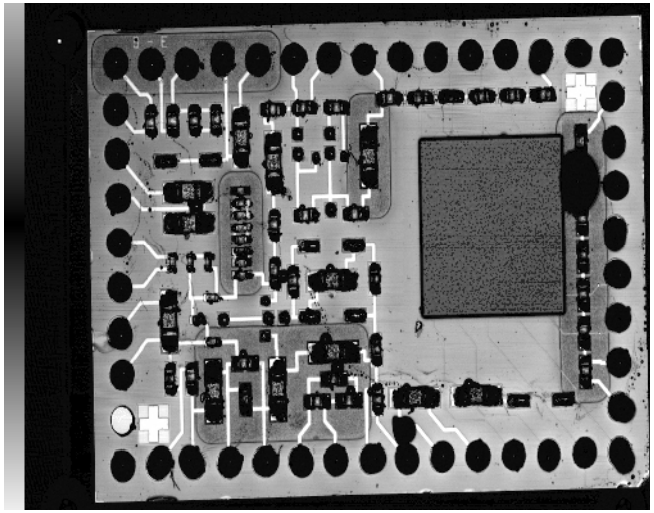


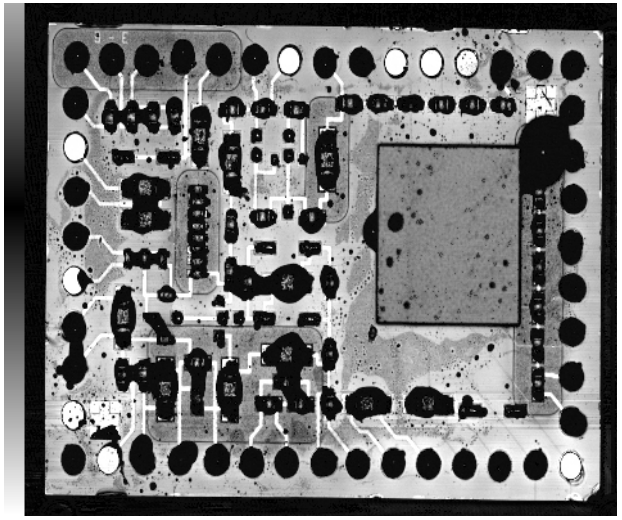
C-SAM Images of Sample 4 from LLTS shown at 0, 250, 500, 750, and 1000 cycles



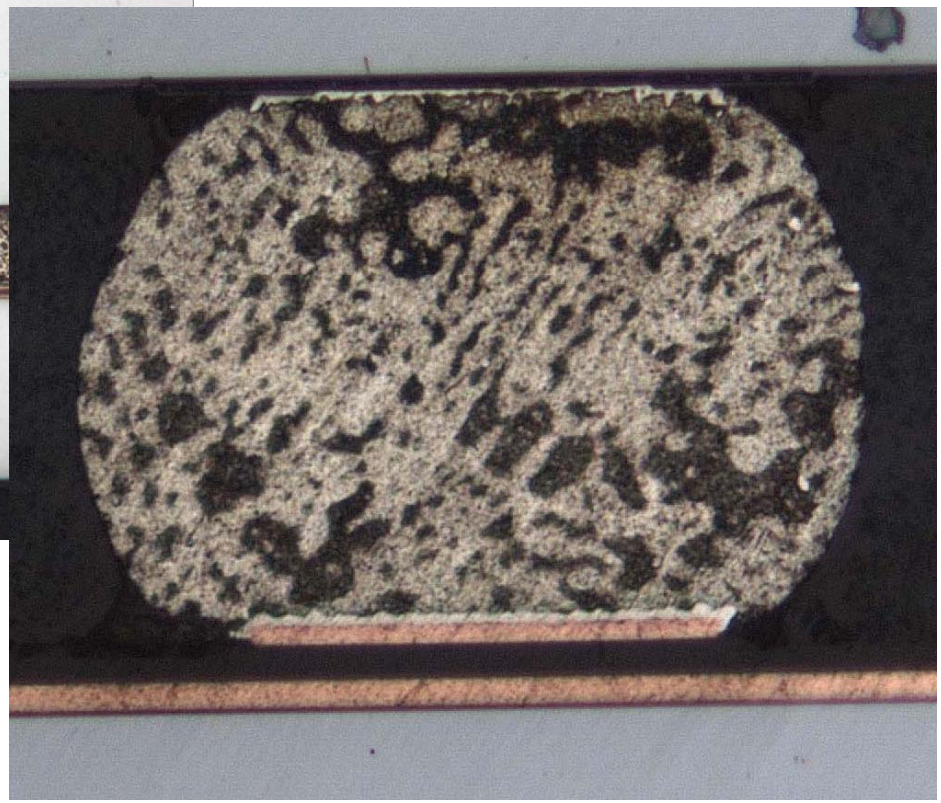








Grain structure coarsening after the 1000 cycle LLTS of Pb/Sn solder units



Shear Testing Analysis

Shear Testing Analysis before and after LLTC cycling (1000 cycles)

Shear Test Data

Encap Sample 1 FC = 8.652				**Non encap** Sample 2 FC = 7.726				**Encap** Sample 3 FC = 10.167				Same design **Organic** Sample 1			
Balls	0402	0201	01005	Balls	0402	0201	01005	Balls	0402	0201	01005	Balls	0402	0201	01005
1.664	0.79	0.399	0.124		1.27	0.547	0.31		1.73	0.385	0.187		0.896	0.525	
2.09	2.22	0.394	0.214		1.2	0.615	0.239		2.43	0.459	0.223		1.03	0.531	
1.91	1.85	0.214	0.214		1.1	0.66	0.198		1.05	0.41	0.268		0.95	0.57	
1.84	1.56	0.664	0.122		1.55	0.57	0.133		1.3	0.525	0.354		1.05	0.426	
1.67	1.01	0.946	0.142		1.45	0.534			1.35	1.01	0.534		0.921	0.545	
1.8	1.48	0.685	0.185		1.46	0.736			1.29	0.721	0.261		1.04	0.526	
	1.19	0.475			1.38	0.723			0.559	1.04			0.901		
	1.41	1.01			1.39	0.466			1.51	0.721			0.779		
	2.12	0.613			1.53	0.613			1.1	1.04			0.879		
	1.03	0.54				0.56			1.18	0.734					
		0.633								0.573					
1.829	**1.466**	**0.5975**	**0.1668**		**1.37**	**0.6024**	**0.22**		**1.3499**	**0.6925**	**0.3045**		**0.9384**	**0.5205**	

T(0) shear values for passives and FC in Silicon based and Encapsulated based areas showed very similar results

non encap 1000 cycles - FC = 8.438				**Encap** 1000 cycles FC = 9.501			
Balls	0402	0201	01005	Balls	0402	0201	01005
0.412	0.619	0.297	0.214	1.934	1.777	0.634	0.213
0.169	0.536	0.221	0.225	1.416	1.284	0.536	0.171
0.305	0.547	0.232	0.214	2.078	1.54	0.484	0.173
	0.54	0.268		2.06	1.317	0.383	
	0.54	0.144				0.421	
		0.243				0.466	
		0.261					
		0.194					
0.2953	**0.5564**	**0.2325**	**0.2177**	**1.872**	**1.4795**	**0.4873**	**0.1857**

T(1000 cycles) shear values for passives and FC in Silicon based and Encapsulated based areas with Encapsulated areas showing no obvious reduction of shear force

T(0) Flip Chip Failure mode after shear in Silicon only area

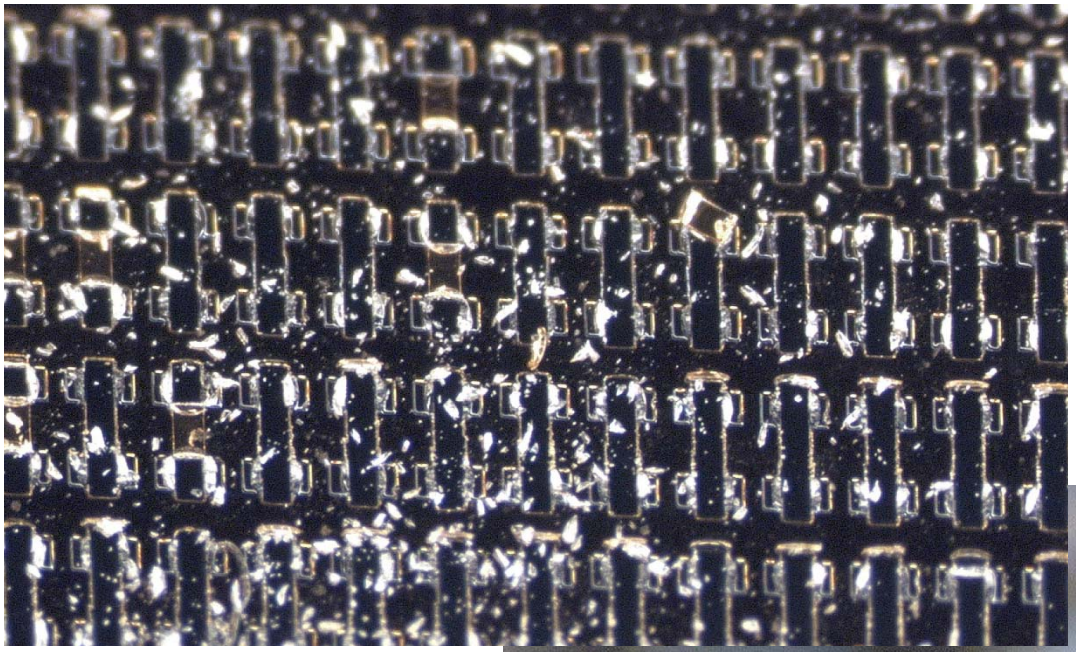
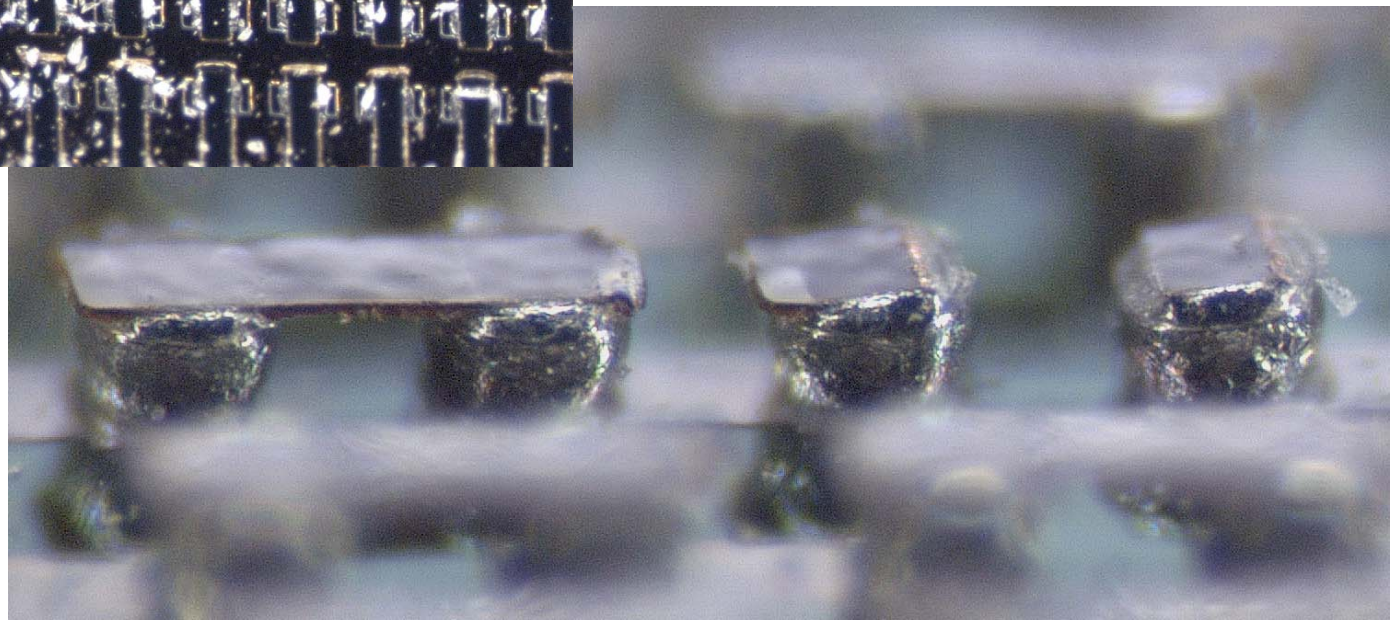
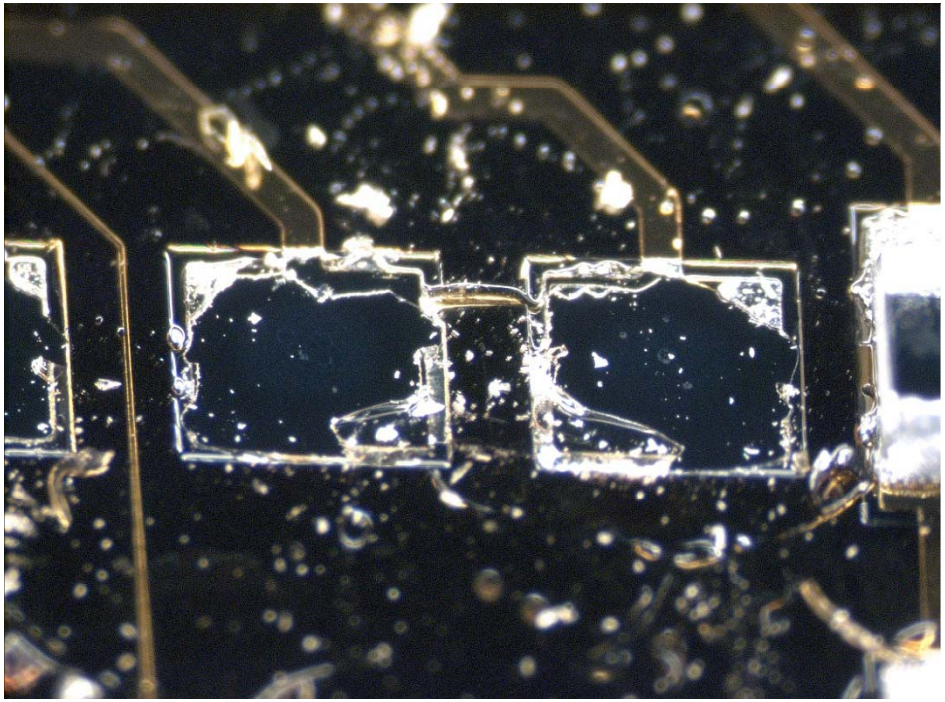


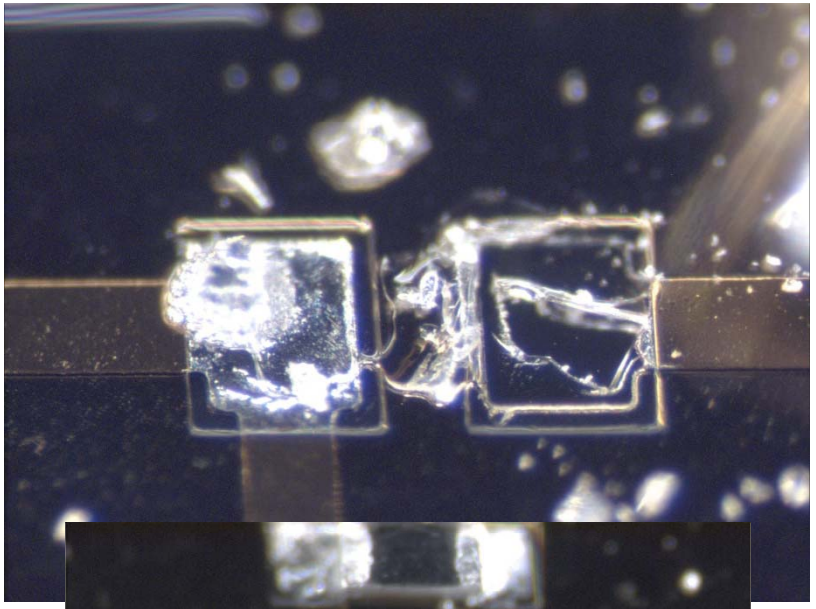
Image of the Draper substrate with all top metal pulled out

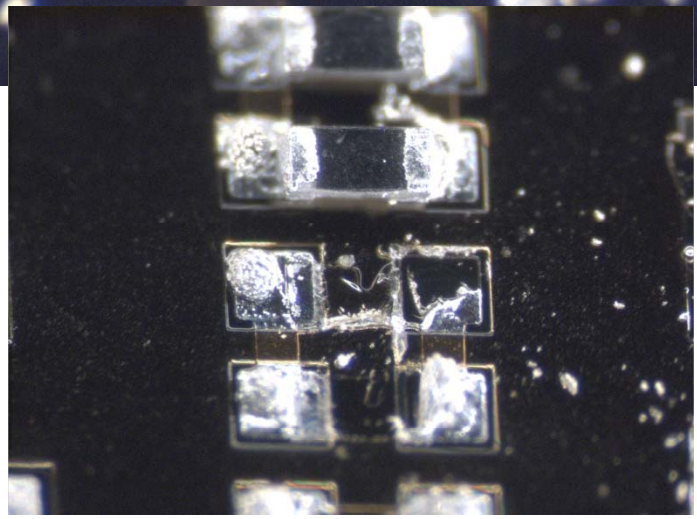


Bumps shown on chip with Draper substrate metal still attached to solder

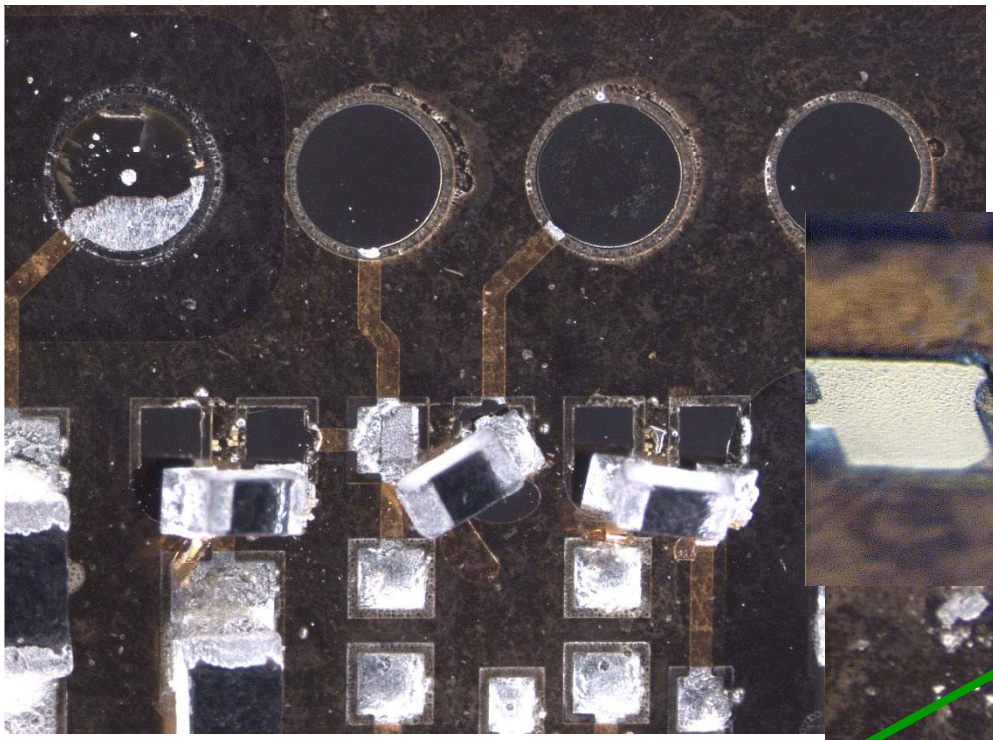
T(0) Shear test failure modes for larger passives over silicon only area

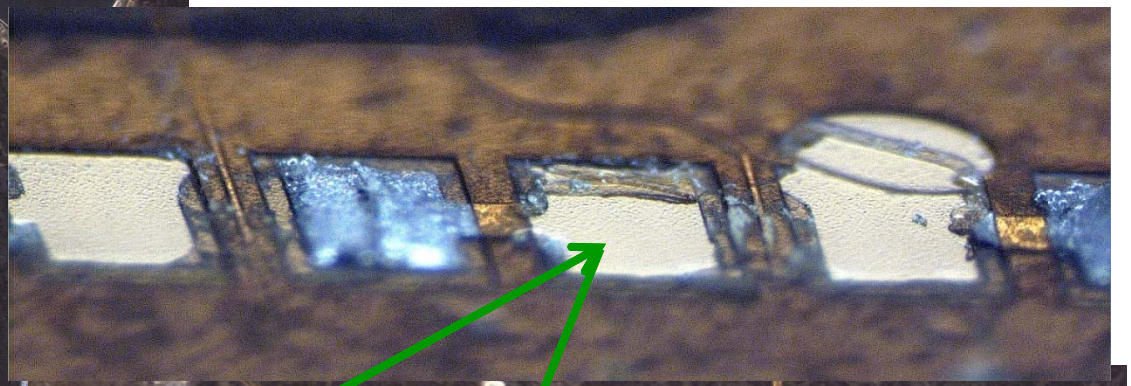


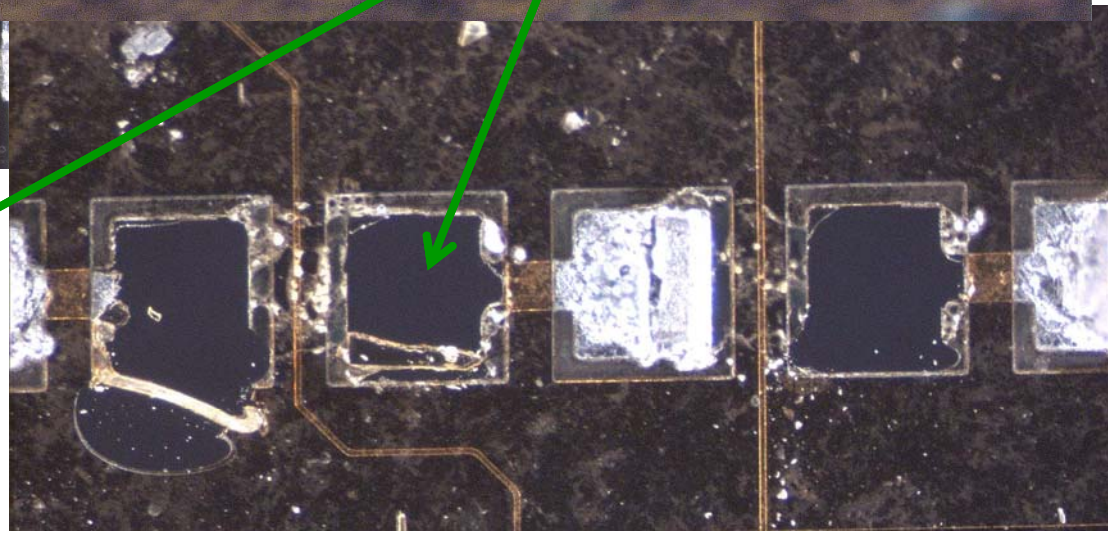




Shear results after 1000 cycles LTS on Silicon substrate

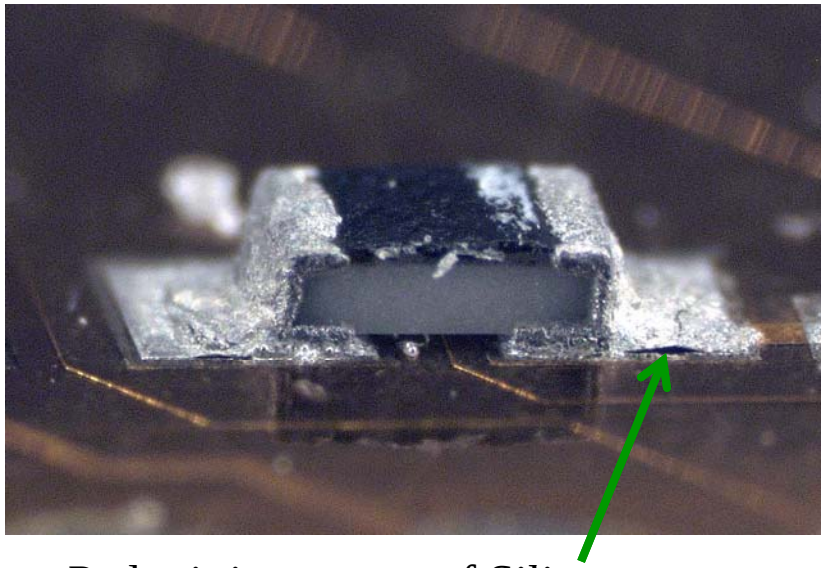




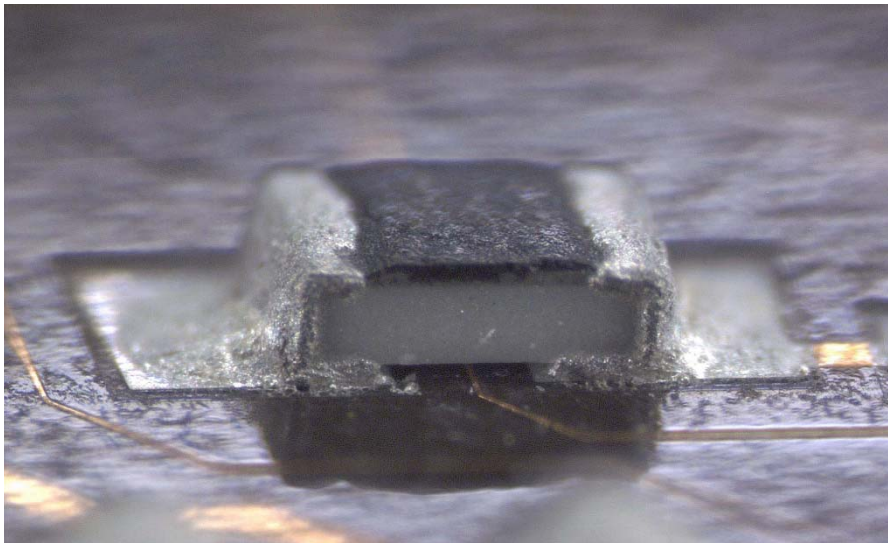


Side optical view appears that all material released from bare silicon layer

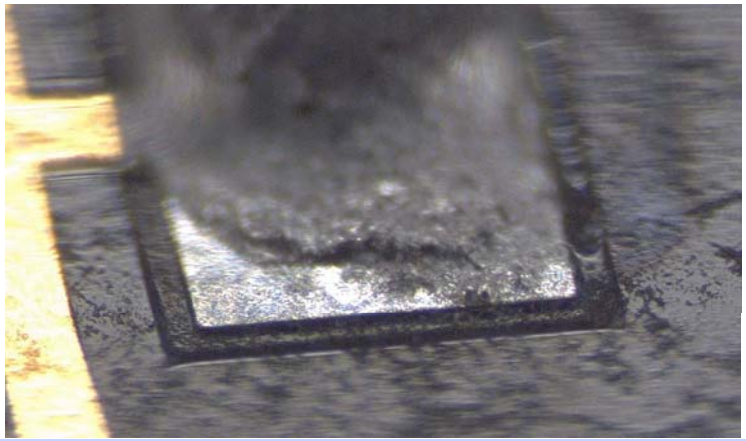
Pad effects after 1000 cycles of LLTS in both types of areas



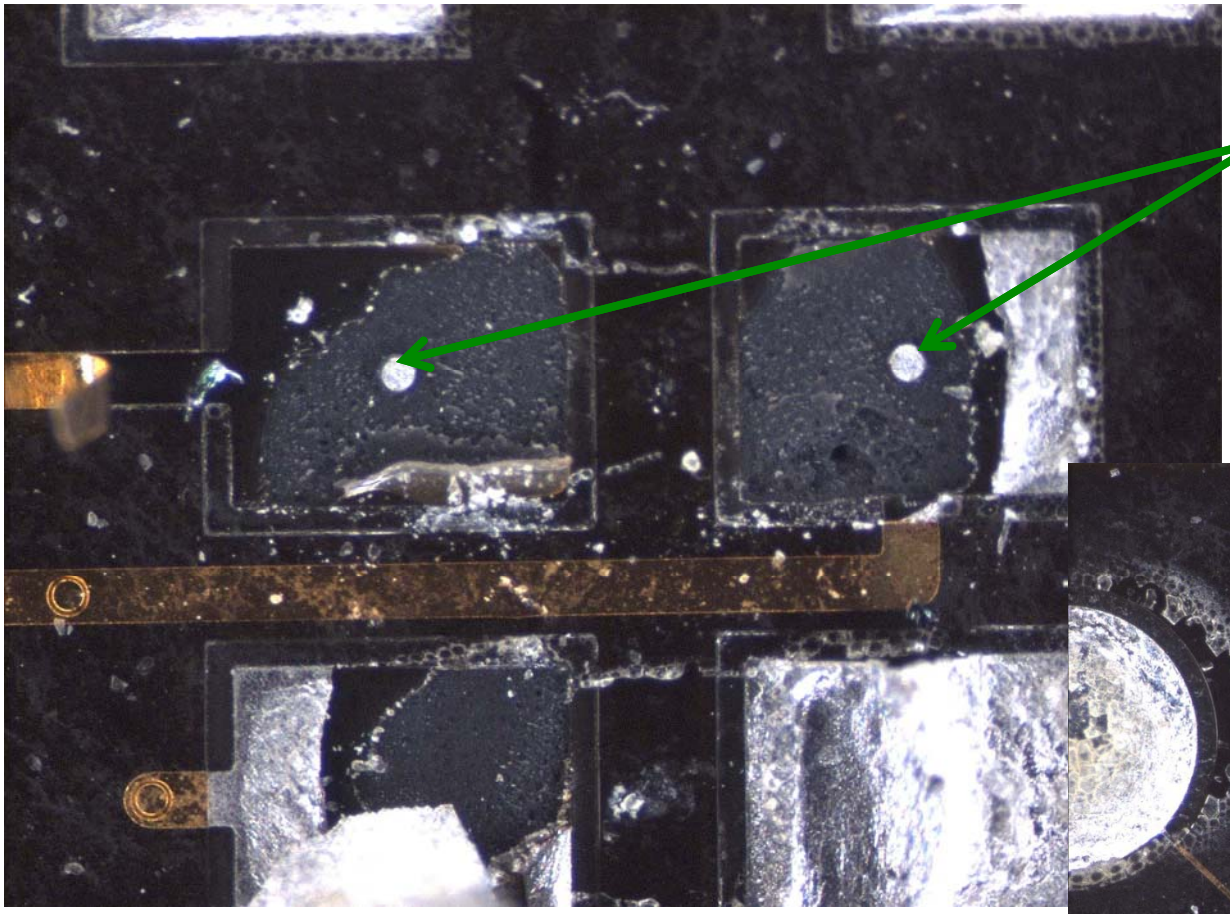
Pads sitting on top of Silicon start to show signs of delamination



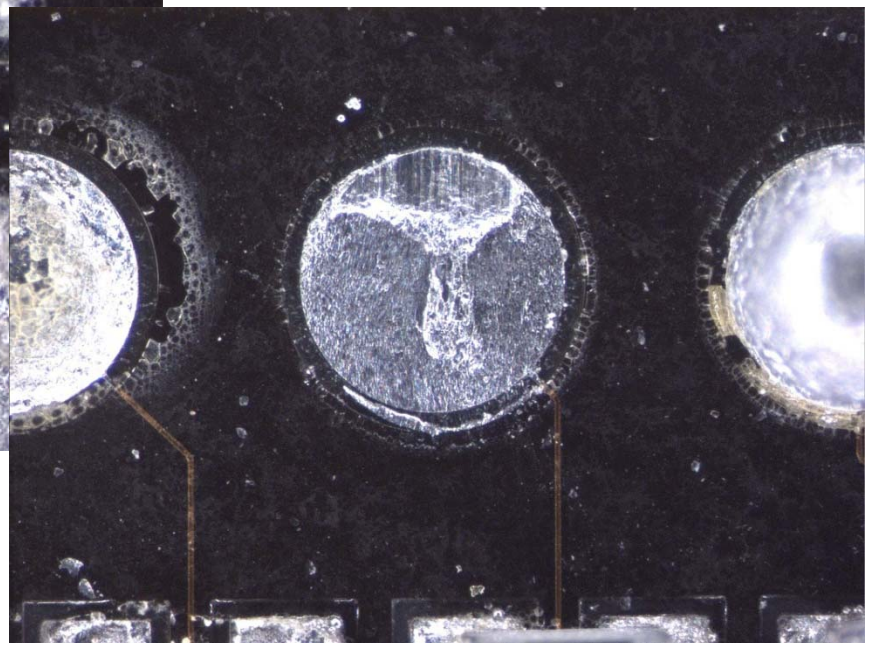
Pads sitting on top of Encapsulant **do not show** the peeling edges



Shear results on an Encapsulated area after 1000 cycles show good adhesion of the pad to polymer



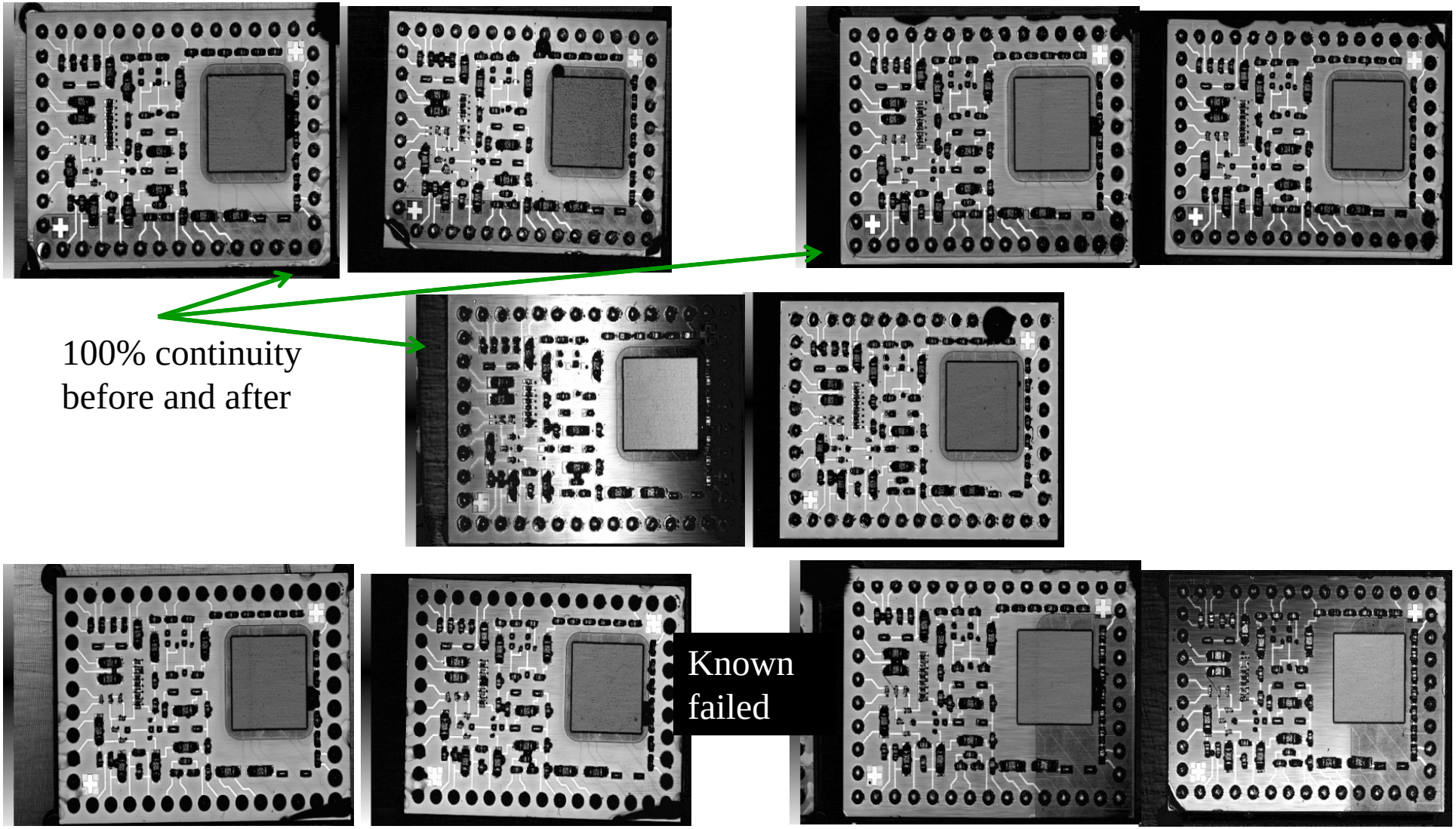
Micro-TSV-posts under the bond pads in the encapsulated areas



Moisture Sensitivity Level Testing – Level 1

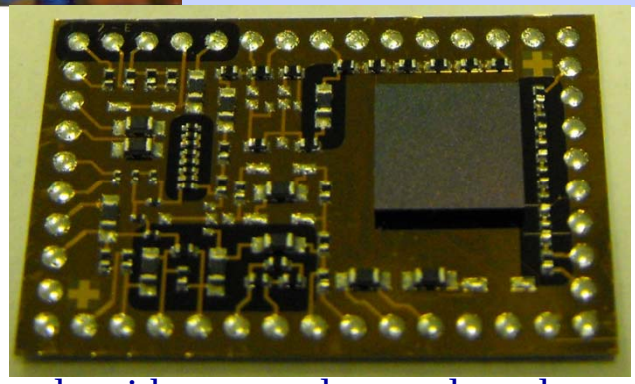
85C/85% RMH then three subsequent reflows peaking at 260C

5 sample Pre and post MSL level 1 testing – no obvious changes seen



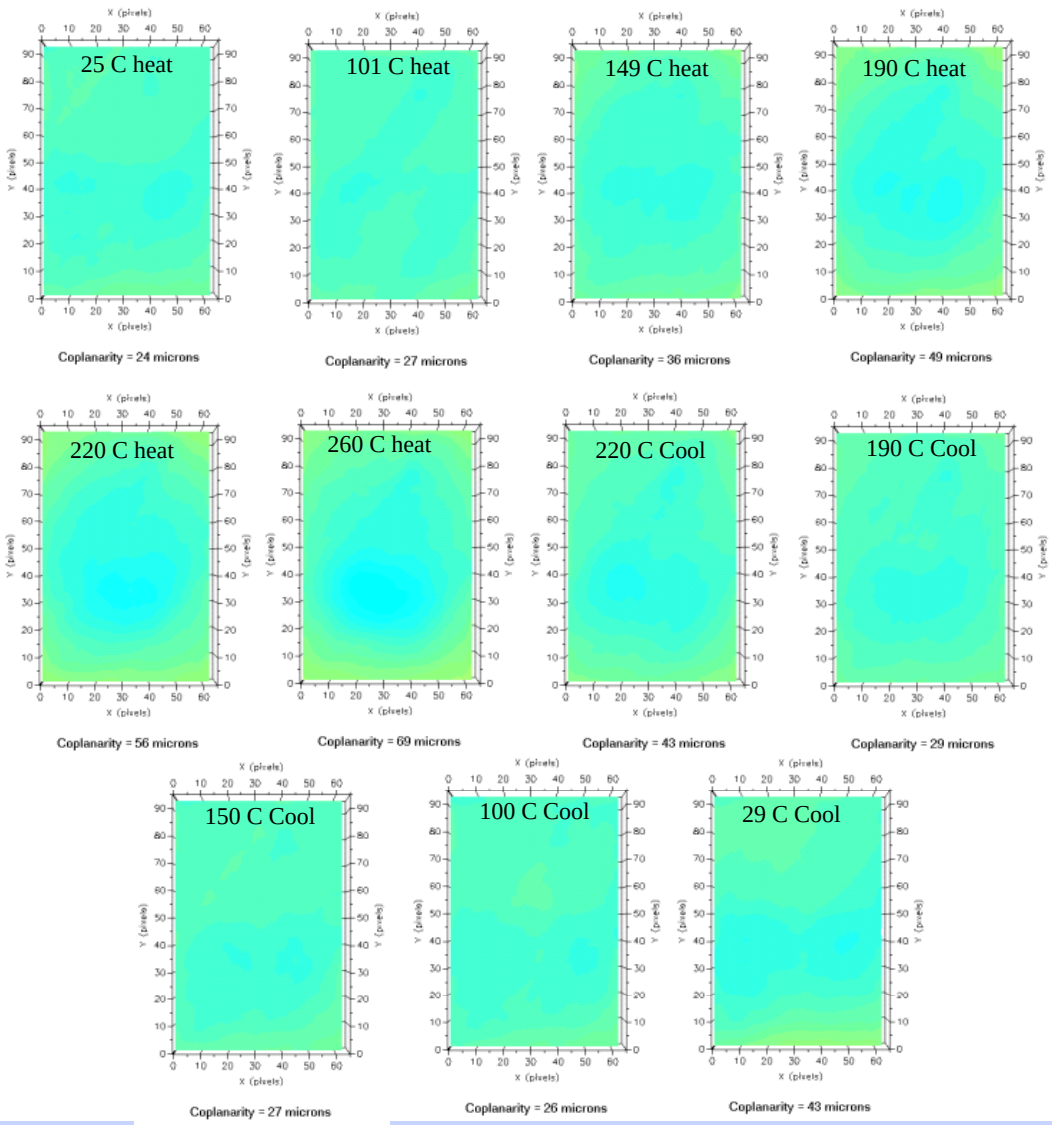
Thermoire Analysis

Sample 1 Thermoire Analysis – Maximum 69 micron warpage

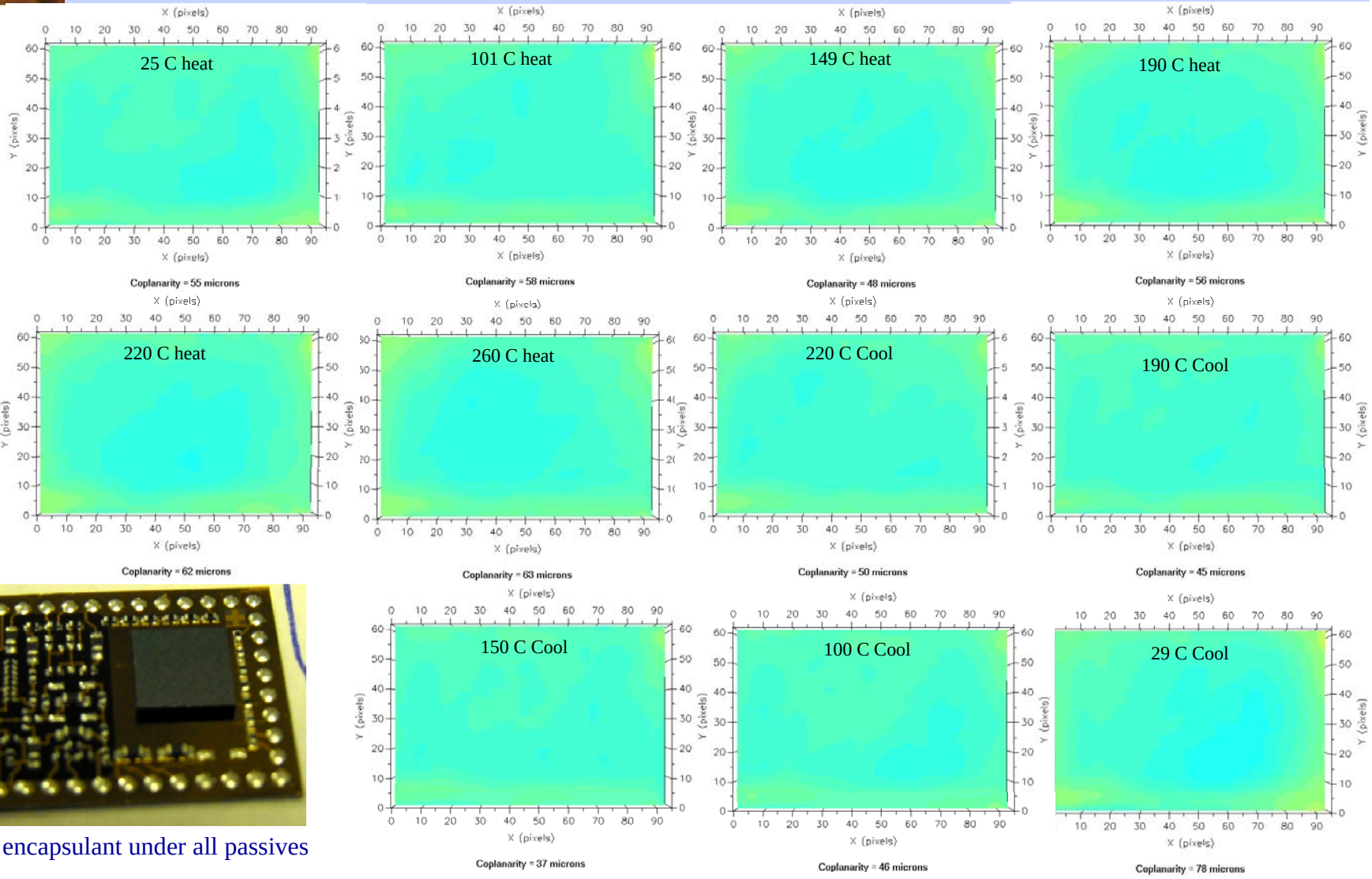


Sample with encapsulant under select passives

Three samples were run through a lead free profile using a Thermoire analysis system. These two slide show the warpage profile across this heat range at critical points through the heating and cooling curves. Overall, the warpage was quite low on these samples. Additional samples should be run to understand their behavior.



Sample 2 Thermoire Analysis – Maximum 78 micron warpage



Sample with encapsulant under all passives

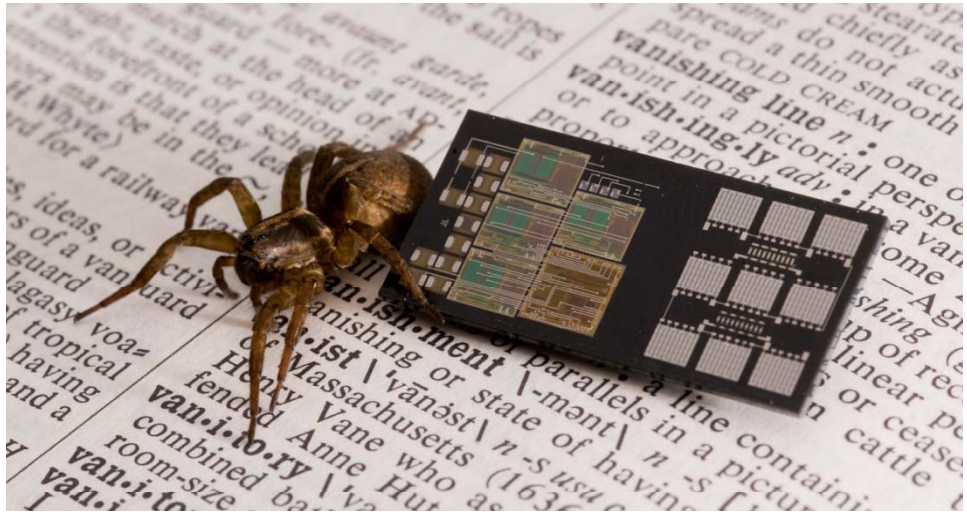
Conclusions and Summary

Summary

- Substrates used in the design overall did very well with the assembly steps. Substrates printed well, handled placement forces and successfully made it through a 260C reflow process with adequate wetting of the solder to the bond pads.
- T(0) shear testing showed all layout iUHD substrates had similar shear values to the same designed organic substrates. After 1000 cycles of LLTS, the silicon only area bond pads had shown some level of adhesion loss that resulted in a 50% reduction of shear value to T(0). On the other hand, shear values of devices over encapsulate areas showed no obvious reduction in adhesion or shear values.
- LLTS, MSL level 1 and uHAST testing showed no obvious substrate related problems with layer adhesion, as seen in CSAM. There was coarsening of the solder, but no evidence of solder joint cracking could be found from the thermal/moisture testing.
- Moiré analysis was performed on several of the different layout structures. Although obvious warpage could be seen from substrates entirely composed of encapsulate, the ones that had a 50% encapsulate to Silicon ratio showed no obvious signs of detrimental warpage

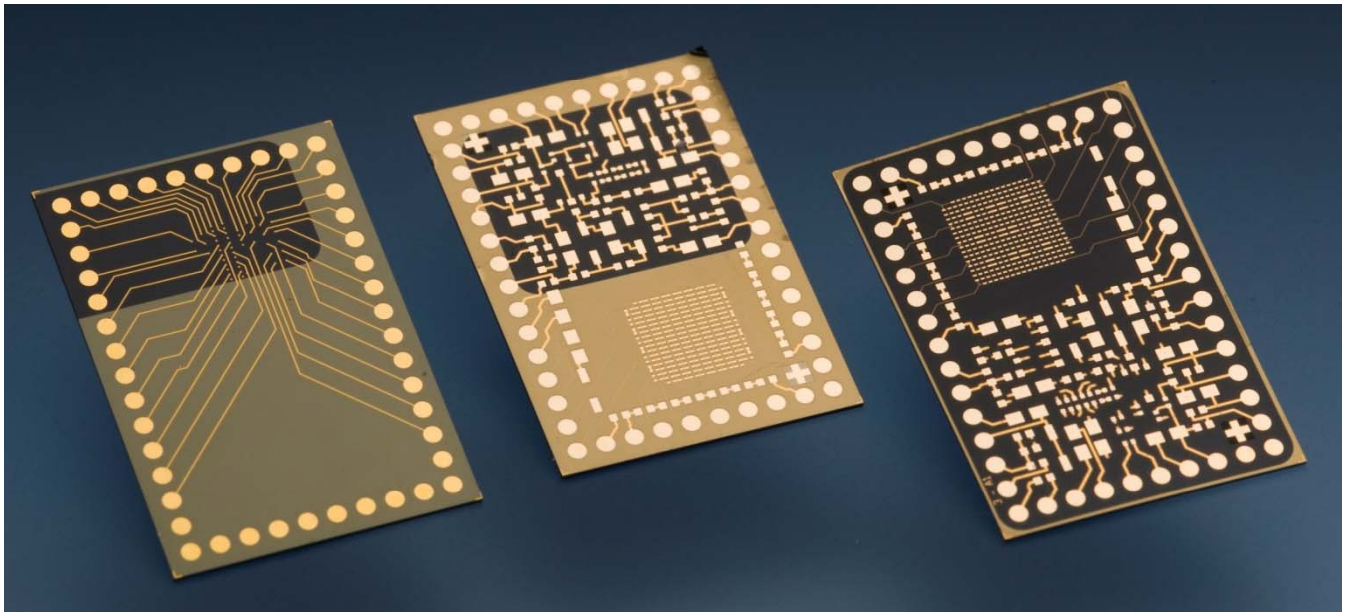
Summary

- iUHD offer order-of-magnitude increase in interconnect density for SOP
- Small size leads to lower thermal resistance than COTS BGAs
- Hybrid Si-encapsulant iUHD module offers better mechanical properties compared to all-Si and is thermo-mechanically stable with proper material selection:
  - Stress driven mainly by encapsulant-Si ratio
  - Extremes in stress occur at 50% loading for standard material
  - Stress increases as CTE increases, even when accounting for effect of modulus



Future Work

- Further reliability testing of various applications, substrate sizes and Si-Encapsulate ratios
  - Already 1000 thermal cycles, MSL Level 1
- RF and high speed I/O characterization
- 3-D module stacking
- Cost reduction through miniaturization



Thank You!!