Failure Analysis and Reliability of 3D Integrated Systems

Peter Ramm [1*], Armin Klumpp[1], German Franz [2], Laurens Kwakman [2]

[(1)] *Fraunhofer Institution for Modular Solid State Technologies EMFT*

Hansastrasse 27d, 80686 Munich, Germany

[(2)] *FEI Electron Optics, Achtseweg Noord 5, Eindhoven, the Netherlands*

* *corresponding author*

peter.ramm@emft.fraunhofer.de

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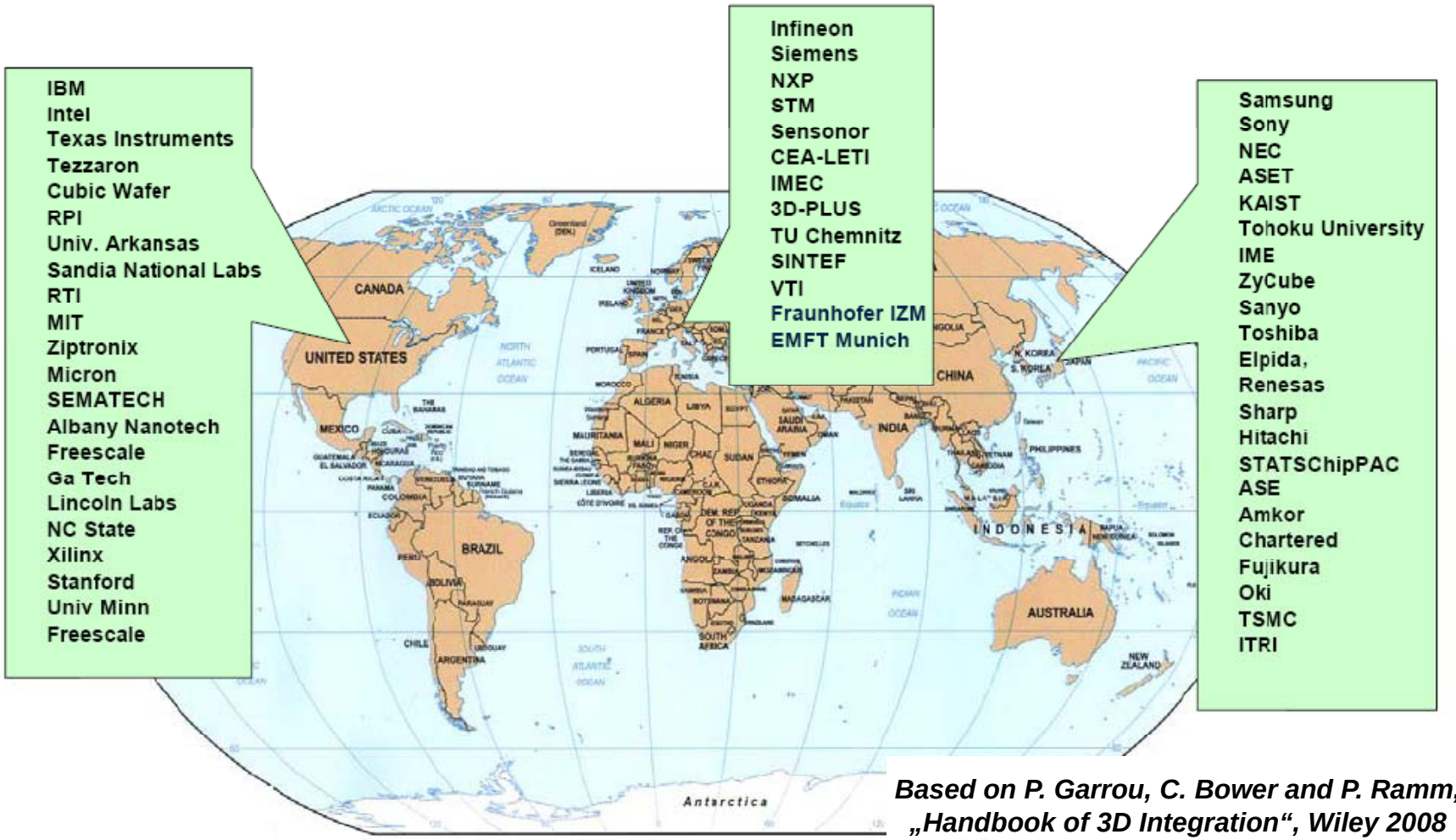
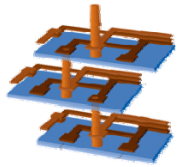
Global Activities in 3D Integration Technology

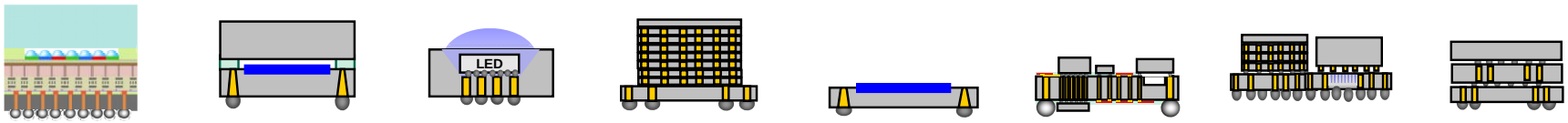


Based on P. Garrou, C. Bower and P. Ramm, „Handbook of 3D Integration“, Wiley 2008

3D TSV Application Segmentation



3D TSV Applications



CMOS image sensors
- WLP CIS
- BSI CIS
- 3D integrated CIS
- Wafer level auto-focus

MEMS & Sensors
- Gyros
- Acceleros
- Pressure sensors
- Si-micro
- FBAR filters
- RF-Switches
- Oscillators
- µProbes
- µFluidic / IJ
- µValves
- Finger-print sensors
- Micro-mirrors
- IR-bolometer
- Opto *(laser, VCSEL)*

HB-LED modules
- Mobile µ-Flash
- Automotive
- Projection engine
- LCD Backlight
- General Lighting

Stacked memories
- Stacked DRAM
- Stacked NAND Flash
- Stacked NOR / PCRAM

Power & Analog
- PA
- MOSFET
- IGBT
- IPD
- DC-DC converters

Wireless SiP
- MMICs
- BT/GPS/ WLAN/FM
- NFC
- UWB
- RFEM

Logic + Memory SiP
- Wide IO Baseband
- CPU / GPU / MCM
- FPGA
- High. Perf ASICs
- HPC

Logic & Analog 3D-SOC/SiP
- Baseband / DSP
- MCU / Processors
- DVB / DAB
- Low-end ASICs
- PMIC

YOLE DÉVELOPPEMENT

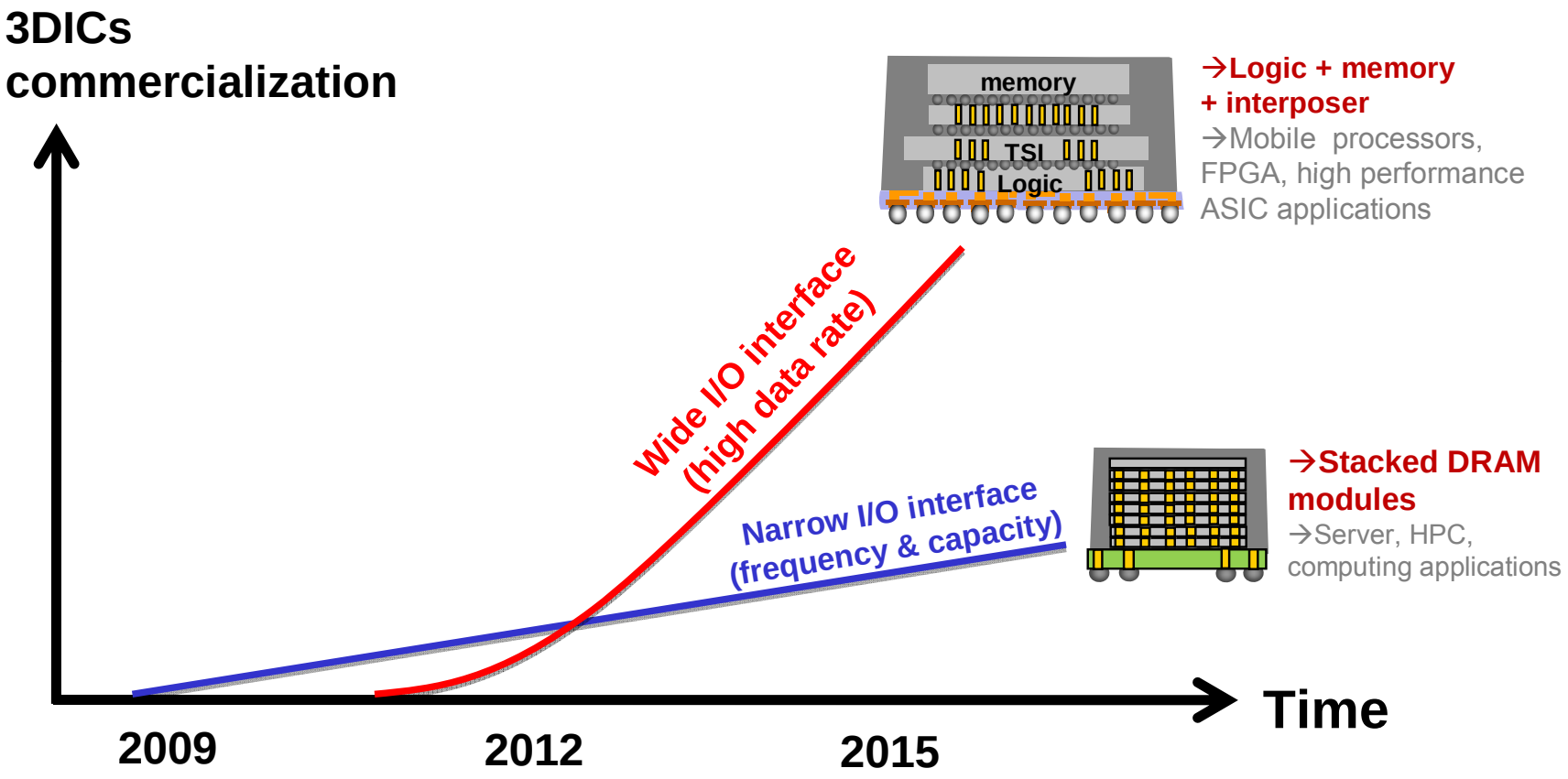
2nd IEEE International 3D System Integration Conference (3DIC 2010) – Invited Speakers and Chairmen

Peter Ramm, Fraunhofer EMFT Munich

IMAPS Int. Conf. Device Packaging, Scottsdale, March 10, 2011

Fraunhofer EMFT

Performance: “Narrow” vs “Wide” I/O interface



- **High demand is expected for “Wide I/O interface” applications, linked to the integration of Logic + Memories + interposer in the same package**

Application Development

2008 2010 2012 2014

BSI

Stacking of
ROIC, DSP

CMOS Image Sensor
50 µm TSV / 50-100 µm Si

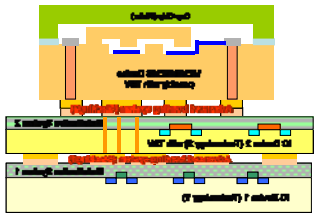
DRAM
35 µm TSV / 50 µm Si
Vias last

FLASH

DRAM & FLASH
< 5 µm TSV / < 20 µm Si
Vias middle

Memory on Logic
CoC no TSV / 50 -100 µm Si

Memory on Logic
5 µm TSV / 10 – 20 µm Si



Heterogeneous Integration
of MEMS/IC

3D Integration

Definition:

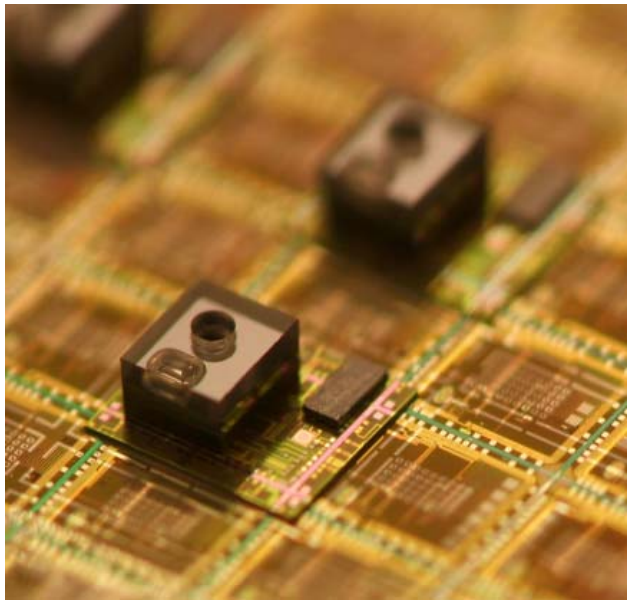
Fabrication of
stacked and vertically interconnected device layers

Motivations:

Form Factor
- Reduced volume and weight
- Reduced footprint

Performance
- Improved integration density
- Reduced interconnect length
- Improved transmission speed
- Reduced power consumption

"More than Moore" Applications
- Integration of heterogeneous technologies



Source: Infineon, Fraunhofer, SINTEF

3D Integration – Definitions (ITRS)

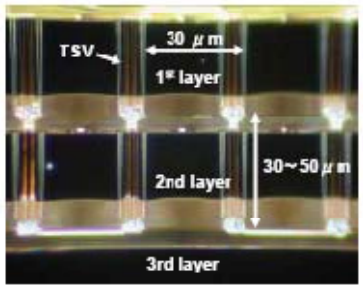
3D TSV Technology

- **3D-IC**

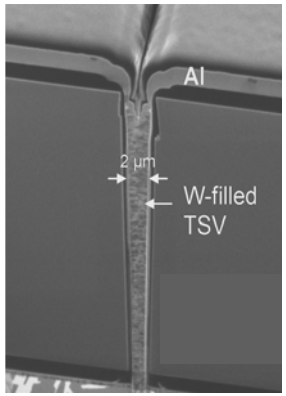
  3D Integrated **C**ircuit: stacking of transistor layers

  (3D connections at density level of local interconnects)

Source: Honda



Source: EMFT



- **3D-SIC**

  3D Stacked **I**ntegrated **C**ircuit

  (very high TSV densities)

Table INTC4 Intermediate Interconnect Level 3D-SIC Roadmap

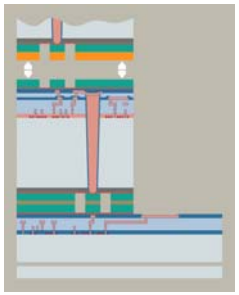
Intermediate Level, W2W 3D-stacking	*2009-2012*	*2012-2015*
Minimum TSV diameter	1-2 µm	0.8-1.5µm
Minimum TSV pitch	2-4 µm	1.6-3.0 µm
Minimum TSV depth	6-10 µm	6-10 µm
Maximum TSV aspect ratio	5:1 – 10:1	10:1 – 20:1
Bonding overlay accuracy	1.0-1.5 µm	0.5-1.0 µm
Minimum contact pitch	2-3 µm	2-3 µm
Number of tiers	2-3	8-16 (DRAM)

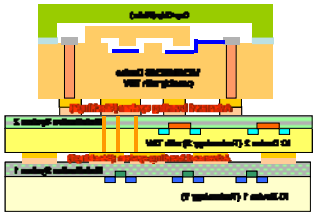
Source: ITRS 2009 Edition

- **3D-SOC**

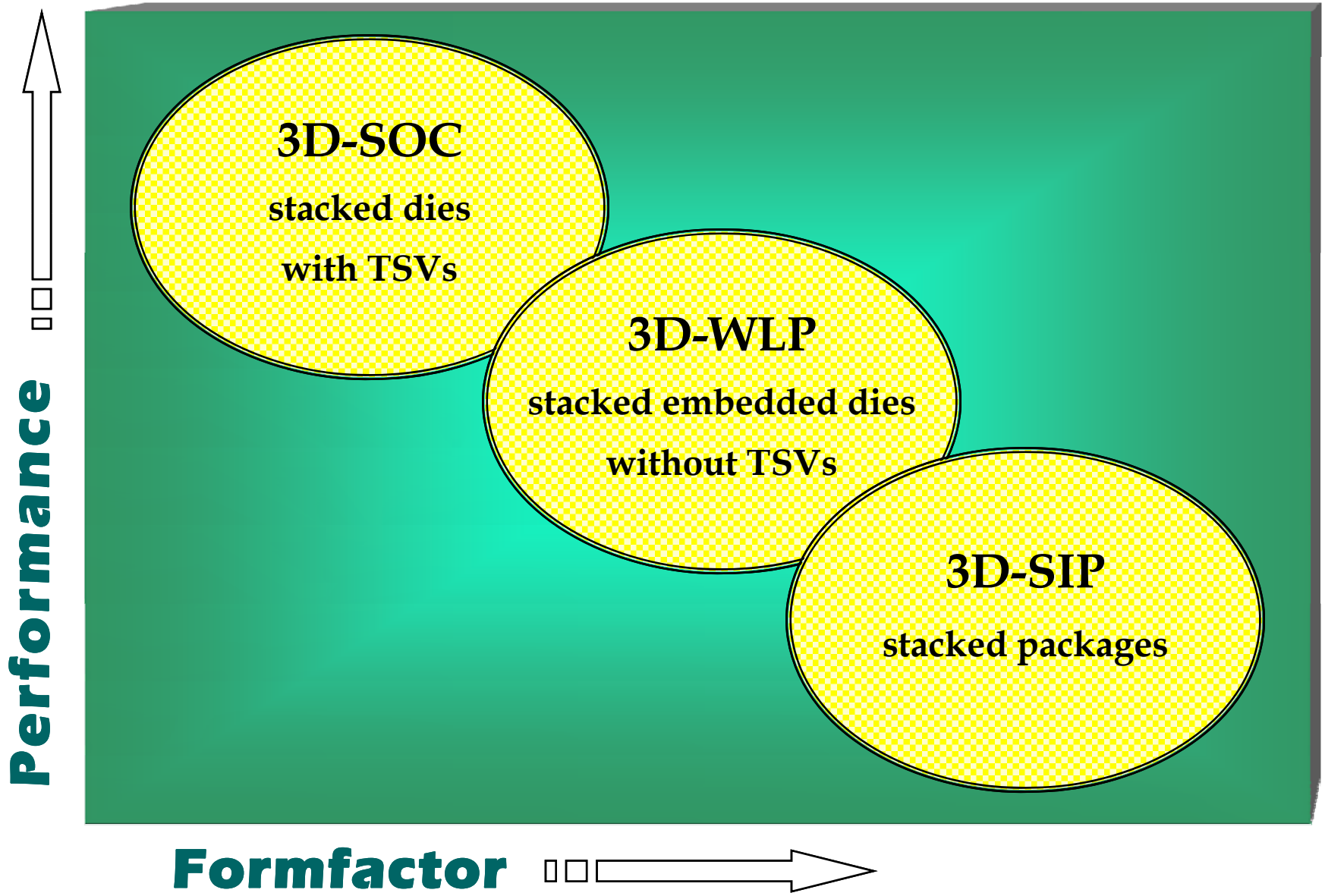
  3D System-**O**n-**C**hip: stacking of devices or large IC blocks (global level)

  - **Fabrication of Heterogeneous Systems**





3D Technologies for Heterogeneous Systems



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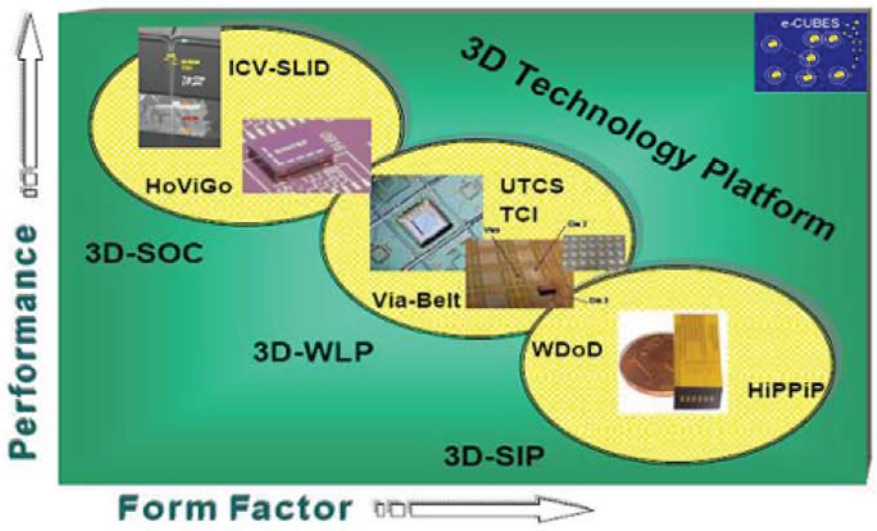
European 3D Technology Platform (e-CUBES)



Technology	e-CUBES Partner
3D-SOC	
Through Silicon Via (TSV) Technology (ICV-SLID)	Fraunhofer EMFT (formerly IZM-M)
Hollow Via & Gold Stud Bump Bonding (HoViGo)	SINTEF
3D-WLP	
Thin Chip Integration (TCI/UTCS)	Imec and Fraunhofer IZM & EMFT
Via Belt Technology Chip-in-Polymer and µInsert)	CEA-Leti
3D-SIP	
High Performance Package-in-Package Technology (HiPPiP)	3D-PLUS
Wirefree Die-on-Die Technology (WDoD)	3D-PLUS
Submicron Wire Anisotropic Conductive Film Assembly (SW-ACF)	Tyndall

Futue Fab International, Issue 34 (July 2010)
"The European 3D Technology Platform (e-CUBES)"
P. Ramm, A. Klumpp, J. Weber, M. Taklo, N. Lietaer, W. De Raedt, T. Fritzsch, T. Hilt, P. Couderc, C. Val, A. Mathewson, K. M. Razeeb, F. Stam

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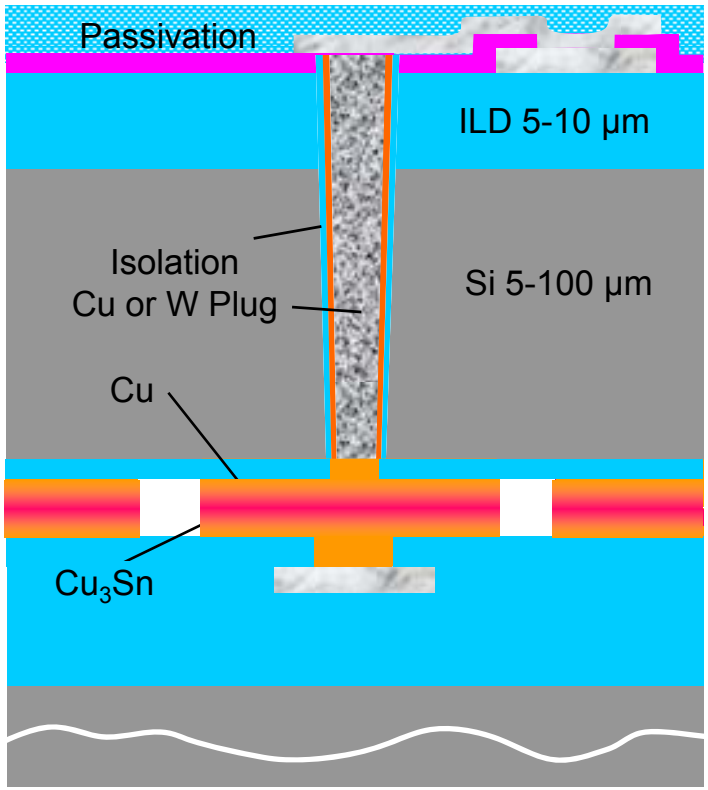
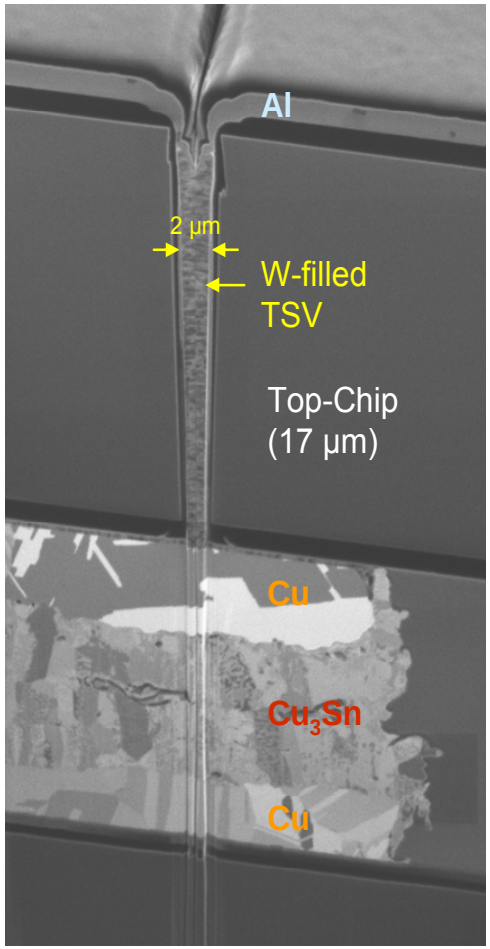
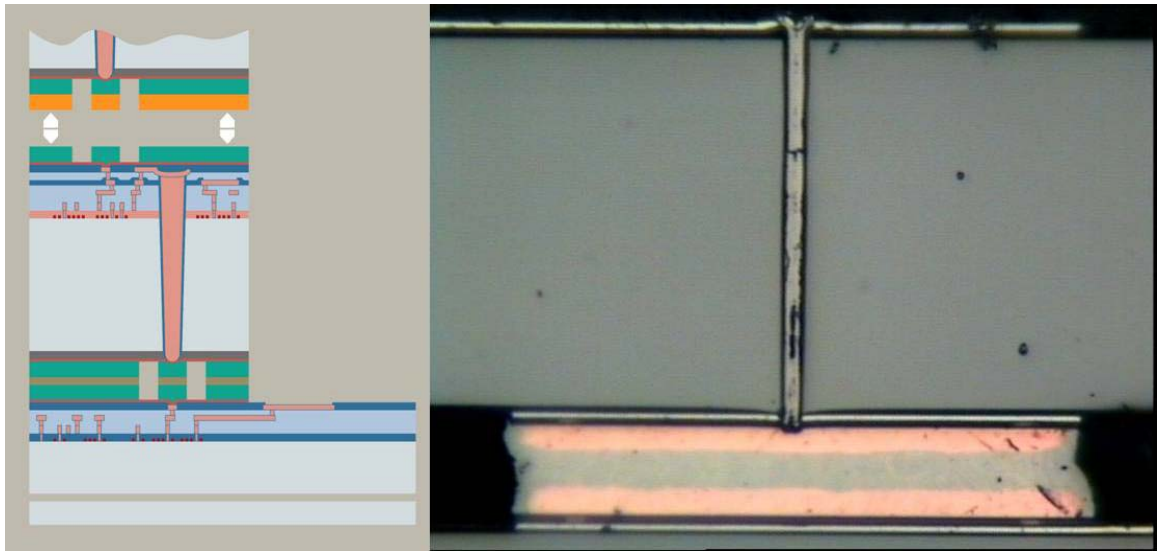
Chip-to Wafer Stacking by ICV-SLID Technology





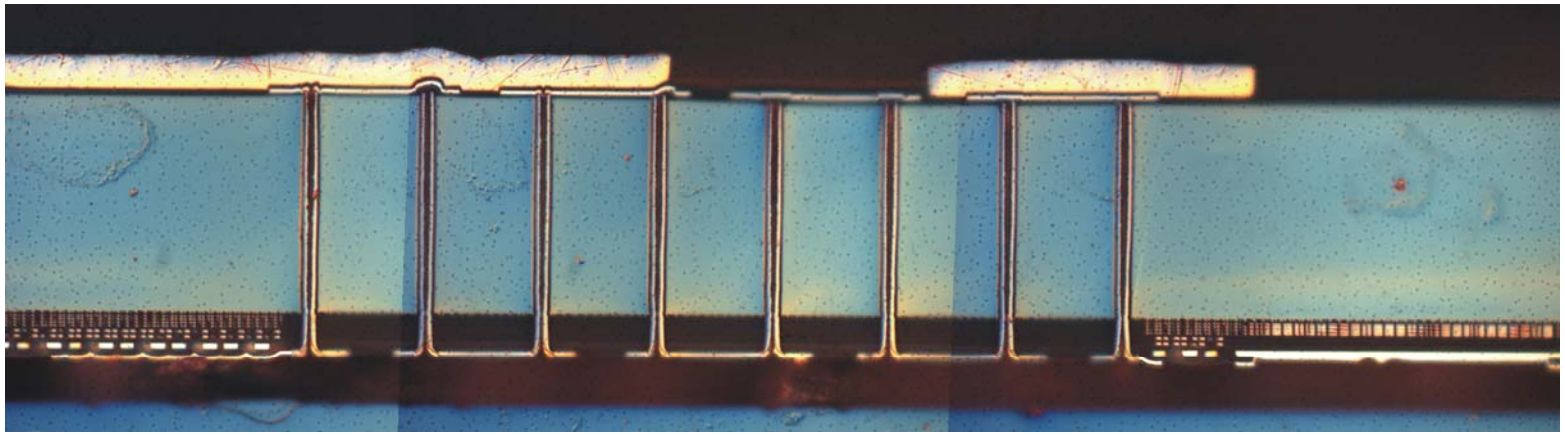
ICV-SLID – a robust 3D TSV Technology, but ...



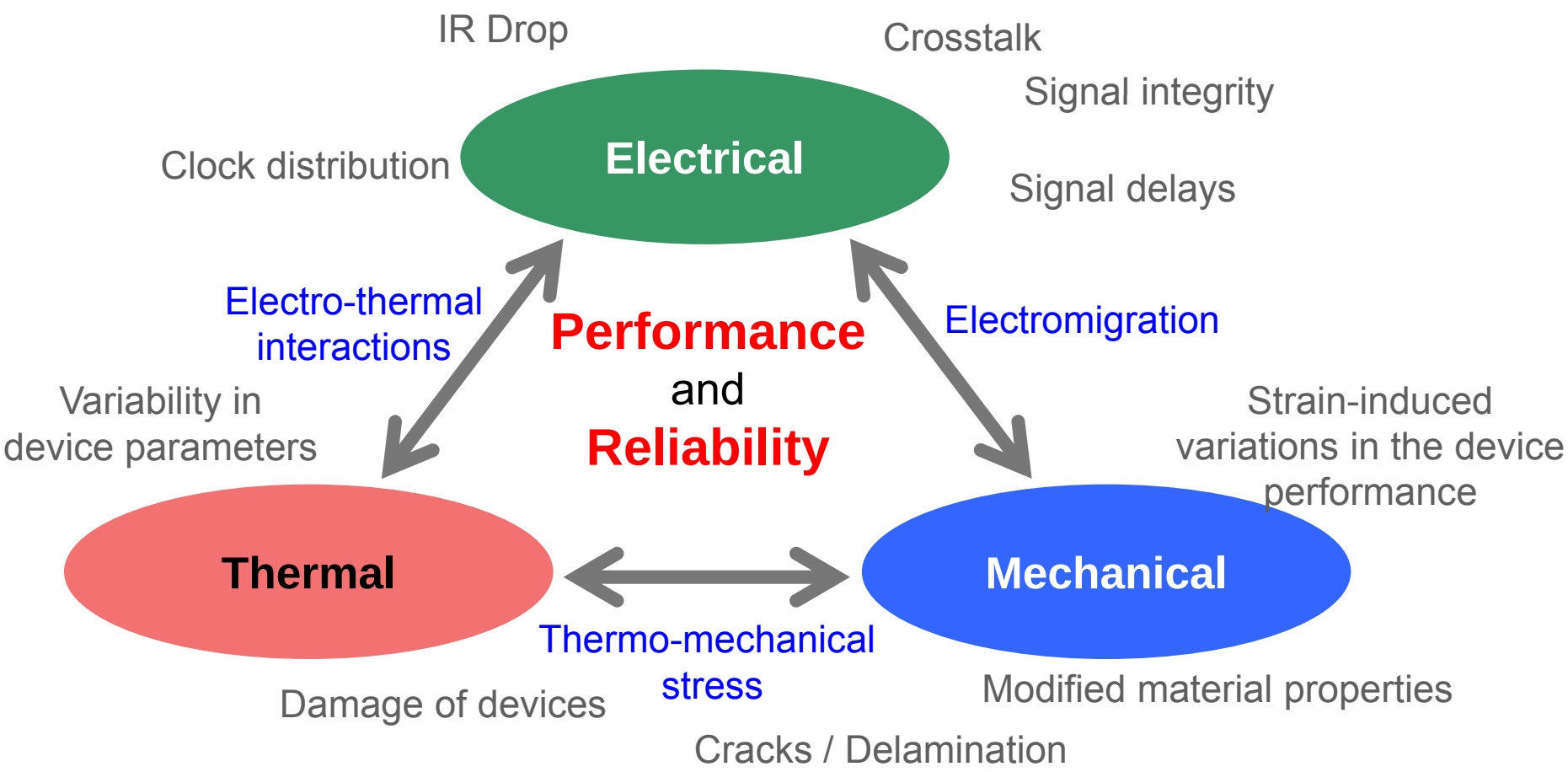
Source: Fraunhofer EMFT

ASIC (7-level metallization)
Process control module (PCM)

Daisy chains in PCM

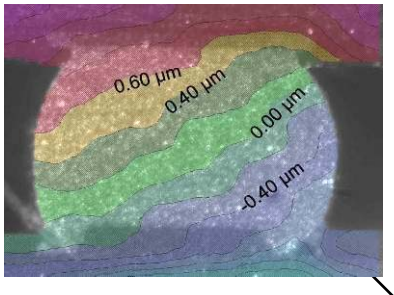


3D Integration – Impact on System

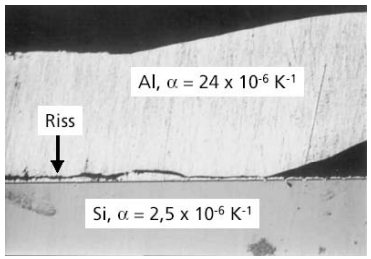


Ref.: A. Wilde, P. Schneider, P. Ramm, DTC 2010

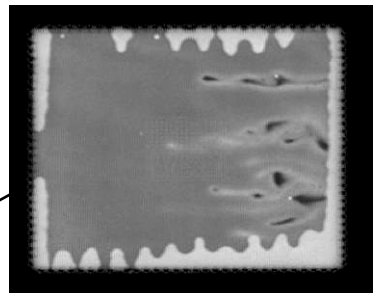
Failure Mechanisms 3D Integration



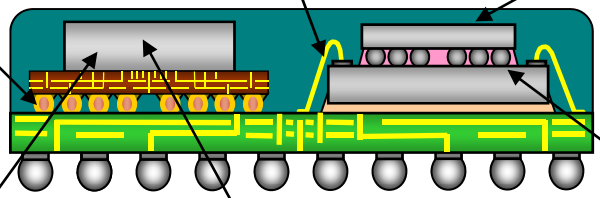
Solder Fatigue
(microDAC)



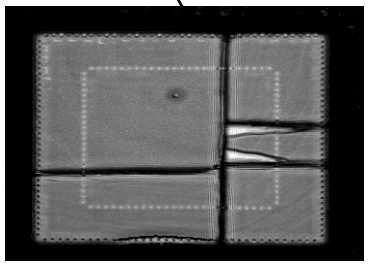
Wirebond Failure



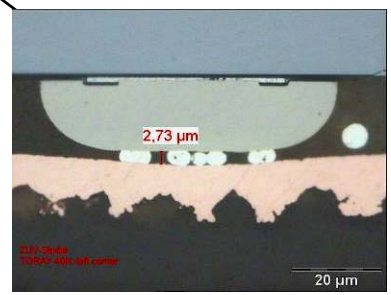
Delamination/
Interface crack



TSV Failure



Die Crack

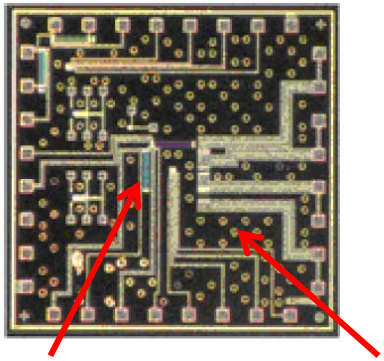


ACA Failure

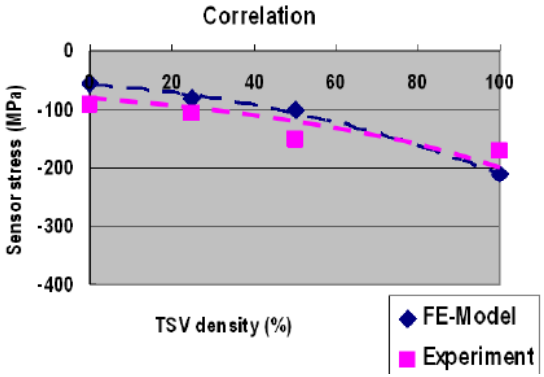
ECTC 2010

TSV Stress Testing and Modeling

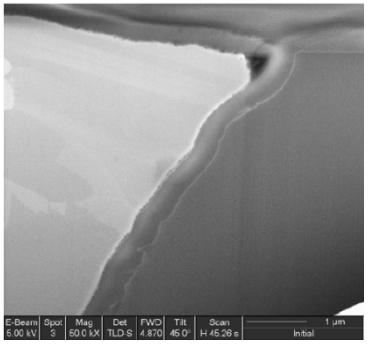
Masazumi Amagai, Yutaka Suzuki
Modeling Group, TMG Japan, Texas Instruments

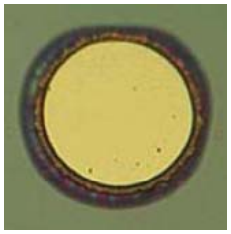


stress-sensor via

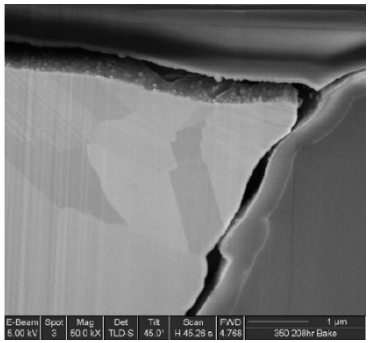


compressive stresses in Si for different via population densities

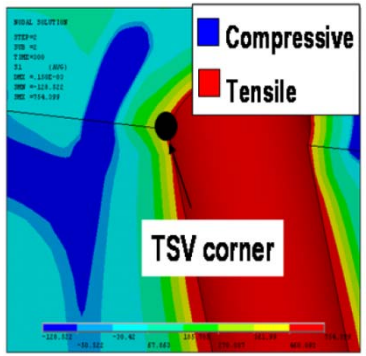




before annealing



400 °C annealing



the paper addresses:

- stress and strain measurement in Cu TSVs
- damage due to annealing, picture of delamination
- does not interprete the findings

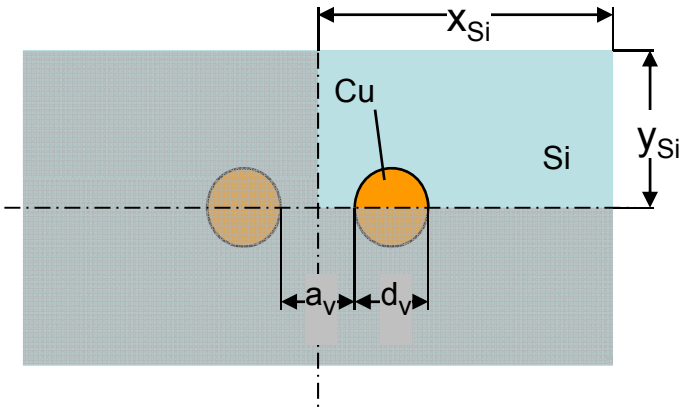
Stress in Silicon due to TSV-Array

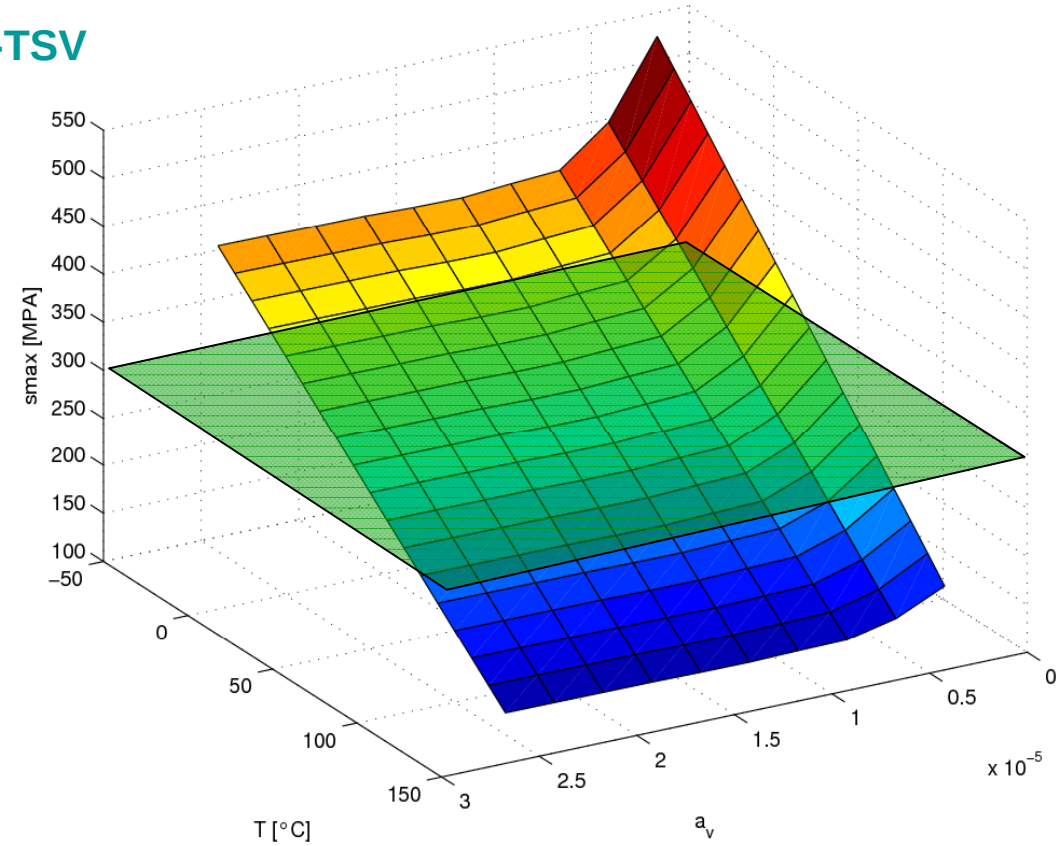
Example: Silicon substrate with Cu-TSV

diameter$_{TSV}$ = 10 µm
distance variation a_V = 2.5 .. 25 µm
depth $_{TSV}$ = 50 µm

Cell size
x_{Si} = 5* d_v µm
y_{Si} = 3* d_v µm

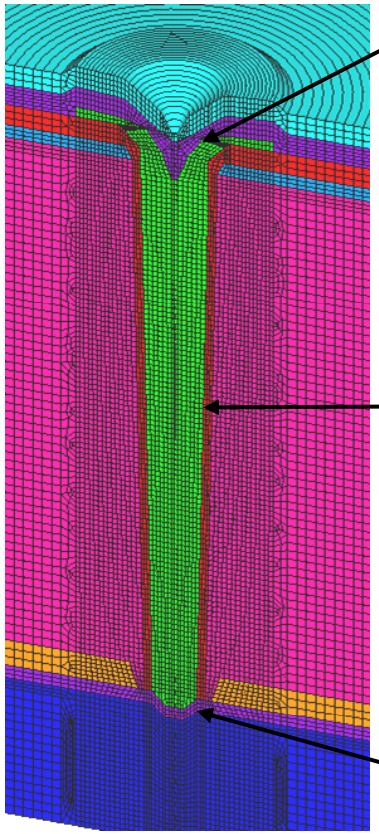
annealing temperature
= 200 °C





- Stress increases exponentially with reduced distance between TSVs
- Deposition / annealing temperature adds linear component to stress values

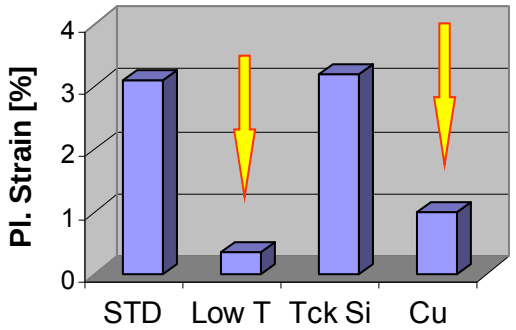
Simulation: Critical Locations



Top:
AlSiCu
with SiO2/W

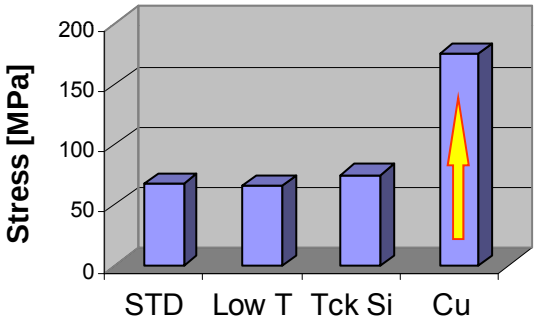
TSV centre:
W or Cu
with SiO2

Bottom:
Cu
with W/CuSn

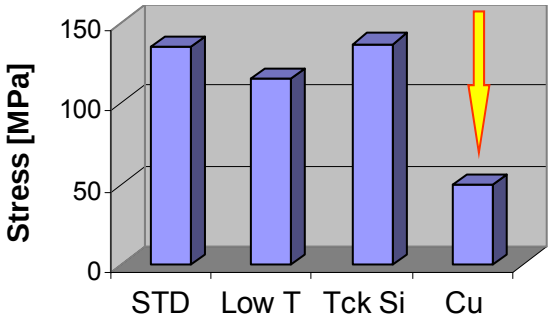


Low T proc & Cu promising

no periodic plasticity



High stress due to Cu filler (CTE!)



Cu promising

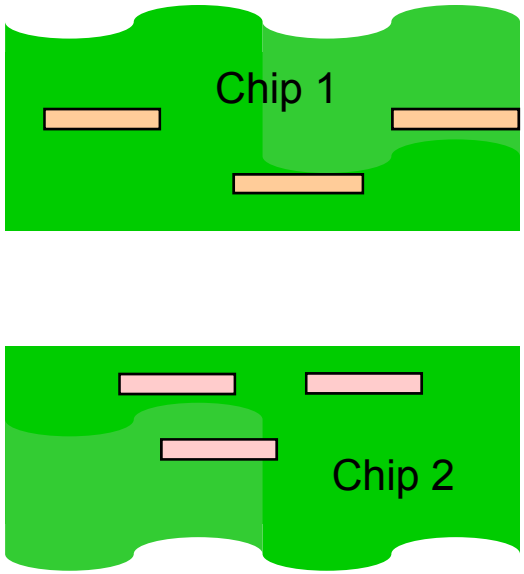
Ref.: P. Ramm, J. Wolf, B. Wunderle in „Handbook of 3D Integration“, Wiley 2008

Issues for Production Launch of 3D TSV Technology

- Die degradation due to TSV technology
  - Stress fields (homogeneous, inhomogeneous)
  - Copper contamination due to direct silicon access ?
- TSV: electrical behavior
  - Engineering reliability
  - Electromigration ?
- Interconnect pad: electrical contact reliability
  - Chip warpage (stress introduced by device fabrication)
    due to e.g. passivation layer, BCB, polyimide or oxide/nitride (tensile stress)
  - Lateral stress due to assembly / bonding process
    metal system melting or solidification temperatures
- Thermal management

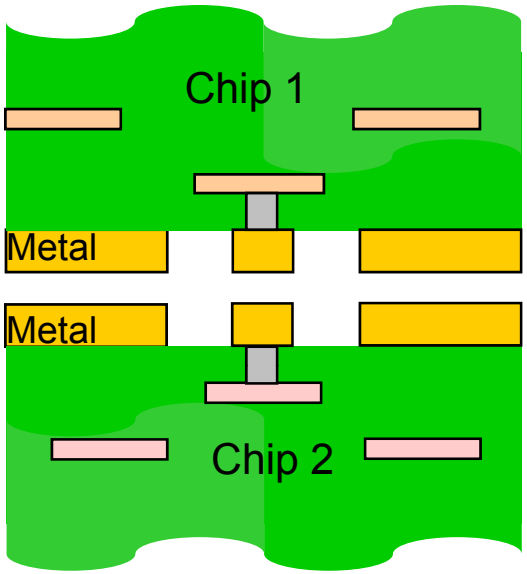
  T: mean temperature
  ΔT: temperature swing
  grad T: local temperature distribution (hot spots)
- Testability of subsystems

Permanent Bond Technologies for 3D Integration



Direct Oxide Bonding

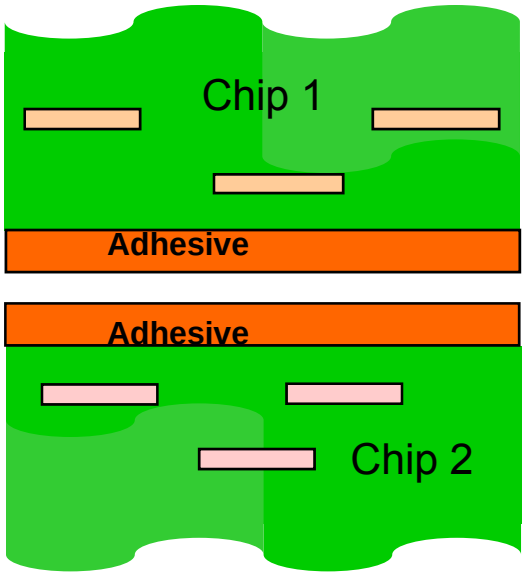
Via Last
Low temperature/pressure
High sensitivity to defects
High flatness/roughness requirements



Direct Metal Bonding

Via First and Via Last

Cu–Cu, Au–Au, … Intermetallic Compounds (IMC)



Adhesive Bonding

Via Last
Medium temperature/pressure
Defect tolerant
Low flatness/roughness requirements

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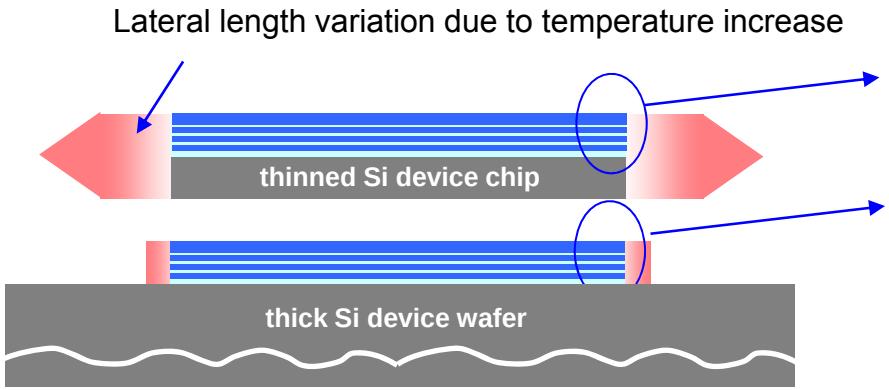
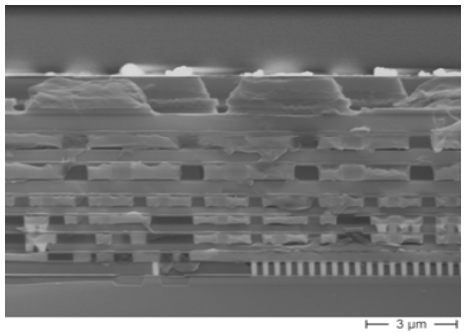
Fraunhofer EMFT

Mechanical Stress Issues due to Bonding Process



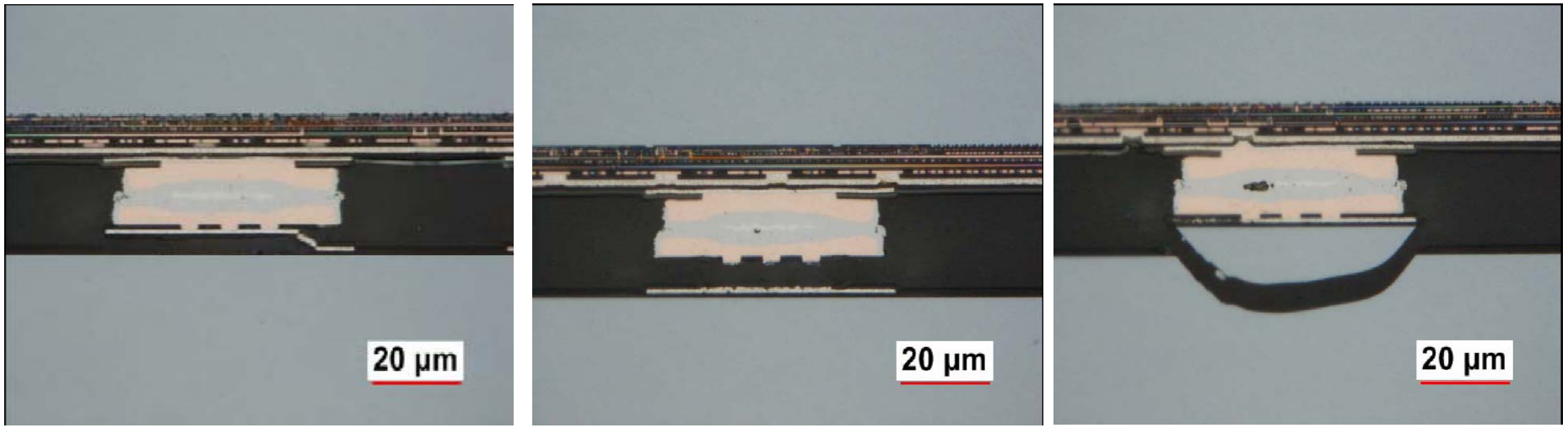


IC multilevel metallization (MLM): Metal/ILD compound (e.g. 56% dielectrics and 44% metal)

- "Freezing" of different dimensions takes place at the moment of interconnect solidification.
- Depending on the technology, this temperature can be far above room temperature or operating temperature of the devices:
  - SLID: Isothermal solidification at temperature set point; variation between melting point and up to 300 °C (Sn, mpt. 230 °C)
  - µ-bumps: Melting point of eutectic material composition e.g. 220 °C for AgSn
  - Cu-Cu: Bonding temperature 200 (?) … 400 °C

Materials of interest and their thermal expansion coefficient α [ppm / K]
Aluminium, 25; Copper, 17; Gold, 14; Silver, 20; Silicon, 2.6; SiO2, 0.75

“Failure Archive” (without process optimization)



a) b) c)

Typical impact of high stress due to bonding process:

a) Delamination of dielectrics (redistribution layer)
b) Delamination of complete SLID-pad
c) Local cracking of silicon substrate

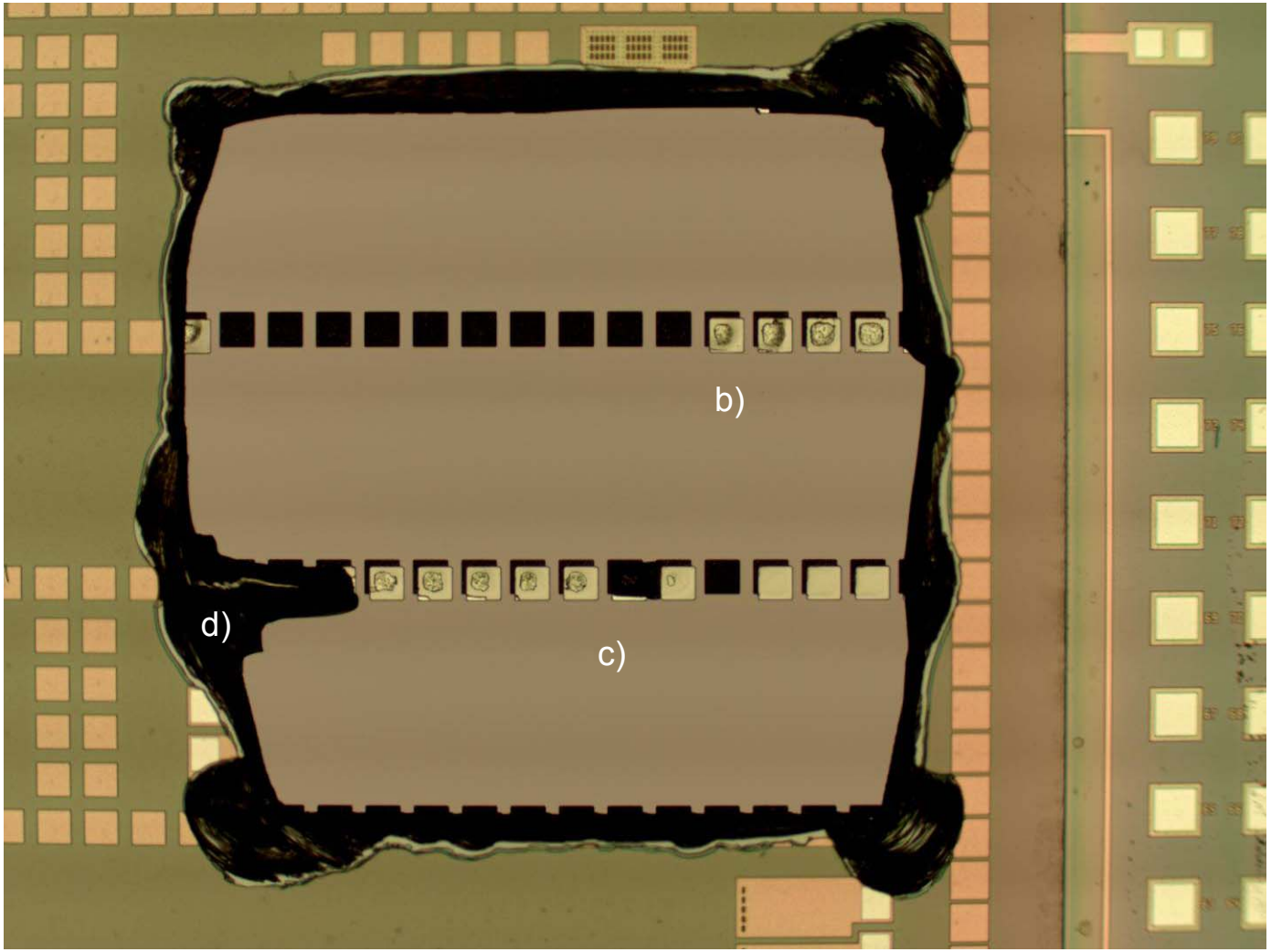
“Failure Archive” (2)

Impact of high stress:

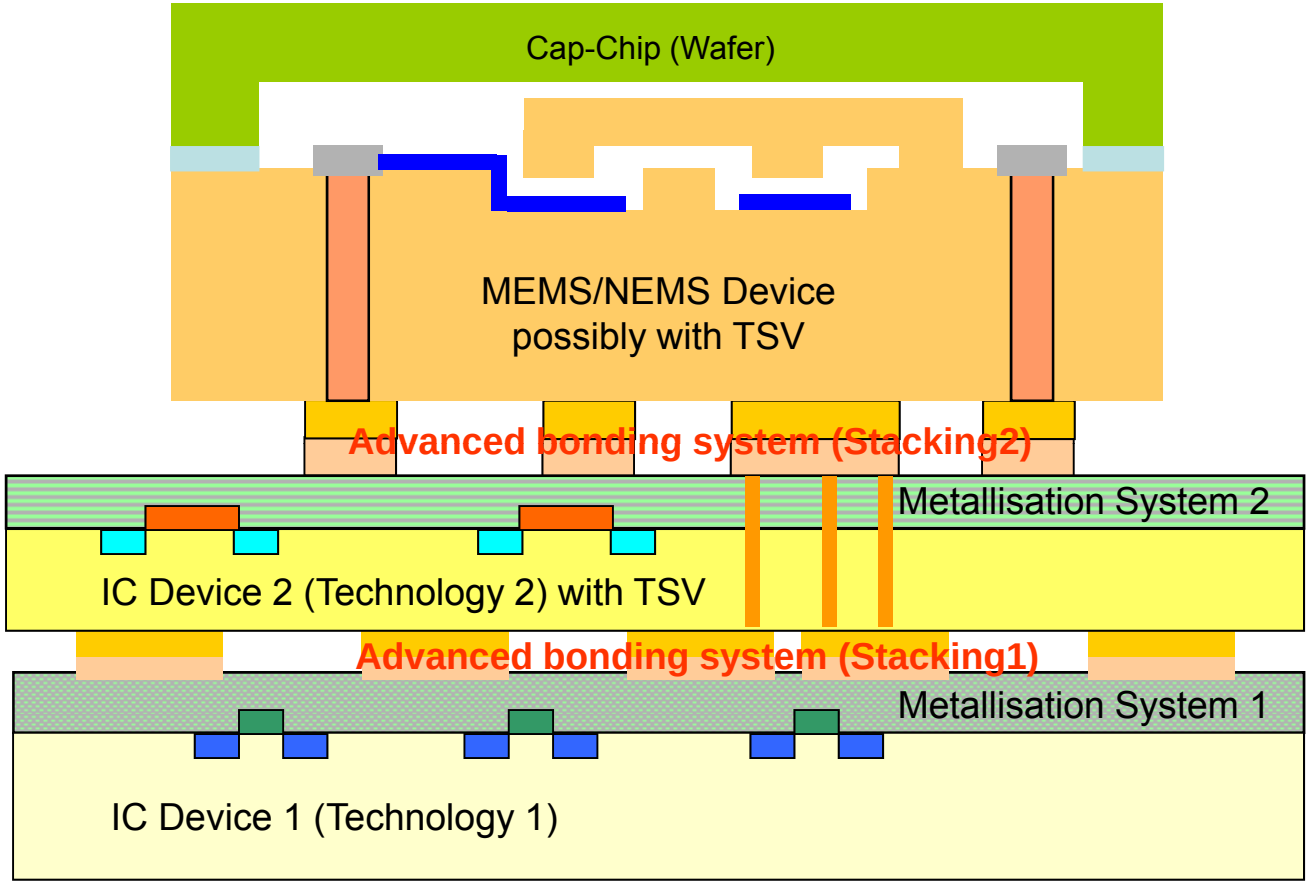
b) Delamination of complete SLID-pad

c) Local cracking of silicon substrate

d) Partially “explosive” removal of top chip silicon



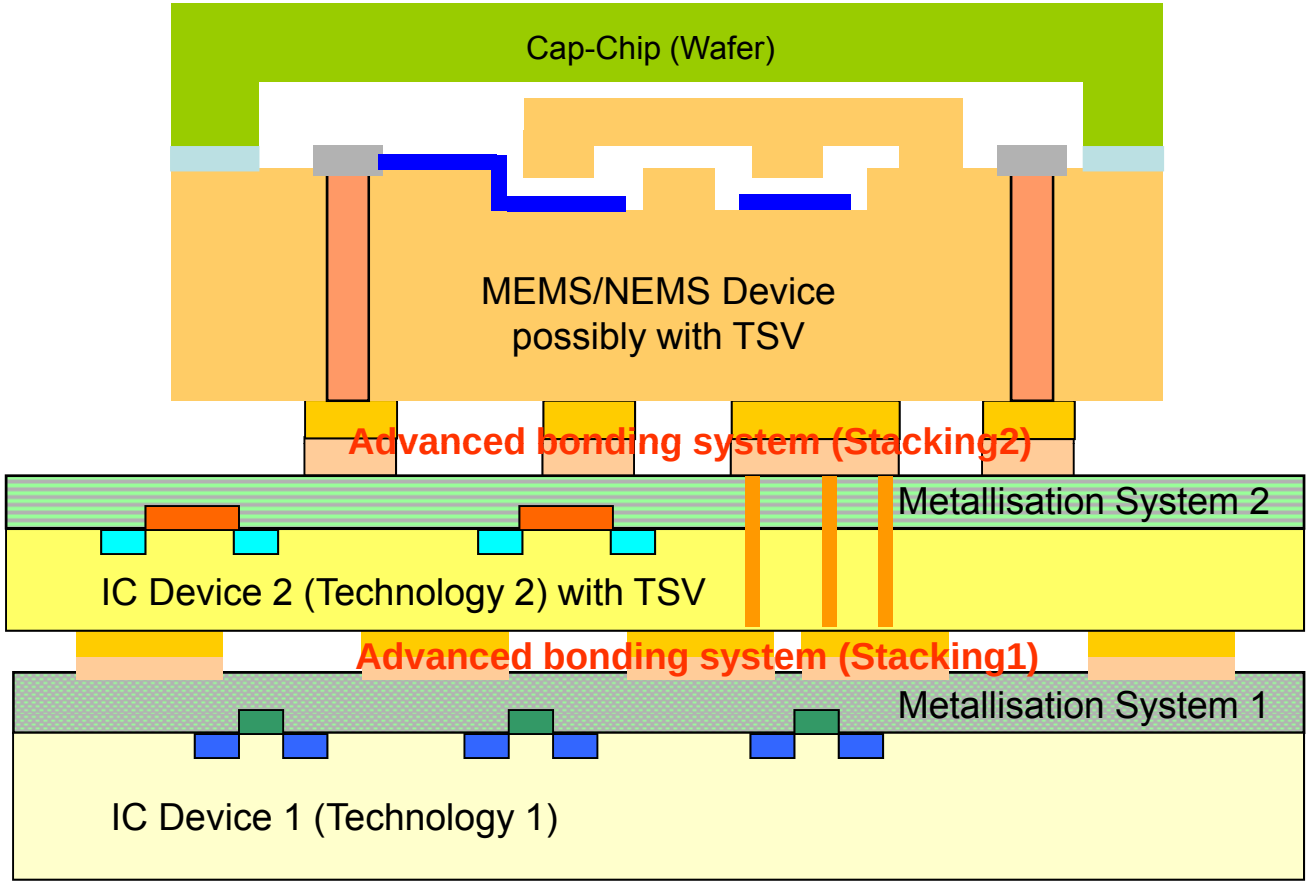
3D MEMS / IC Integration – a Challenge!



Issues for **producibility and reliability:**

- Fragile mechanical structures in MEMS/NEMS devices
- Stress induced by **TSVs** and **bonding processes**

3D MEMS / IC Integration – a Challenge!



Robustness and reliability of 3D fabrication processes are the **basic requirements** for future 3D products

- **Physical failure analysis** is essential for implementation of 3D TSV
- Large areas of interest – **very challenging for FIB analysis**

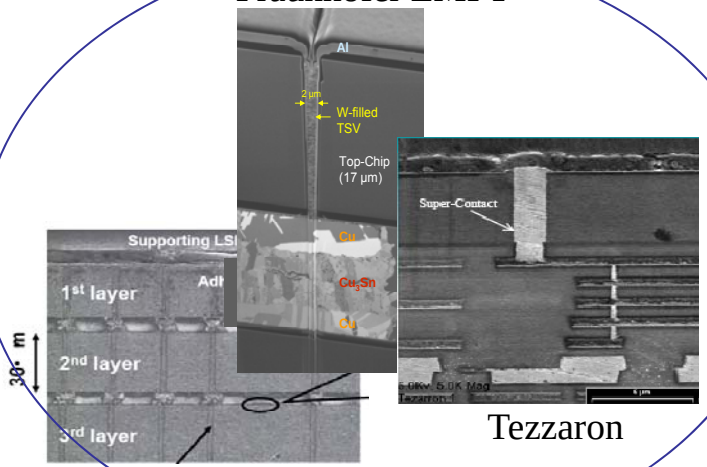
TSVs for IC vs. MEMS

Substrate thickness (µm)

30 … 50 … 300 … 1000

IC

Fraunhofer EMFT

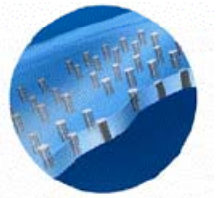


ZyCube

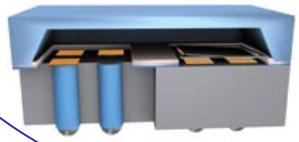
Tezzaron

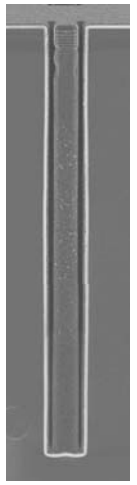
SINTEF

NEC Schott

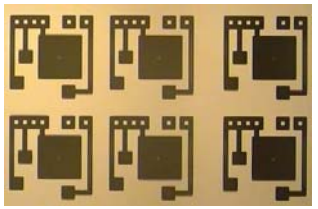


Silex





Planoptik



MEMS

Source M. Taklo / SINTEF

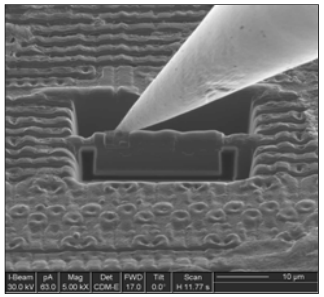
Pitch (µm) 30 … 50 … 100 …

3D Device Analysis Challenges

- For “Chip Access” large volume material removal is needed within reasonable time and at precise locations…
- The zone of interest has a Field of View of ~ 100 x 100 μm, and has to be inspected with nm resolution….

We need to think big while keeping eye for details!

More Moore:

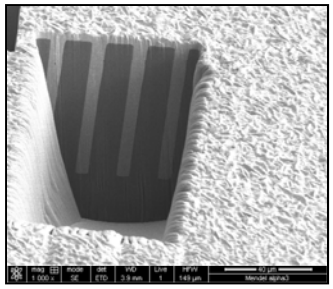


Typical volumes: 10 x 10 x 10 μm^3

Standard FIB mill rate < 5 μm^3 /s

Total Mill time ~ 3 - 10 minutes

More than Moore:

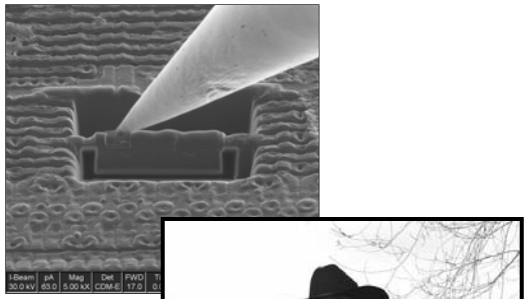


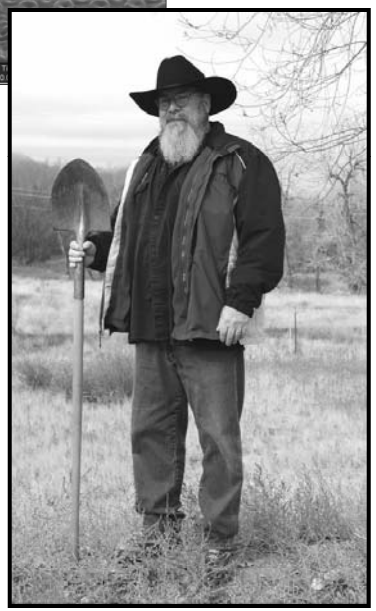
Typical volumes: 100 x 100 x 100 μm^3

Standard FIB mill rate < 5 μm^3 /s

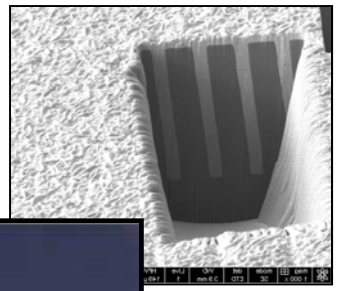
Total Mill time ~ 50 hrs!

What problems is Plasma-FIB designed to solve:





Pick your tool for large volume removal



LMIS FIB: ~ 20-60 [nA]

Plasma-FIB: ~ 1 [uA]

A system that provides unique and fast ion milling capabilities for rapid cross sectioning of features from 50 to 1000 microns.

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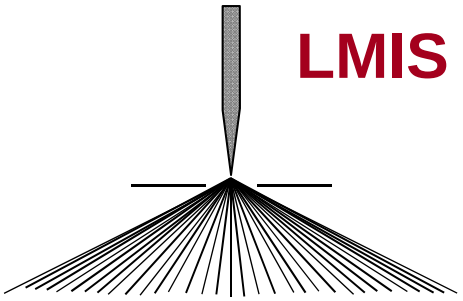
Comparison of FIB Sources

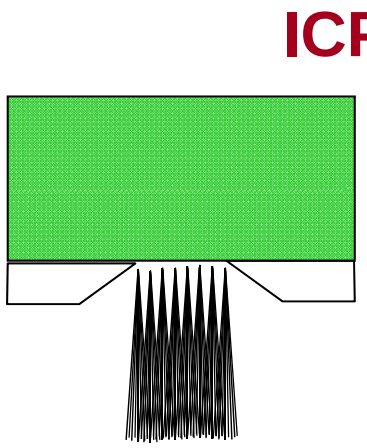
- Liquid Metal Ion Source

  - **"Point" source** with **low angular intensity**
    - Angular intensity = 0.02 mA/sr
    - Virtual source = 50 nm
    - Brightness =1x10^{6} Am^{-2}sr^{-1}V^{-1}
  - Optical Challenge: Above ~10 nA, spherical aberrations limit performance, limited total current

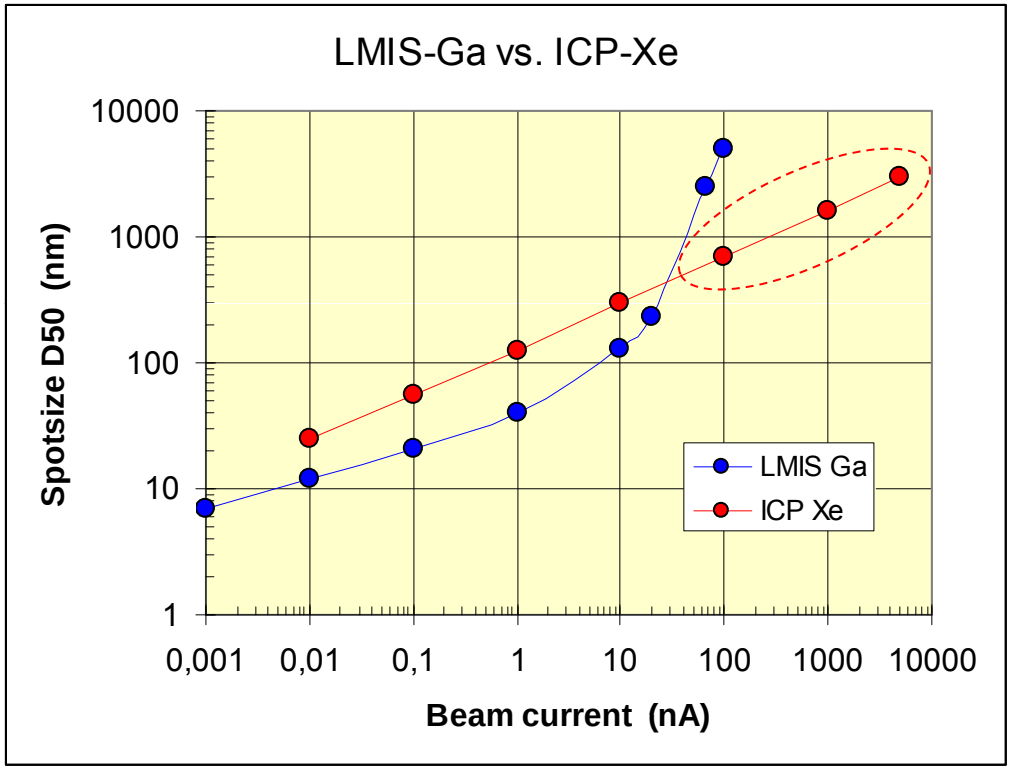


- Inductively Coupled Plasma Ion Source

  - **Broad source** with **high angular intensity**
    - Angular intensity = 50 mA/sr
    - Virtual source = 15 µm
    - Brightness ~1x10^{4} Am^{-2}sr^{-1}V^{-1}

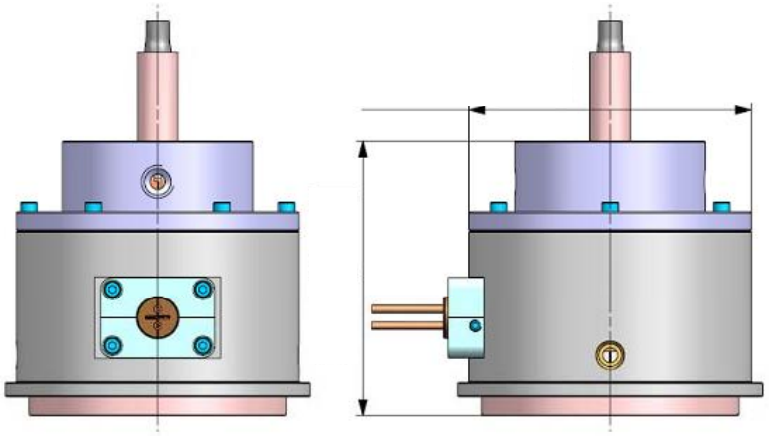


Comparison of FIB Sources (2)

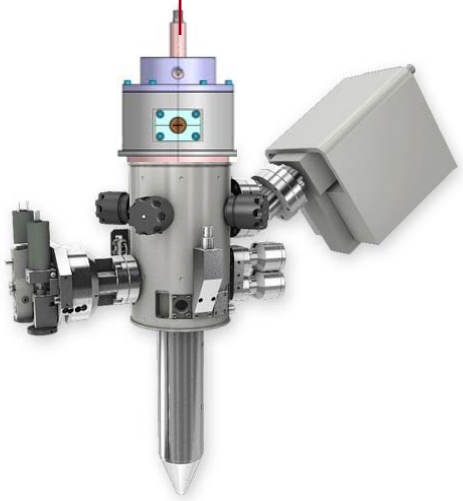


- ✓ High volume milling / high beam current
- ✓ Ga-FIB loses size advantage to plasma source as beam current goes above 20-60 nA
- ✓ Xe has high sputter yield, high brightness, and low energy spread
- ✓ No Ga contamination
- ✓ Stability, long lifetime

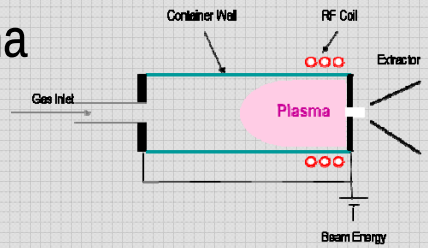
A New Plasma-FIB Source Module



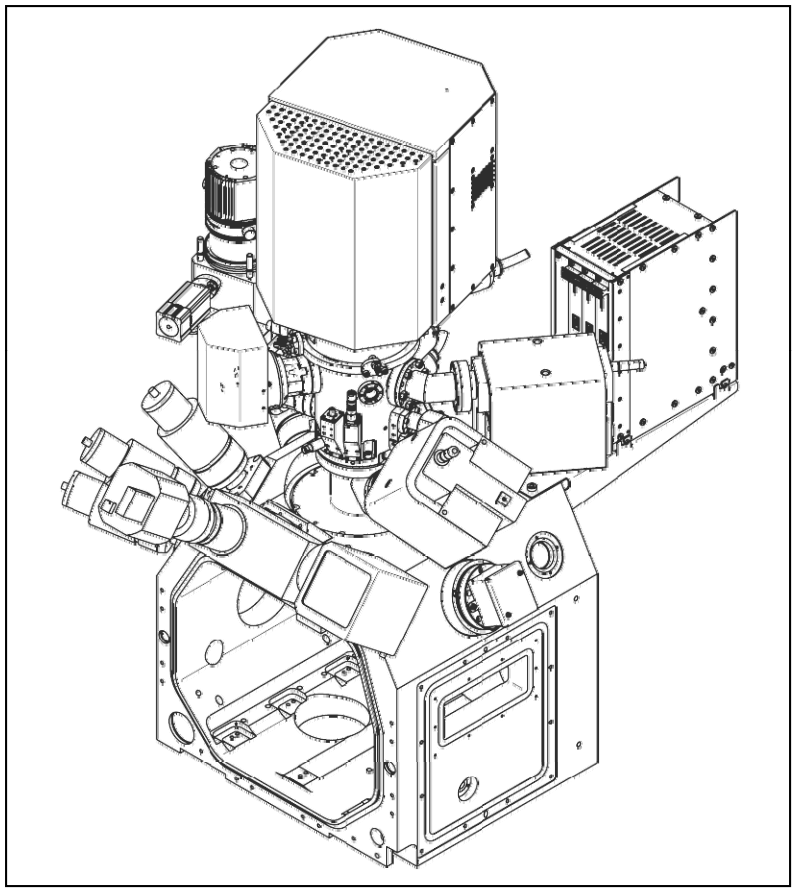
Patented technology developed at FEI



Inductively Coupled Plasma (ICP)



Integrated in a Newly Designed FIB Platform



FEI Assessment Center at Fraunhofer EMFT Munich

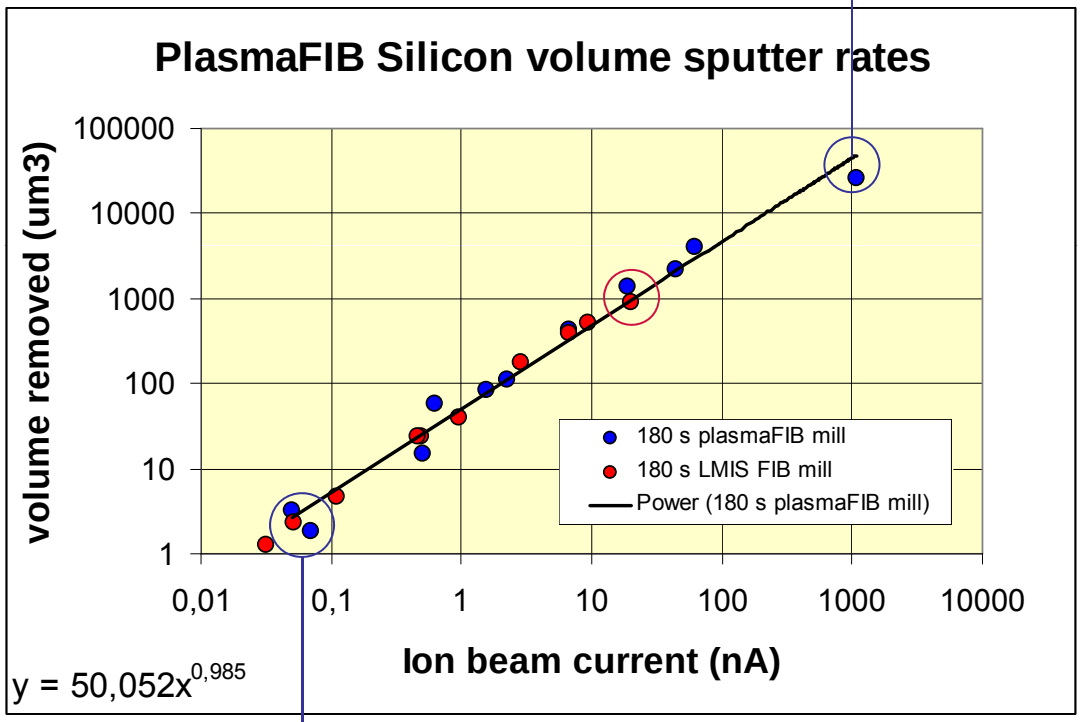
Developed in European ENIAC project JEMSIP-3D

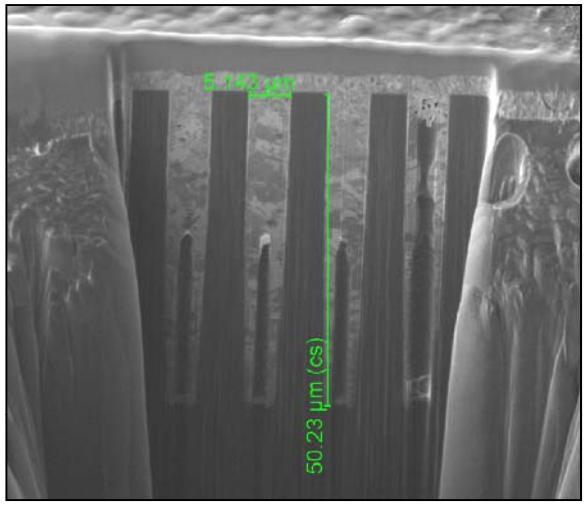
2009: concept-design phase

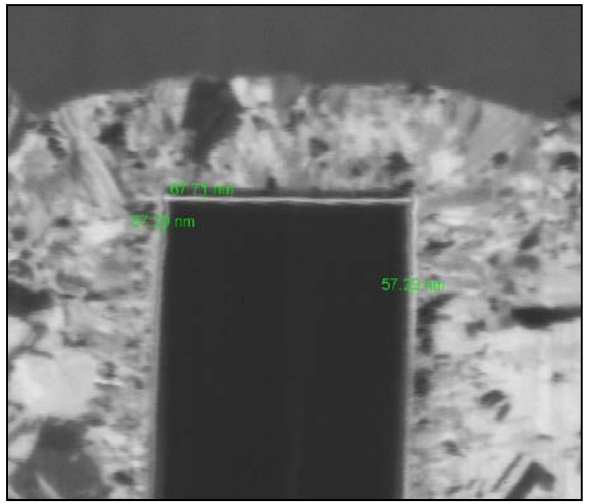
2010: working plasmaFIB system

First Plasma-FIB Results

FIB milling time: ~ 10 min for 200000 um^3



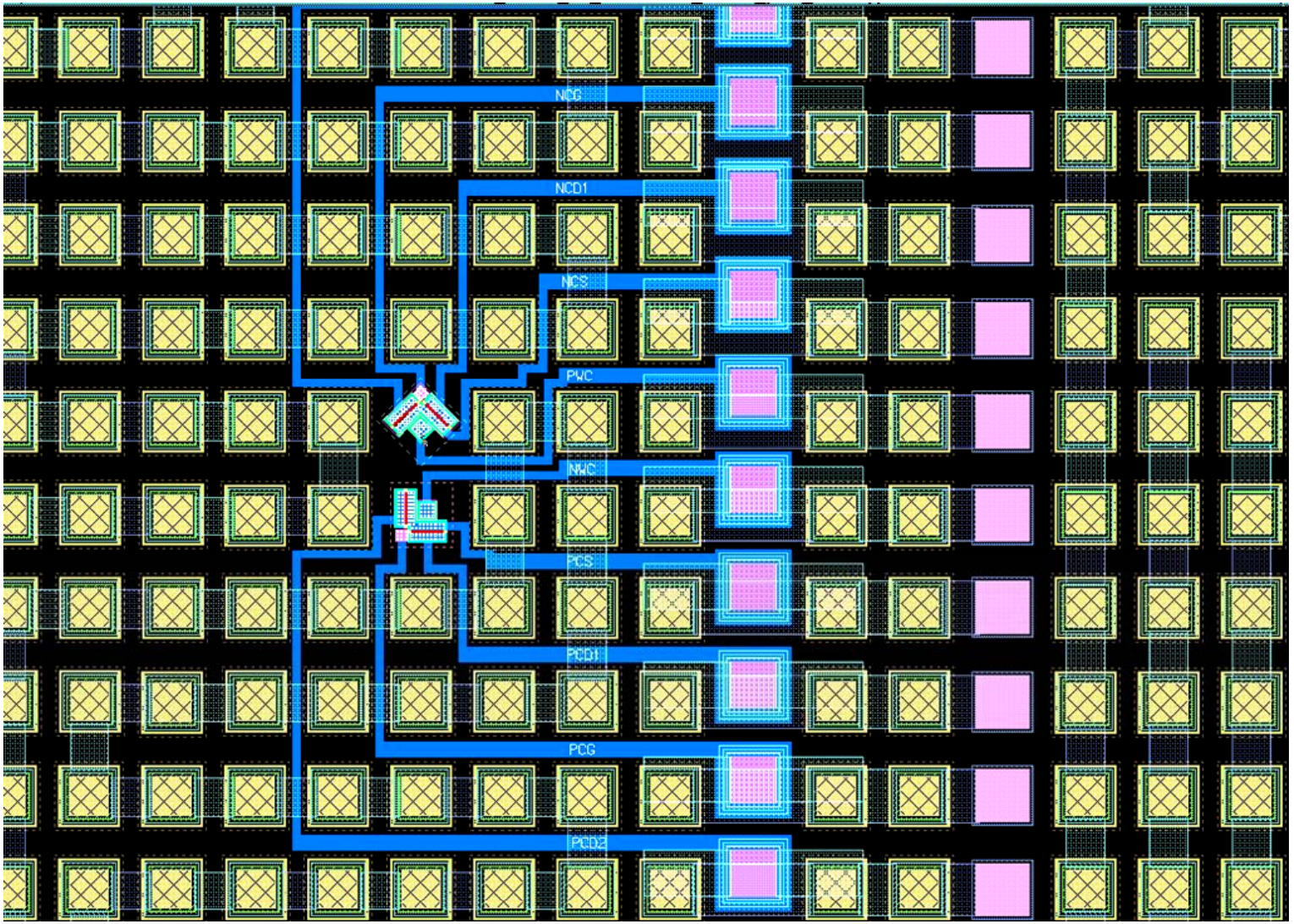




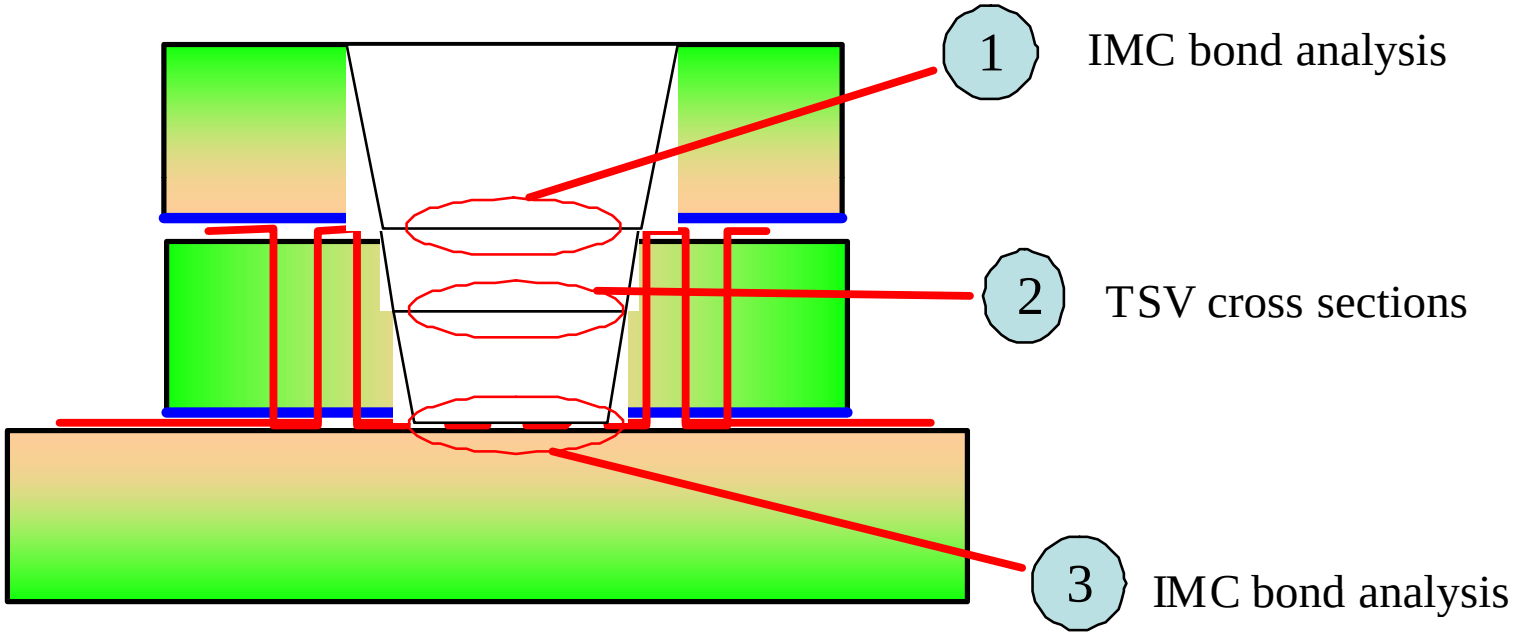
FIB imaging resolution: ~ 60 nm at 50 pA

Reliability Testchip with CMOS stress sensors (EMFT)

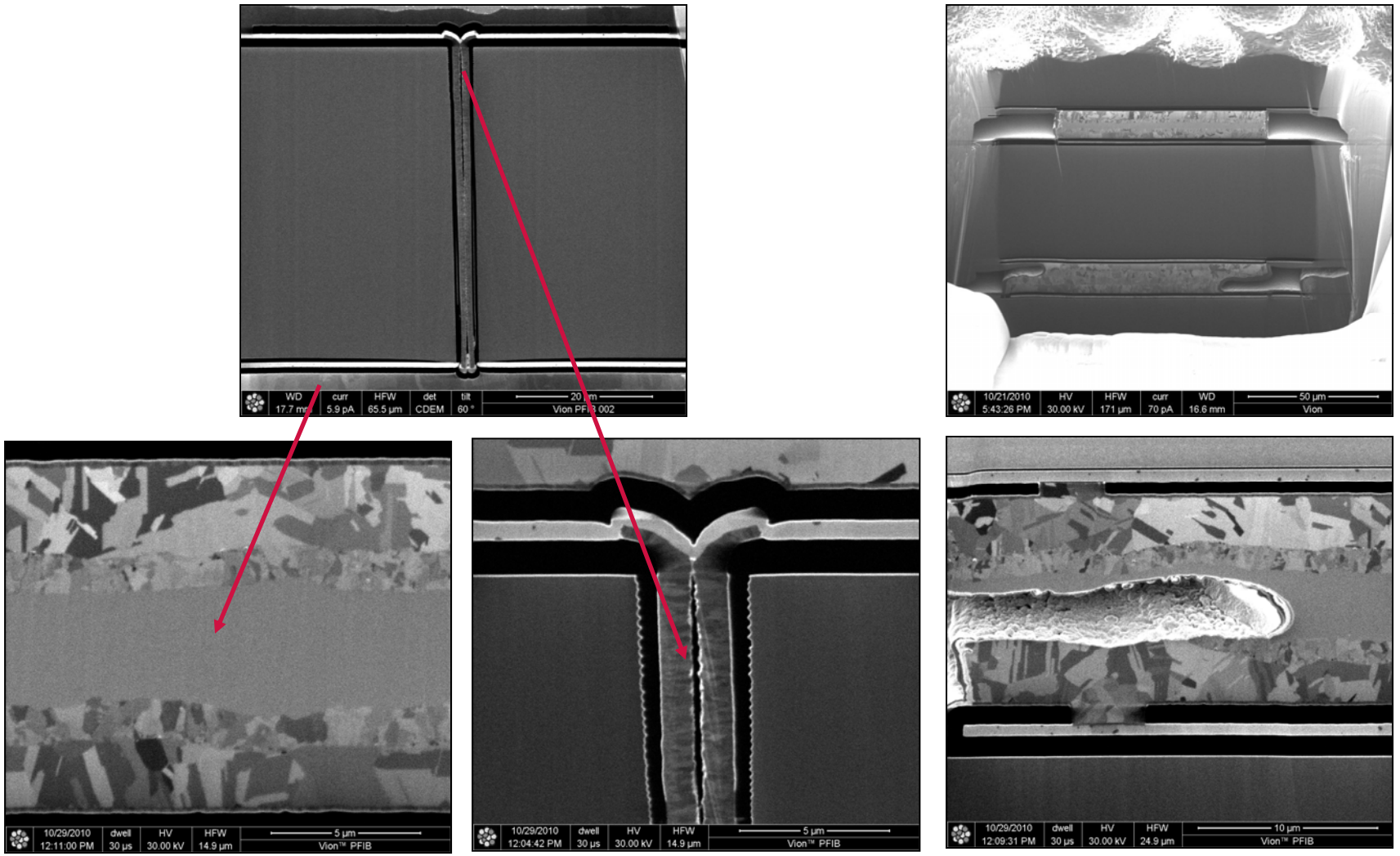
Layout of CMOS stress sensor devices in 3D TSV-integrated Topchip including TSV daisychain for yield analysis



Reliability Test Chip and Application of the novel FIB Analysis Technique



Failure Analysis of ICV-SLID Technology



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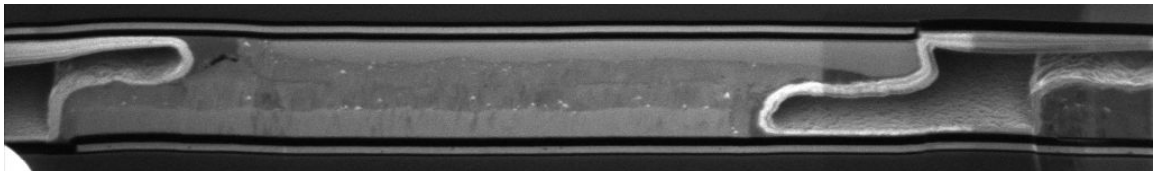


Asymmetric formation of intermetallic compound

Alignment and mechanical contact

above melting point

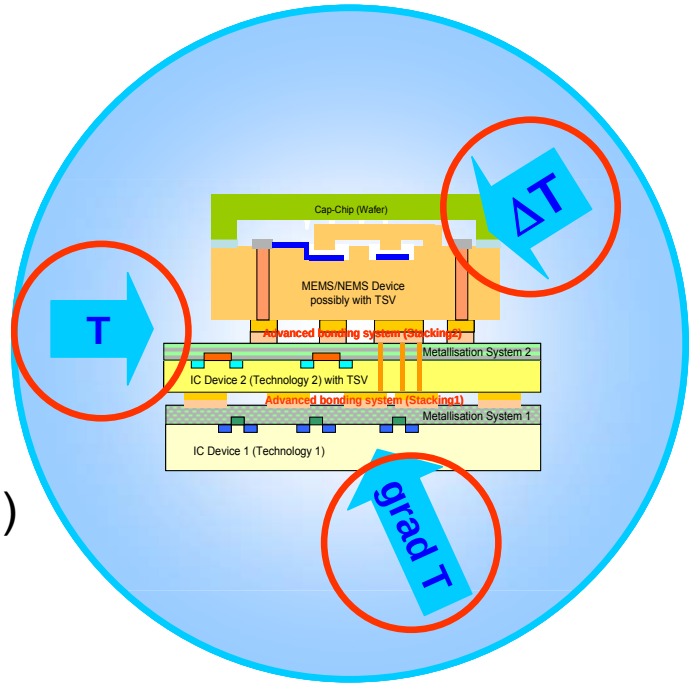
SLID intermetallic formation intermediate phase

SLID final state

New European Integrated Project
e-BRAINS
Best Reliable Ambient Intelligent Nanosensor Systems

supported by the European Commission
under support-no. ICT-257488

- Main objective of e-BRAINS: further research of selected e-CUBES technologies and implementation of new application specific technologies for heterogeneous integration of **complex advanced microsystems**
- Sophisticated new **nanosensor** systems
- 3D integrated **antennae** and **RF MEMS**
- **High Robustness and Reliability**
  - Fragile mechanical structures in MEMS/NEMS
  - Stress induced by TSV and bonding system
- Efficient **system design** support
  - Architectural design of heterogeneous systems
  - Tool set to predict functionality (incl. test devices)



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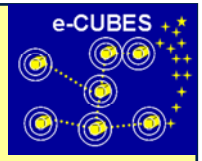
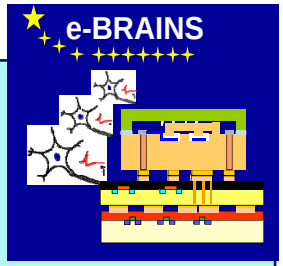
The e-BRAINS project will advantageously implement results from e-CUBES, especially the European 3D technology platform

e-CUBES



- 3D-SOC (with TSVs)
  - **Through Si Via (TSV) Technology (ICV-SLID)**
  - Hollow Via & Gold Stud Bump Bonding (HoViGo)
- 3D-WLP (without TSVs)
  - **Thin Chip Integration (TCI / UTCS)**
  - Via Belt Technology (µInsert)
- 3D-SiP (Stacking of packages)
  - HiPPiP
  - **Wirefree Die on Die Technology (WDoD)**
  - **Submicron Wire Anisotropic Condustive Film (SW-ACF)**

e-BRAINS



From technology to **system level**

Highly reliable and robust processes for high-performance nanosensor systems

3D heterogeneous system integration

- Low-temperature TSV-SLID (IMC)
- Low-temperature TSV-SWACF
- Low-cost TCI (without TSVs)
- Low-formfactor WDoD (Stacking of packages)
- Layer transfer bonding (Quantum wells integration)
- High-performance interposer (extreme fine TSV)

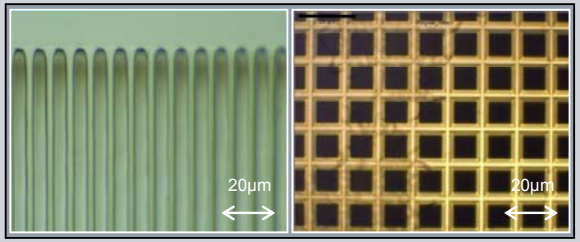
High Density Interposer
for High Performance 3D Systems

Center for Microsystem Integration Munich

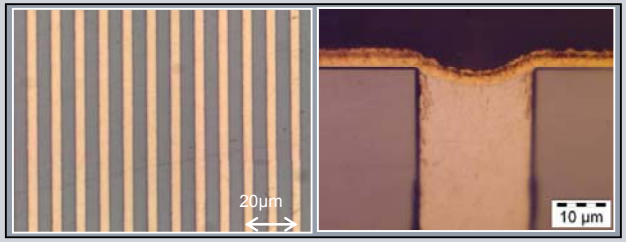
SIEMENS

Fraunhofer EMFT

Ultra Fine Pitch Silicon Etch



Via Fill by Liquid Conductor



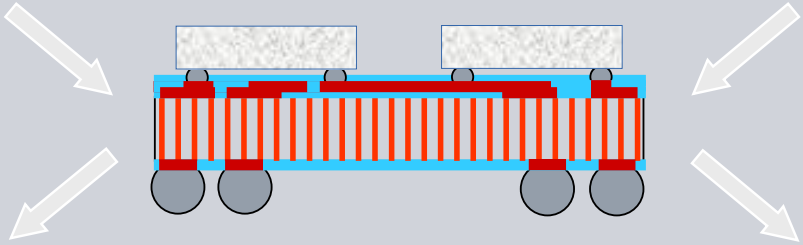


Photo Assisted Electrochemical Etch

- Fine pitch via array etch in Silicon
- Via diameter ~1… 30µm
- Via pitch ~1.2... 50µm
- Via depth → full wafer (!)
- Extreme exact and uniform
- Outstanding fine pitch technology

Liquid Pore Fill

- Fill of any buried pipeline system
- Pressing liquid metal into pores (batch)
- Fills across corners, overhangs,…
- Use of metal fillings (Alloys / Sn, Cu,..)
- No seed layer for processing
- Simple, low cost, high reliability

Conclusions

- **Motivations for 3D integration** are improvement of
  Form factor, integration density, performance and
  ➢ enabling of new heterogeneous systems.
- Choice of 3D technology depends on **cost-effectiveness, performance requirements** and **availability of devices**.
- **TSV technology** is considered today one of the most promising**, high-performant and small-formfactor 3D technologies.**
- **Robustness and reliability** of 3D fabrication processes are the **basic requirements !**
- Methods for corresponding assessments must be available
- **Physical failure analysis is essential** for implementation of 3D TSV products into fabrication.
- **Plasma FIB** is found an **efficient tool** for failure analysis and process development support.

Thank you for your attention !

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Acknowledgements to
the colleagues of the European projects, especially Reinhard Pufall (Infineon), Maaike Taklo (SINTEF), Max Fleischer (Siemens), Eric Beyne (IMEC), Pascal Couderc and Christian Val (3D-PLUS), Alan Mathewson (Tyndall), Bernhard Wunderle (TU Chemnitz) and Josef Weber (Fraunhofer EMFT)

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