High Temperature Silicon Carbide CMOS Integrated Circuits

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Abstract

The wide band-gap of Silicon Carbide makes it a material suitable for IC's [1] operating up to 450°C. The maximum operating temperature achieved will depend on the transistor technology selected, interconnect metallisation and device packaging. This paper describes transistor and circuit results achieved in SiC CMOS technology, where the major issue addressed is the gate dielectric performance.

N and p-channel MOSFET structures have been demonstrated operating at temperatures up to 400°C Test circuits including simple logic cells, ring oscillators, operational amplifiers and gate drive circuits have been fabricated and the characteristics of ring oscillators are presented here. Floating capacitor structures have also been fabricated for use in future analogue and mixed signal circuits.

This technology will be initially applied in applications including signal conditioning for sensors and control of SiC based power switching devices, where the high temperature capability will match that of the SiC power devices which are now becoming commercially available.

Introduction

In order to implement high temperature electronics, an integrated circuit (IC) technology capable of operation at temperatures substantially above those possible with conventional technology will be required. Silicon on insulator technology can operate well above the bulk silicon's maximum operating capability of 125°C today [3], but in order to exceed 300°C, a change to another semiconductor material will be required. In particular, drive circuits for Silicon Carbide power devices will be required to operate at high temperatures in order to obtain the maximum system benefit of reduced cooling. In addition, sensor interface circuits capable of operating above 300°C will be necessary in several automotive, aerospace and deep well drilling applications. CMOS is expected to provide benefits for high temperature design, in particular the ability to use auto zeroing techniques with switched capacitor filter circuits to accommodate parameter shifts with temperature or time. Therefore we demonstrate the first Silicon Carbide CMOS technology for logic and mixed signal IC designs.

Circuit Fabrication

CMOS test structures and test circuits described in [2] were fabricated on 100 mm, Si face, 4° off axis, 4H SiC n+ wafers with a doped epi layer, in which n and p-type well regions are formed by ion implantation. Source/drain regions for n-channel and p-channel devices are formed by further ion implantations as well as threshold voltage adjustments. All implants are annealed together at high temperature with the surface protected by a carbon cap. Thick field oxide and thin gate dielectric regions are then formed followed by doped polysilicon gate electrodes. Nickel based contacts are formed on the doped regions and a refractory metal interconnect is deposited and patterned. A thin Nickel top layer is finally applied to protect the pads from oxidation during probe testing at elevated temperatures. Finally an oxide layer is deposited for final passivation and scratch protection and openings made to the bond pads. A simplified cross section of the device is shown in Figure 1.

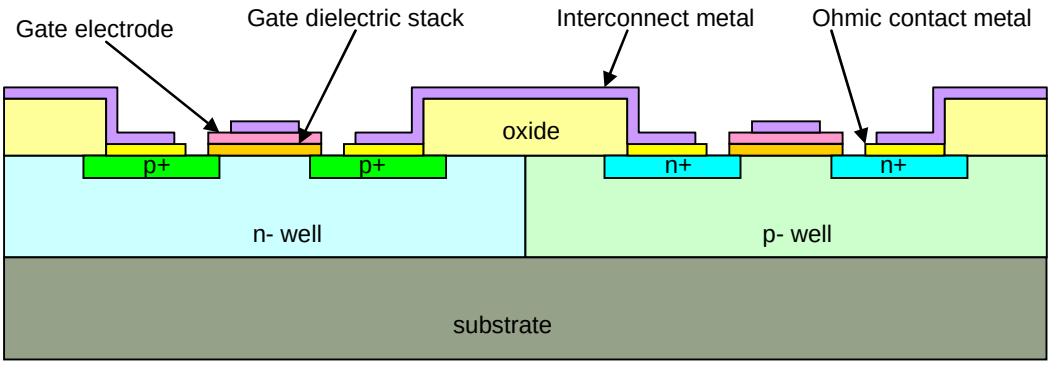

Figure 1. CMOS on SiC cross-section

Test Device Results

An extensive range of test structures including large area diodes, four terminal and bar resistors, contact test structures and transistors with a range of aspect ratios were fabricated on the same wafer. [4]. Layer doping levels were set to support 15V operation for temperatures up to 400C and hence diode breakdown voltages above 30V were required. Figure 2 shows diode reverse leakage as a function of temperature for p+/n- and n+/p- structures. The vertical punch-through voltage, from n+ drain to n+ substrate, constrains the voltage performance more strongly than the diode breakdowns but is still greater than 30V at 300°C as shown by the data in Figure 3.

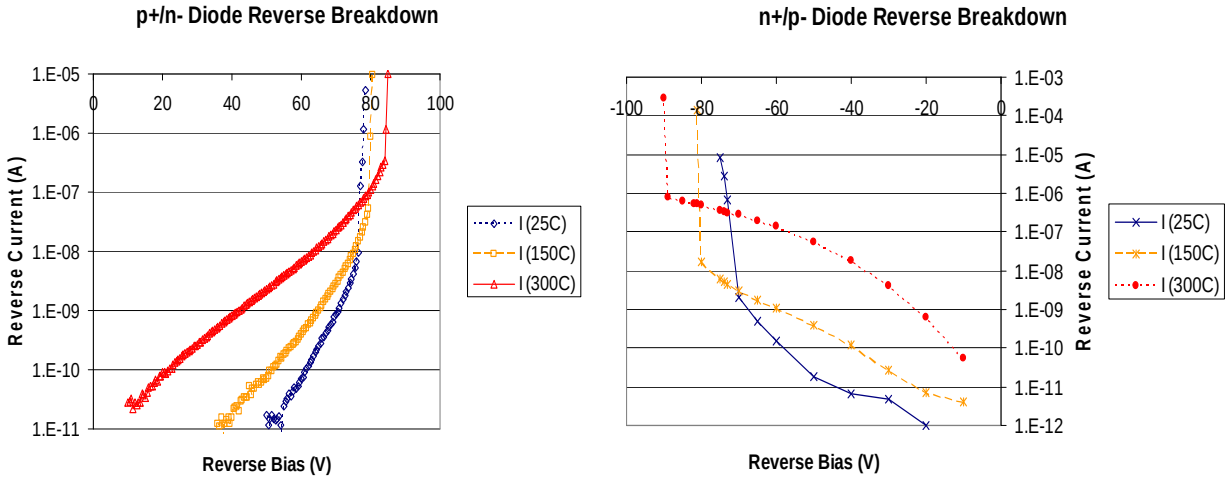

Figure 2. Diode reverse current vs. voltage and temperature for p+/n- and n+/p- diodes.

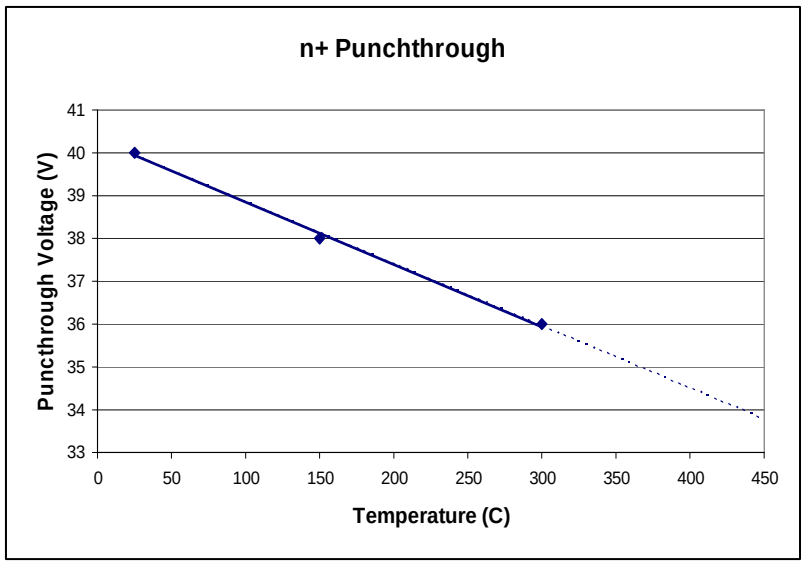

Figure 3. N+ drain to n+ substrate punch-through voltage vs. temperature

During operation, the gate dielectric has to withstand 15V stress at high temperature and ensure low leakage currents to minimise charge injection and degradation [5]. The dielectric also has to maximise that gate capacitance (Cox), to realise a high gain, as the channel mobility in SiC MOSFETS is known to be low [6]. We selected an Equivalent Oxide Thickness of 40 nm. as a compromise between minimising the leakage current and maintaining C_{OX}. The Gate leakage was less than 1pA up to at least 350°C, as shown in Figure 5.

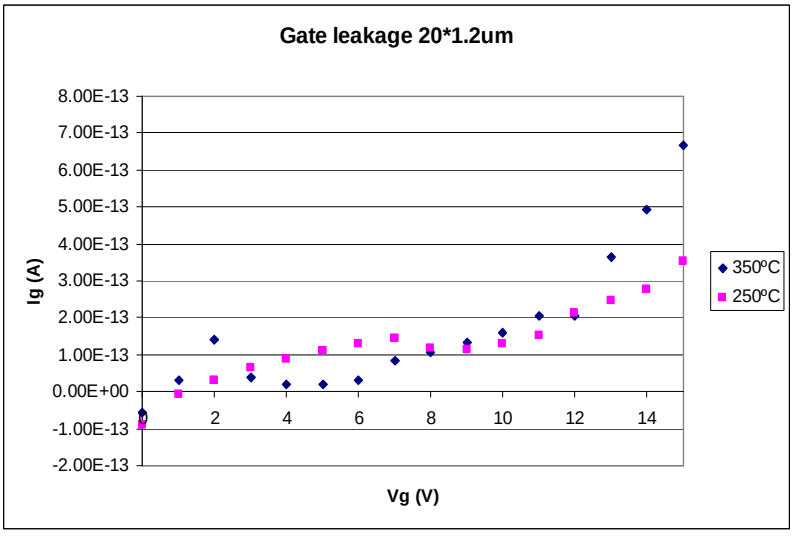

Figure 5 Gate current vs. gate voltage for a 20 x 1.2µm n-channel transistor

The transistors reported here are designed for 15V operation and channel lengths between 20 to 1.0 microns have been investigated. Short channel effects were observed on devices with gate lengths of 1.0 and 1.2 µm, but all devices continued to operate up to at least 350°C. Threshold voltages (V_T) were targeted at +/-5V for n and p-channel devices, to ensure a reasonable operating margin across the temperature range. N-channel devices show a strong temperature dependence, as shown by the data in Figure 6, while p-channel devices show a lesser temperature dependence, as shown in Figure 7. We expect the competing effects of shifts in V_T, Kprime and dopant activation across the temperature range to account for this behaviour. It is also apparent from the data presented in figures 6 and 7 that the metal/p+ contacts

are non-ideal at room temperature, but improve as the temperature rises. Further work is in progress to address this issue and further gate dielectric improvements are required to improve channel mobility and threshold voltage stability.

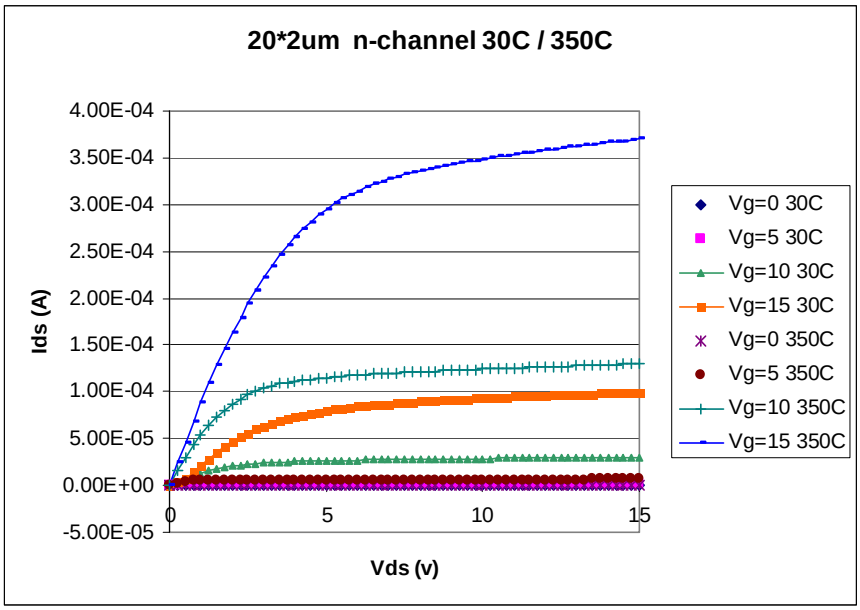

Figure 6 Ids vs. Vds at 30 and 350℃, for a 20 x 2µm n-channel transistor

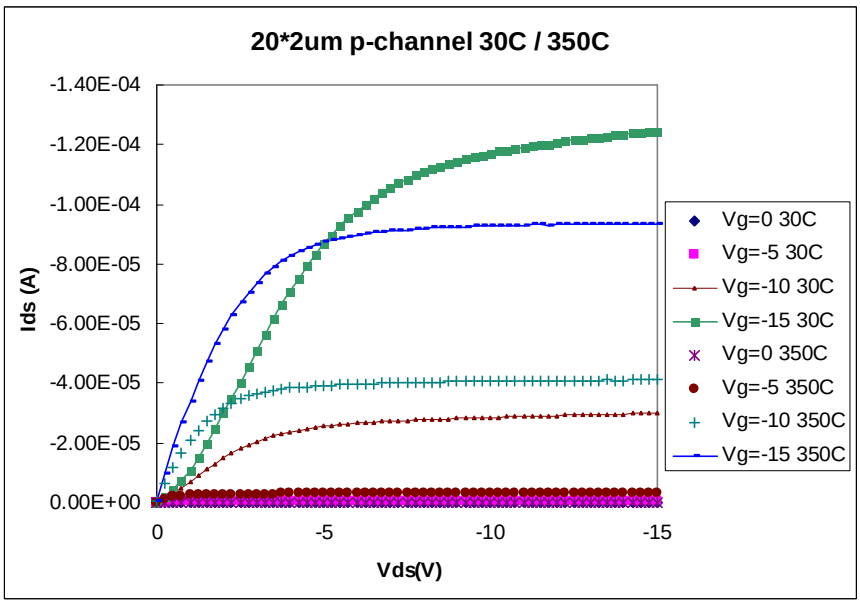

Figure 7 Ids vs. Vds at 30 and 350℃, for a 20 x 2µm p-channel transistor

In order to facilitate analogue and mixed signal design, in particular, switched capacitor circuits, we have formed floating capacitors on top of the thick field oxide. Initial devices are formed between polysilicon and metal, but future designs use a second layer of polysilicon, which also offers the possibility of high value floating resistors also for use in analogue circuits. We have measured the unit area capacitance at 0.70 fF. μm^2 and found it to vary less than +/- 1% over the range of 20°C to 400°C. Breakdown voltage was greater than 40v.

Test Circuit Results

A small range of test structures have been fabricated to date including ring oscillators, operational amplifiers and simple gate drive circuits. The ring oscillator consists of 401 stages including a reset, and contains ~900 transistors. Initial testing on wafer, at 300°C demonstrates operation with the output running at 15V and an extracted stage delay of 9.4 ns, as shown in Figure 8.

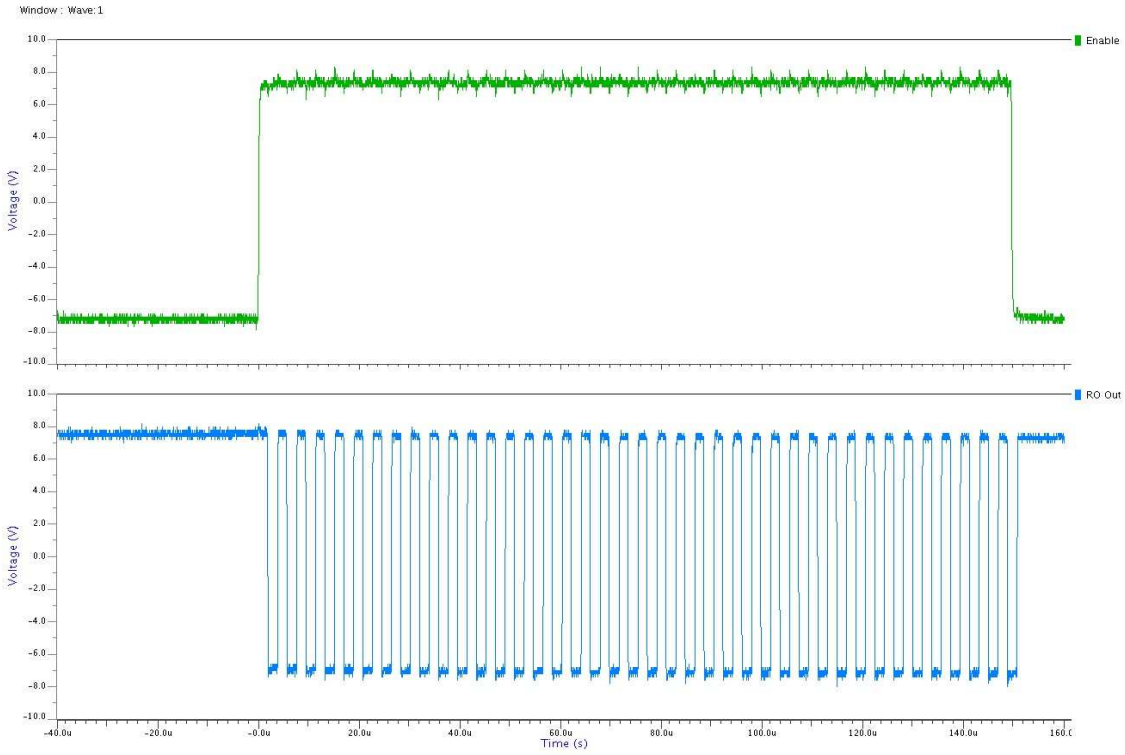

Figure 8 Upper trace - ring oscillator control signal, lower trace - ring oscillator output.

Conclusions

A CMOS process has been demonstrated on 4H SiC, through integrating multiple n and p channel transistors as an integrated circuit. Transistor operation has been shown up to 350°C with low gate leakage. Floating capacitors have been demonstrated operating up to 400°C. Test circuit functionality has been shown to 300°C. Future work will focus on increasing channel mobility by improving the structure of the gate dielectric and on improving the transistor stability, again through dielectric improvements.

Acknowledgments

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