HADES®: a High-Temperature Isolated Gate Driver Solution for SiC-based Multi-kW Converters

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Abstract

This paper presents HADES® Gate Driver, a new solution that efficiently drives Silicon-Carbide (SiC) devices in multi-kW converters. It discusses how it allows taking full advantage of SiC technology by placing the gate driver circuits very close to the power transistors: The resulting lower parasitic inductances enable faster switching times and subsequently higher efficiency. Higher operating temperature for both the gate driver and the power transistors also translate into considerable reduction of complexity, size and weight of the system, in particular of the cooling systems. Finally, the paper describes how HADES® reference design is built from a new chipset especially developed for this purpose and designed to operate up to 225°C: THEMIS, ATLAS and RHEA.

Keywords : High Temperature Electronics, Gate Driver, Power Converters, Motor Drive, Silicon-Carbide (SiC)

1. Introduction

Silicon Carbide (SiC) technology is gaining momentum with the recent announcement and the release of several new power transistors: MOSFETs [1], normally-Off [2] and normally-On JFETs [3], as well as BJTs [4]. These new SiC devices exhibit high-voltage capability, high-current density and very low switching losses thanks to very short turn-on and turn-off times. This later feature allows implementation of higher efficiency power converters and inverters compared to traditional silicon IGBT-based designs. Moreover, as the switching losses are greatly reduced, the designer can also increase the switching frequency which makes possible the use of much smaller passive and magnetic components, hence reducing the size and weight of the filtering circuits [3].

Another key advantage of SiC is its ability to operate at very high temperatures. This feature is paramount for applications where the ambient temperature is already high (e.g. in oil & gas down-hole tools or in aerospace, for actuators & motor drives close to aircraft engines or brakes). In less severe environment applications, this high temperature capability is also key as it allows to further reduce the complexity, size and weight of the systems: for instance in inverters or battery chargers for EV/HEVs, the fluid-cooling systems can either be simplified or purely removed as the junction temperatures of the power switches together with their drive-circuits can operate normally in the range 200~225°C.

In these applications, one of the biggest challenges is to drive the SiC transistor properly in order to take the full advantage of their very short switching times. But there is another issue: each SiC device type has its own gate drive specificities that require the driving circuitry to be specifically tailored. All these requirements make most of the existing silicon gate driver ICs at best unpractical, and more often unusable. CISSOID has developed a versatile isolated gate driver chipset and a reference design called HADES® (see) which brings a technological answer to all these issues.

HADES® is based on 3 new high temperature ICs: THEMIS, ATLAS and RHEA. As these ICs operate normally up to 225°C, they can be located very close to the SiC power transistor, or inside the power module, minimizing the parasitic inductances and then further reducing switching times and associated dynamic losses.

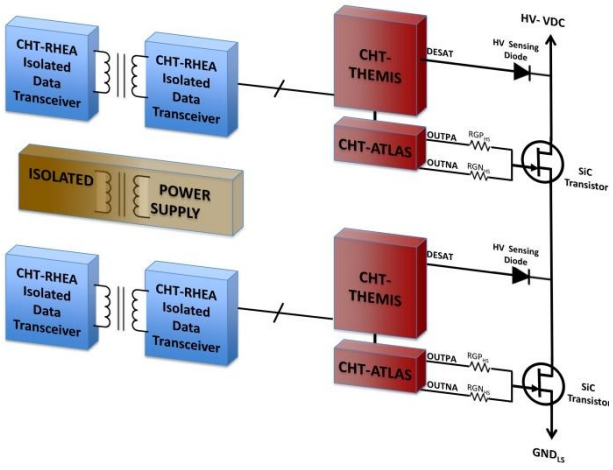

Figure 1. HADES® High Temperature Gate Driver

2. HADES® Gate Driver

As shown in Figure 1, HADES® gate driver includes high-side and low-side floating drivers, each of them being based on one THEMIS, one ATLAS and two RHEA chips. THEMIS includes the control and the protection functions. ATLAS is a push-pull driver stage able to sink or source up to 4A to the gate of the power switches. THEMIS controller takes care of the voltages and timing generation as well as the control logic that manages the exchange of control inputs and fault detection with the host controller. All the signals exchanged with the host are galvanically isolated through RHEA (2.5kVDC isolation), a dual-channel transceiver which implements a 2MBit/s data transmission through a tiny pulse transformer. High immunity to dV/dt (up to 50kV/µs) is achieved. The floating low-side and high-side drivers can be supplied by an isolated DC-DC converter also optimized for high robustness to dV/dt.

3. THEMIS/ATLAS Power Transistor Driver

In this study, silicon carbide Power MOSFET CMF20120D from CREE have been used. The Figure 2 shows the specific hardware configuration and electrical schematic using THEMIS and ATLAS driver chipset for this power switch type. The solution supports other types of SiC and silicon switches [5, 6 and 7] with specific hardware changes.

The driver controller THEMIS integrates all the necessary functions to detect faults such as power supply fault detection (built-in under-voltage lockout comparator) and desaturation detection of the power transistor, through the monitoring of the drain-to-source voltage with a comparator. THEMIS' control logic manages the interrupt signals from the fault comparators, masking the input signal and sending back flags to the host controller in case of faults. THEMIS also includes three pre-driver stages: one for the input PWM signal, and one that can typically be used when the power device requires a specific current profile in order to be properly turned-on (e.g. need to generate a short pulse when turning-on some normally-off SiC JFETs). A third pre-driver generates an inverted and delayed signal for the driving of an external MOSFET for the Active Miller Clamping function. Concerning the local power supply, the THEMIS' built-in 5V voltage regulator supplies the control logic, the pre-drivers and the external ATLAS circuit. It can also supply the 5V to some external circuitry such as the secondary RHEA in HADES® implementation.

The driver circuit ATLAS includes two independent 2A push-pull stage channels. These two channels can be put in parallel in order to provide up to 4A output current

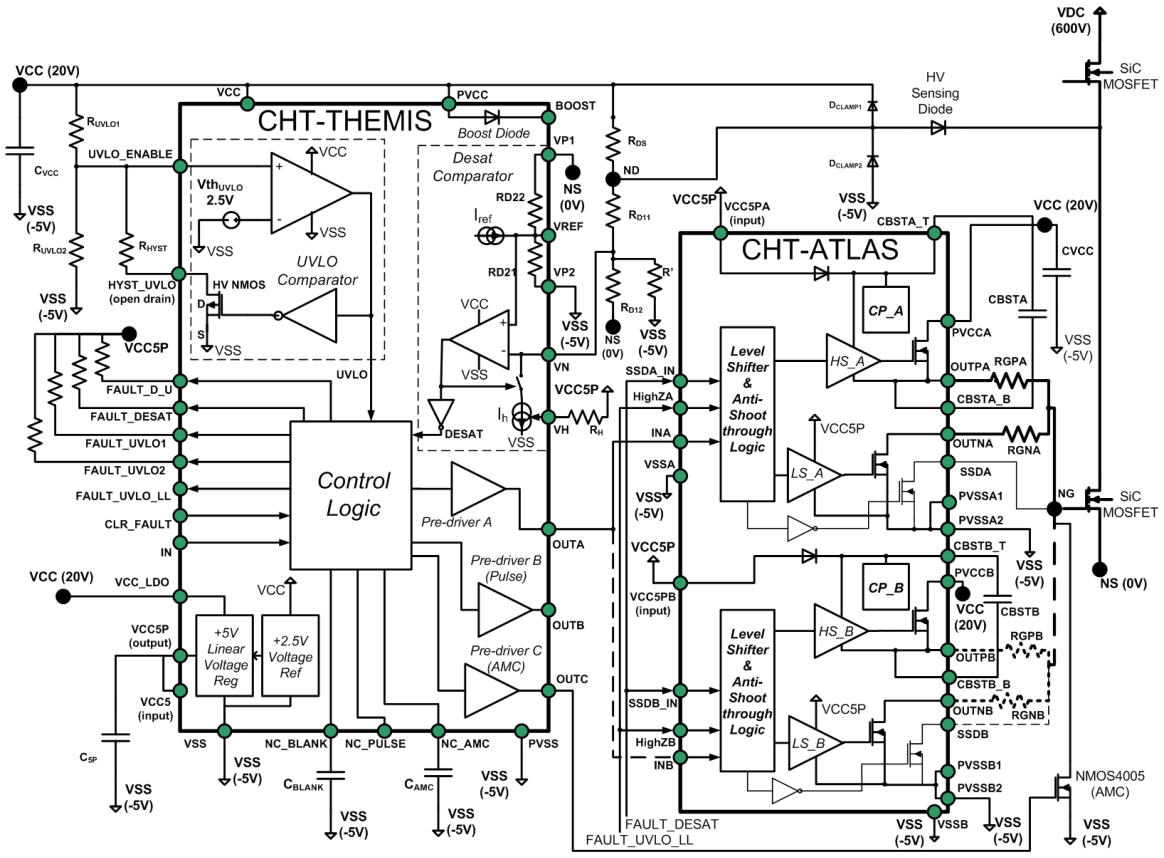

Figure 2. THEMIS and ATLAS driving a SiC Power MOSFET

to the gate of the power transistor. Output sink and source transistors are two N-channel high voltage MOSFETs. The transistor sourcing current is driven by a level-shifter and supplied by a bootstrap capacitor and diode. A non-overlapping logic avoids shoot-through between the sink and source output transistors. An internal charge-pump circuit starts charging the bootstrap capacitor when the voltage across it is too low, enabling 100% duty cycle operation. An internal soft-shutdown transistor is also available to smoothly discharge the gate of the power transistor in case of fault (desaturation). The outputs of ATLAS can be also put in high impedance via the HighZx inputs.

It must be noted that up to 5 ATLAS chips can be controlled in parallel, bringing the output current up to 20A for use in very high power converters.

3.1 Measurements results on THEMIS

Figure 3 to Figure 6 shows several characterization results for THEMIS chip. Figure 3 shows the very good stability of the Undervoltage lockout (UVLO) comparator threshold voltage versus temperature, within +/-1% with respect to the value at 25°C. Figure 4 illustrates the even better stability of the desaturation comparator threshold voltage versus temperature. The line regulation of THEMIS internal linear regulator at different temperature can be seen in Figure 5.

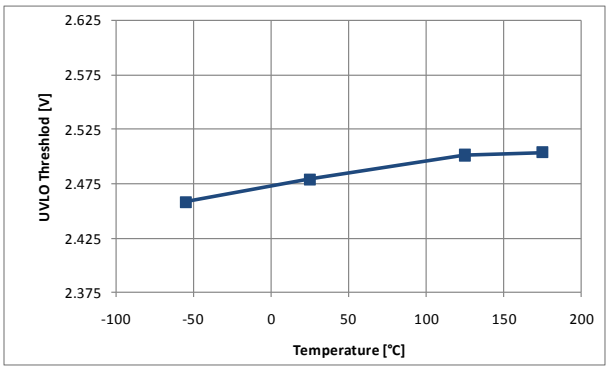

Figure 3. Undervoltage lockout (UVLO) comparator threshold voltage versus temperature

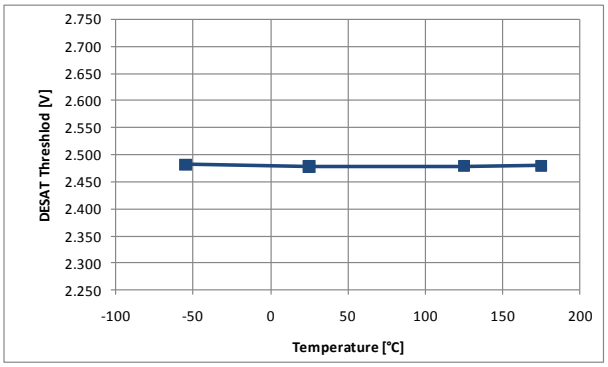

Figure 4. Desaturation comparator threshold voltage versus temperature

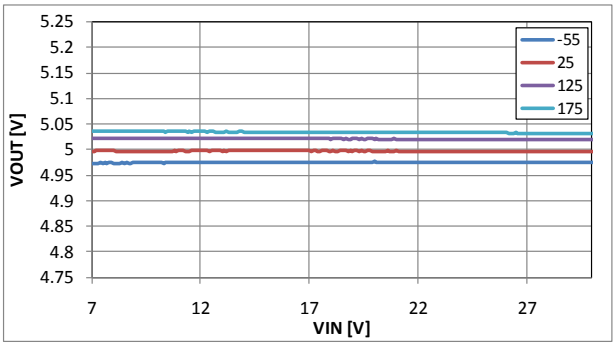

Figure 5. 5V linear voltage regulator line regulation at different temperatures

Finally, the Figure 6 shows the stability of the Active Miller Clamping delays as a function of the temperature. In this last case, design techniques have been used in order to reduce the influence of temperature drift of on-chip components.

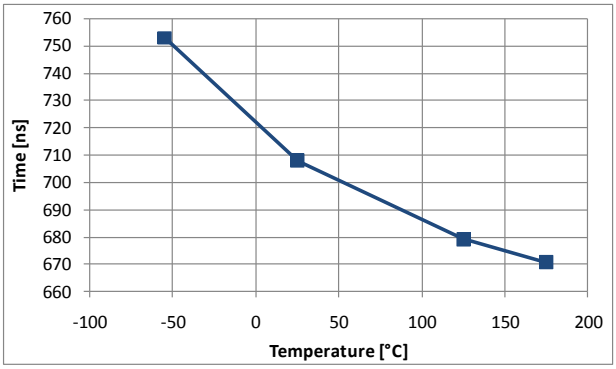

Figure 6. Active Miller Clamping delay versus temperature

3.2 Measured ATLAS performances

Figure 7 and Figure 8 show respectively the low and high output state resistance of one ATLAS channel versus temperature. Figure 9 and Figure 10 illustrate the sink and source current as a function of the temperature.

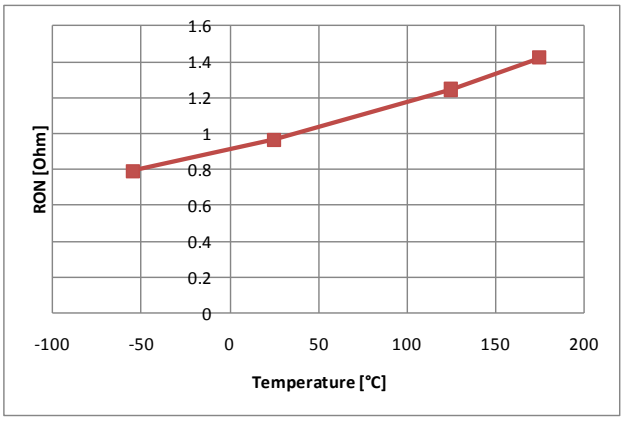

Figure 7. Low state output resistance vs temperature (for a single ATLAS channel)

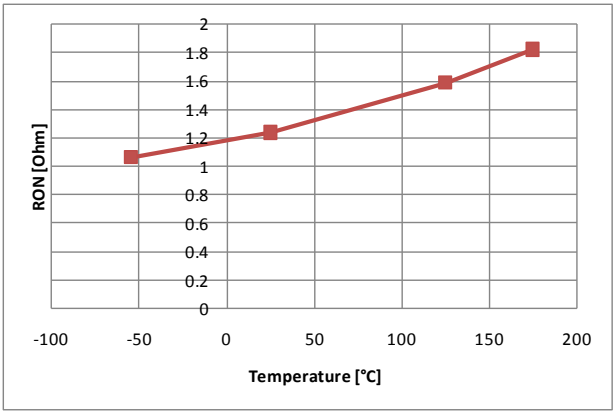

Figure 8. High state output resistance vs temperature (for a single ATLAS channel)

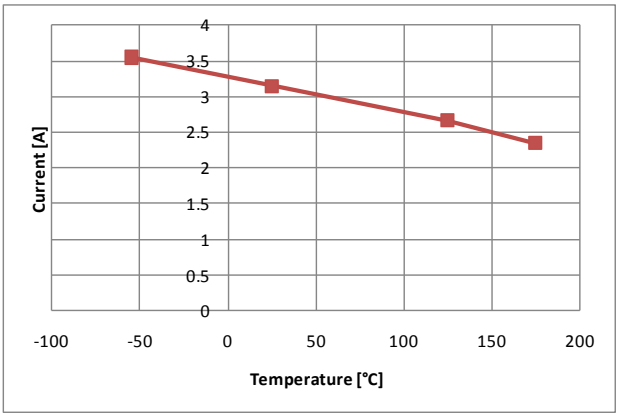

Figure 9. Sink output current versus temperature (for a single ATLAS channel)

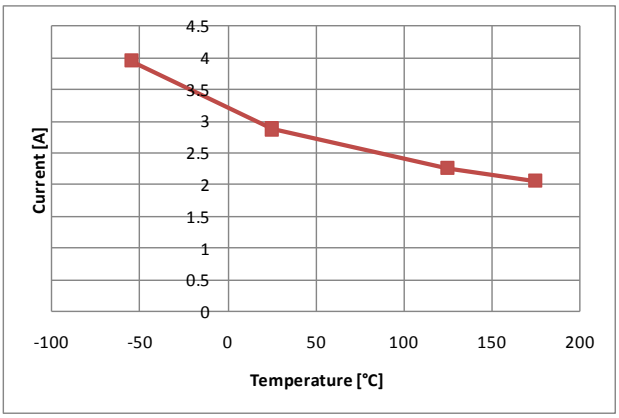

Figure 10. Source output current versus temperature (for a single ATLAS channel)

3.3 Measurement results on THEMIS/ATLAS driver board

In order to validate the operation of THEMIS and ATLAS as a power transistor driver, an evaluation board has been developed (see Figure 11). Together with ATLAS and THEMIS, the board implements a high temperature power transistor for the Active Miller Clamping function.

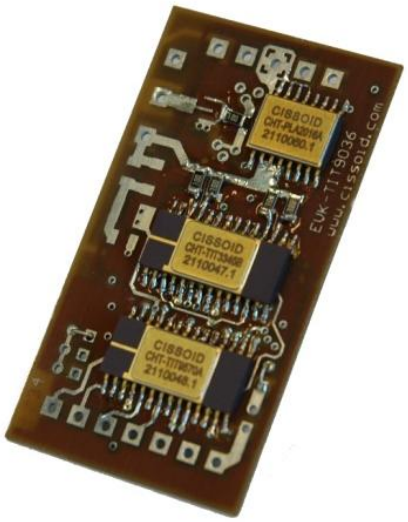

Figure 11. THEMIS/ATLAS driver evaluation board

The board has been characterized in a well-known "double pulse" measurement setup (Figure 12). The current in the inductor rises during the first on time until the desired value. The fall time is measured at the turn off after the first pulse while the rise time is measured at the turn on of the second pulse.

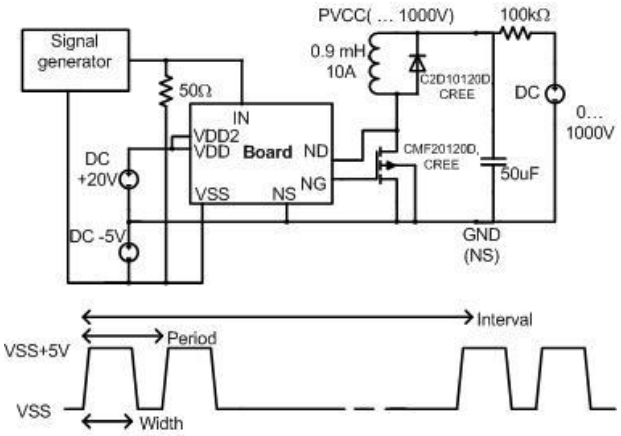

Figure 12. Double pulse measurement setup

The Figure 13 shows the turn-off when driving a 20A SiC MOSFET from Cree (CMF20120D). The high DC voltage is equal to 450V and the switched current is 5A. The THEMIS/ATLAS driver turn-off delay (from Control to SiC Gate) is typically equal to 35ns at room temperature and increase up to 55ns at high temperature. The SiC MOSFET turn-off delay is 40ns and the rise time is 20ns at room temperature.

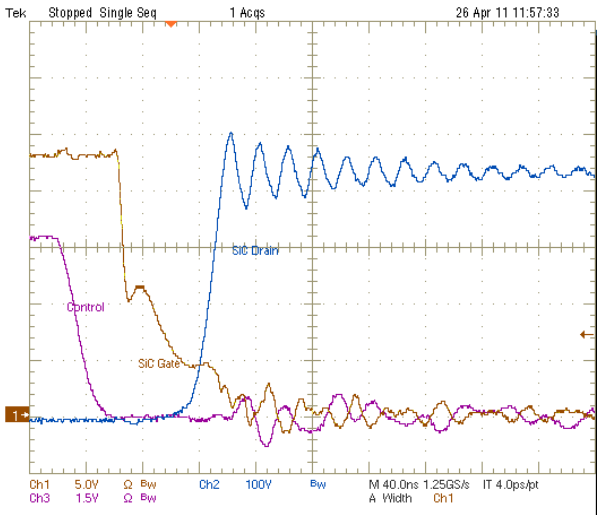

Figure 13: Turn-off of SiC MOSFET CMF20120D at 5A, 450V

The Figure 14 shows the turn-on in the same conditions. The THEMIS/ATLAS driver turn-on delay (from Control to SiC Gate) is typically equal to 50ns at room temperature and increase up to 75ns at high temperature. The SiC MOSFET turn-on delay is 25ns and the fall time is 30ns at room temperature.

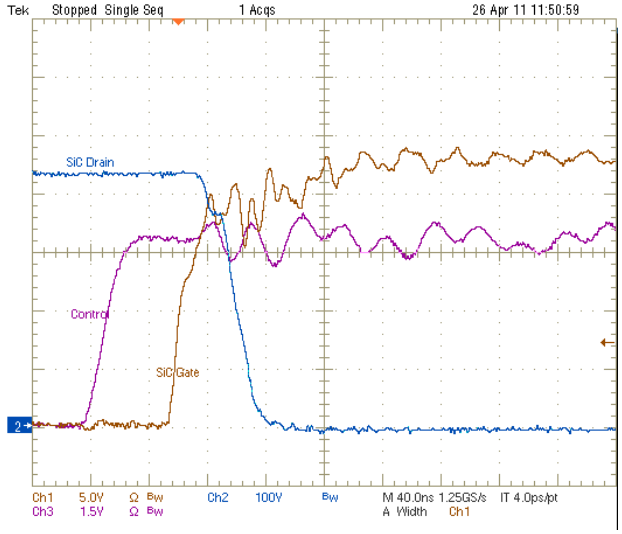

Figure 14: Turn-on of SiC MOSFET CMF20120D at 5A, 450V

4. RHEA isolated data transceiver

RHEA is a high-temperature IC that implements a dual-channel full duplex isolated data transceiver. It provides a galvanically isolated signal transmission. The galvanic isolation is achieved by means of a small external pulse transformer for each digital signal. The chip integrates in a single package 2 transceivers (2 transmit and 2 receive channels) as shown in Figure 15.

In HADES®, RHEA is used to transmit the PWM and Clear Fault signals to THEMIS and to send back to the transmitter the UVLO and DESAT fault signals. The solution has been optimized to minimize the size of the transformer and the number of external components, hence the HADES® board footprint. The transmission delay (<120ns) has been minimized in order to reduce the total transmission delay through the complete gate driver. Finally, as HADES® high side-driver is floating with high dV/dt (typically up to 50kV/µs), the architecture has been used to maximize the noise margin in such harsh conditions.

Each transmit channel (Tx) implements a modulation block using a circuit's built-in clock generator, which frequency can be programmed with one among 8 different values inside the range [6-20 MHz] as shown in Figure 16 for different temperature. Each receive channel (Rx) demodulates the signal coming from the transformer. The data transmission rate is up to 2 Mbit/s. During power-up of the circuit, the output signals can be forced to the 0 state through the control input pin ENABLE.

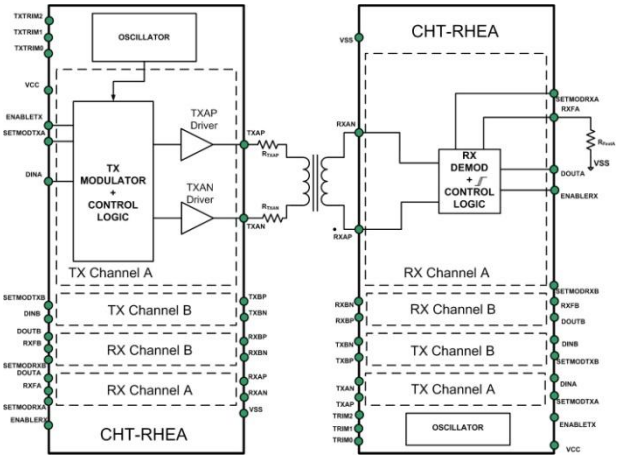

Figure 15: RHEA high temperature data transceiver with highlight on one transmission channel.

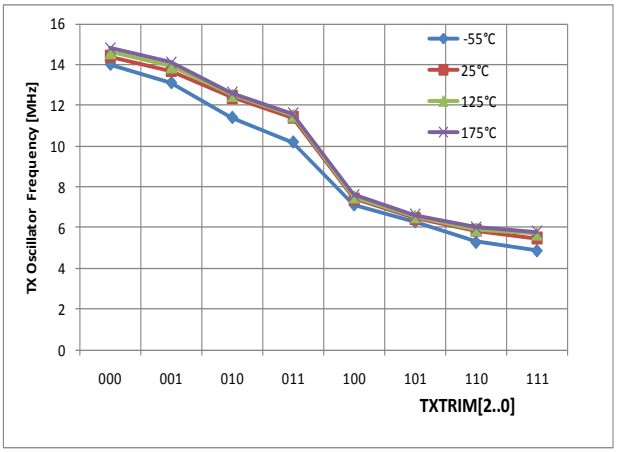

Figure 16 : TX Oscillator Frequency versus TXTRIM[2..0] configuration bits and temperature

In order to validate the operation of RHEA and characterize its performances, an evaluation board has been developed (Figure 17).

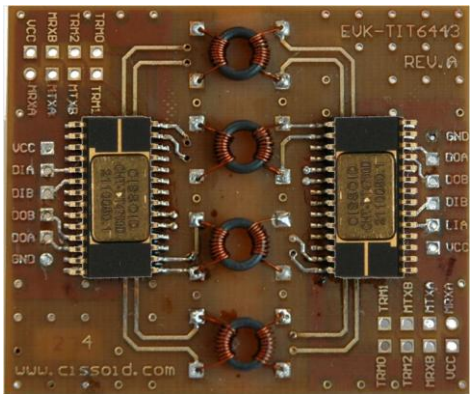

Figure 17: RHEA high temperature evaluation board

Figure 18 and Figure 19 show the measurement of the propagation delay through one RHEA channel (TX+RX) respectively for rising and falling edges. Both delays are below 100ns. Figure 20 and Figure 21 show the peak-to-peak jitter for rising and falling edges that is typically between 10ns and 20ns, depending on transmission frequency and temperature.

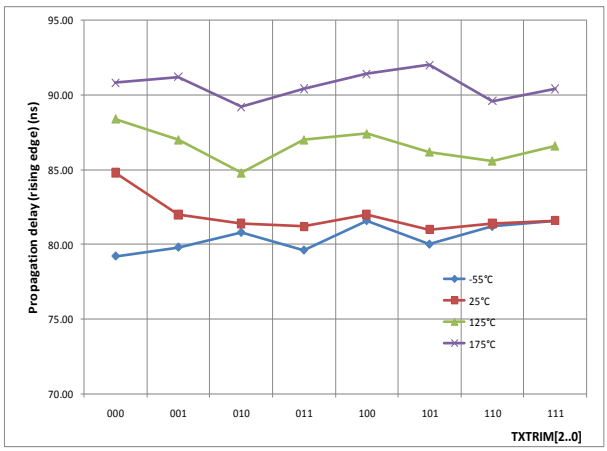

Figure 18: Propagation delay (rising edge) vs. TXTRIM[2..0] configuration bits and temperature

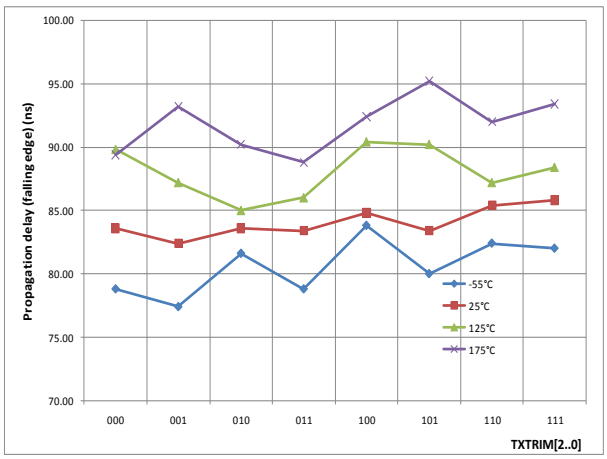

Figure 19: Propagation delay (falling edge) vs. TXTRIM[2..0] configuration bits and temperature

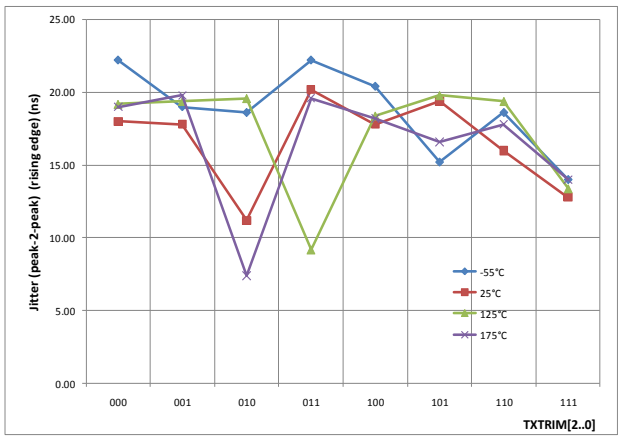

Figure 20: Jitter (peak-2-peak) (rising edge) vs. TXTRIM[2..0] configuration bits and temperature

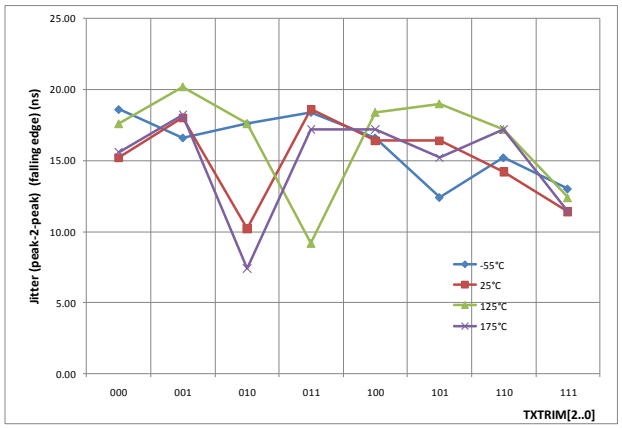

Figure 21: Jitter (peak-2-peak) (falling edge) vs. TXTRIM[2..0] configuration bits and temperature

5. Conclusions

This study show-cased the new CISSOID high-temperature integrated circuits THEMIS, ATLAS and RHEA and the possibility to combine them in a complete isolated gate driver implementation called HADES®. The test vehicle was based on the SiC MOSFET CMF20120D from CREE. The goal of this study was to demonstrate the ability of the solution to bring:

- A seamless SiC gate drive circuitry directly accessible from a generic host,
- The ability to switch dramatically faster than traditional gate-drive / IGBT implementations,
- The ability to run normally and reliability at temperatures above existing solutions today.

Seamless driving circuitry for SiC is clearly achieved: from an electrical function perspective, the evaluation boards were designed and optimized in order to reach performance similar to the traditional gate-driver boards that are commonly used in the industry for IGBT switches and modules. All the features typically

implemented in such boards are supported by HADES®: 2.5kVDC galvanic isolation between the host and the high-voltage load; a power supply with undervoltage lockout protection; high immunity to dV/dt; active miller clamping; desaturation detection.

Concerning the switching time, the solution exhibits very short rise-time / fall times, which translates into lower losses and hence allows higher switching frequencies with respect to traditional IGBT converters. These aspects are needed primarily when focusing on the reduction of the size of the passive and magnetic components of the power converters.

In regards to the operating temperature, the results show an outstanding stability of the functions on the full temperature range. This opens the door to multi-chip module implementations where both the power transistor(s) and the driver dice can be assembled together, minimizing the parasitic inductances and running at the same junction temperature. The Intelligent Power Modules (IPMs) can now be realized combining both silicon carbide and high-temperature Silicon technology, with an operating junction temperature of up to 225°C. As a result, the system will need dramatically reduced cooling systems. An immediate application is with Hybrid Vehicles (HEVs) where the power electronics can now be cooled from the primary cooling system (i.e. the fluid coming from the thermal engine, typically slightly above 100°C), bringing a significant advantage over the existing implementations that require a secondary cooling system for the electronics with a fluid running at 60~85°C.

The last compelling advantage of the combination of HADES® + SiC technology is about the reliability and lifetime expectancy: Even though these aspects were not addressed in this paper, the Silicon technology used for HADES® integrated circuits was already proven to provide lifetimes above 20 years when running at 125°C, and above 5 years at 225°C. None of the existing standard silicon components can even approach such figures, which are compelling advantages for a number of applications such as aeronautics, or in solar converters where the lifetime goals can be in the range 20 to 30 years. Such figures can be achieved with HADES®.

Silicon carbide technology paradigm is full of promises for the power electronic industry: It combines high-current density, high voltage support, lower switching losses, high frequency capability, and high temperature junction capability. But is the surrounding ecosystem ready to support such features? The high power density and the low dynamic losses are intrinsic to the SiC devices. We have seen in the past 2 years a significant increase of advanced R&D programs focusing on these 2 aspects: Leading universities, research laboratories and advanced R&D groups of various companies already demonstrated efficiency gains for solar power converters or inverters for electric vehicles or aeronautics with figures above 98% and even 99%. Such an efficiency gain could be obtained in the power converters mainly by replacing the IGBTs by some SiCs, but keeping the same surrounding components and architectures. The vast majority of these R&D programs were using traditional gate-drive circuits, i.e. made from standard silicon, typically limited to 85°C operation. As a result, they had either to keep the driver remote – to the detriment of the parasitic inductance and therefore unable to increase the switching frequency – or to place the driver close to the SiC switch but then having to keep a large, oversized- and complex cooling system in order to keep the junction temperature sustainable by the driver, …whereas the junction of the SiC could go much higher. None of these solutions are viable if the design goals also include weight and size reduction, or the increase of the switching frequency. As shown in this paper, HADES® is an enabling technology for SiC switches. Thanks to HADES® , the trade-off switching frequency / efficiency / operating temperature / reliability / size (and weight) of the SiC-based systems is no longer dictated by the constraint of the existing components, but it is now a deliberate choice of the designer depending on what his design goals are.

Silicon carbide combined with high-temperature HADES® is not only a solution of choice for advanced developments; it is a disruptive technology that uniquely allows the shrinking of the power converters, removing the fluid cooling, while achieving efficiency gains when needed.

6. References

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