Fabrication of an electrostatically actuated impingement cooling device

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Abstract

This paper reports on the fabrication and characterization of an electrostatically actuated liquid droplet, impingement cooling device. The continuous increase of IC power density and the widespread use of 3D integration call for advanced cooling techniques. These are necessary to keep the device temperature low and to improve the reliability. Here we propose a 3D cooling device in which droplets are electrostatically actuated through vertical channels and impinge on an IC surface. The channels are formed by stacking thinned perforated silicon dice. By means of DRIE, vias with diameters ranging from 100 μm to 300 μm are etched into a low resistivity 200 mm silicon wafer. Further processing involves passivation with oxide, contact opening, bonding to a carrier wafer and grinding. Finally, stacking of the dies is achieved by debonding individual dies from the carrier wafer and bonding the first die to a silicon base. A second die is then aligned and bonded on top of the first one, and this operation is repeated a third and fourth time so as to create a "tower of Hanoi" structure. The preliminary results on the electro wetting properties of this device are reported.

Keywords: (1) Silicon micro-fabrication, (2) electrowetting, (3) electronic cooling, (4) stacking

Introduction

Performance and reliability of electronic products require a tight control on the temperatures and temperature gradients of their components [1]. Because of the continuous increase of single IC power density and because of the ever increasing use of 3D integration technology, effective removal of the heat dissipated by the electronic devices becomes more challenging. When the power generated by the electronic circuit exceeds approximately 100 W/cm^2, conventional cooling methods, such as natural convection or fan-induced air-cooling, are no longer effective at maintaining device temperatures below the operational limits. Therefore, more advanced cooling methodologies such as those based on liquid flow in microchannels, and eventually two-phase, liquid-vapor phase change (*i.e.*, flow boiling) in microchannels, may become necessary [2]. Cooling of 3D integrated, stacked packages provides further thermal management challenges. Recent studies [3, 4] pointed out that an efficient microchannel cooling plate mounted on top of a stacked package is not a sufficient thermal management solution, and complex interlayer cooling strategies might become necessary.

The most common and straightforward approach to liquid cooling of integrated circuits, was proposed in the early 1980's [5]. It was based on microchannels aligned parallel to the surface to be cooled; heat flows up to about 1000 W/cm^2 can be removed using a sufficiently high liquid flow rate, forced into the small hydraulic diameter channels. The main drawback of this approach is the large pressure drop across the channels. A large external pump is therefore required to overcome this large pressure drop. Micropumps integrated into a microchannel cooling device have also been proposed as an alternative to external pumping [6, 7, 8]; although their effectiveness has never been proven in a fully functional cooling device. A second drawback of the parallel microchannel configuration is that the liquid heats up and a large temperature gradient develops across the IC circuit as the liquid is transported through the cooler. This gradient can be minimized by increasing the flow rate at the expense of further increasing the operational pressure drop. A third inconvenience of parallel microchannel coolers is that the coolant flow rate cannot easily be adapted to match the cooling requirements of local hot spots (both spatial and temporal).

An alternative approach to parallel channel cooling consists of implementing a large number of channels in an impingement orientation (*i.e.*, perpendicular to the surface to be cooled). This option is in general more complex from the point of view of fabrication but requires smaller operating pressures and provides a more uniform temperature over the device to be cooled. Various implementations of this concept have been presented in the literature [9, 10]. However, generating the pressure required for pumping the fluid still requires an external pump and tailoring the flow rate in individual channels according to the locations of hot spots remains a challenge.

In this paper a vertical flow cooling system based on electrowetting is presented. The proposed cooling strategy involves electrical actuation of liquid droplets in vertical channels which impinge on an IC surface. The electrical actuation serves as an integrated pumping mechanism. The electrical actuation also provides the possibility of individually controlling the droplet flow rates in specific regions of the chip to mitigate hot spots. Thus, such a cooling scheme has the potential to solve the open issues mentioned previously. The paper is organized as follows: (1) the concept of the electrowetting vertical cooling system is described, (2) the fabrication process flow and the results of the fabrication are presented, and (3) the preliminary experimental characterization of the electrowetting device is described.

Device concept

The proposed cooler is based on the electrostatic actuation of droplets in a channel, obtained by applying a voltage at consecutive electrodes integrated in the channels and insulated from the liquid by a dielectric layer. This actuation technique, known as electrowetting on dielectric [11, 12], has previously been proposed as a cooling strategy in cases where the coolant moves parallel to the electronic component [13-17]; but, as far as the authors are aware, it has never been demonstrated in a vertical impingement microchannel cooler.

A schematic representation of the proposed vertical channel cooler is shown in Fig. 1a. Individual liquid droplets, electrostatically actuated downwards through the vertical channels, impinge on the chip surface and after exchanging heat with the IC, are then transported upwards by electrostatic actuation. If the cooler is used in a two-phase mode, where the coolant evaporates completely while in contact with the chip surface, then the vapor will

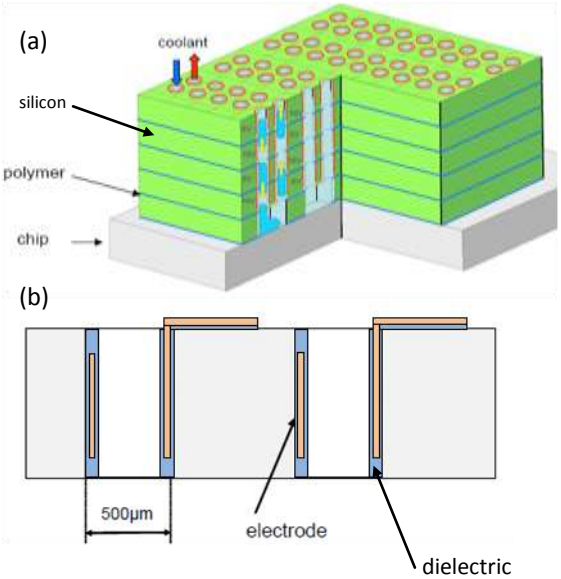

Figure 1: a) Schematic representation of the electrowetting based vertical channel cooler. b) Schematic cross section of the individual layer.

leave the surface by diffusion, and there is no need of an electrostatic upward force.

The cooler is formed of a stack of layers; typically silicon layers about 150 µm thick. Each layer is perforated and the walls of the hole are coated by an insulating layer with an embedded metal contact acting as electrode (see Fig. 1b). The metal layers are routed to the periphery of the chip in such a way that a voltage can be easily applied to each electrode independently. Layers are stacked on top of each other by using a polymer adhesive, in such a way that the holes form a plurality of vertical microchannels. The polymer layer also provides electrical insulation of the silicon layers. By this construction, vertical microchannels are formed, each having a series of electrodes which can be used to transport droplets by electrostatic actuation along the channel itself. The stacked layers are attached to the chip to be cooled. The resulting device combines the fluidic microchannels with an integrated pump.

In a previous publication, the physical model of the device has been described in detail [18]. According to the model, up to 100 W/cm^2 can be removed by the described device when operating in single-phase liquid mode (*i.e.*, no evaporation). The heat removal rate can be further increased if the device is operated in such a way that the droplets evaporate when arriving in contacts with the silicon chip.

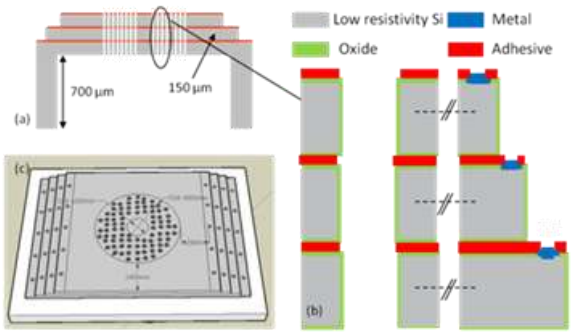

Figure 2: Proposed simplified test device: (a) cross-sectional image, (b) close-up view of the stack showing different components including silicon, oxide, metal and adhesive, and (c) schematic 3D view of the final device.

In this paper, we present a simplified version of this device, whose cross sections and 3D schematics are shown in Fig. 2. The four stacked layers are made of low resistivity silicon (5 mΩ/cm). The horizontal extents (or width) of each chip layer increases from top to bottom as seen in Fig. 2. The large silicon conductivity allows controlling the potential around each section of the channel without implementing a complex metal routing scheme for the actuation electrodes while the variable silicon chip layer width allows contacting each layer without the use of through silicon vias (TSV).

The simplified version can be more easily fabricated while still allowing for the study of electrically actuated droplets in a vertical microchannel. However, control of individual channels cannot be achieved using this simplified fabrication process; furthermore, only unidirectional flow is possible.

Process flow

The fabrication can be divided into three main blocks: a) the base holder, b) the device die, and c) the dice assembly. The process flow for each block is described in this section.

The base holder is simply a silicon die with approximate dimensions of 2 cm x 2 cm and having in the center a hole of a few mm diameter. The base acts as a reservoir for the coolant and as a support for the final assembly. The process flow for its fabrication is straightforward: a 200 mm full thickness wafer is bonded on a carrier wafer by means of temporary glue. Lithography is performed to define the circular structure which is then deep reactive ion etched down to the interface with the carrier wafer. Resist is stripped, the temporary glue is removed, and base holders of appropriate dimensions are diced.

The process flow for the device wafer is shown in Fig. 3. It starts with coating and exposure of thick 14 µm resist on a 200 mm low resistivity (5 mΩ/cm) silicon wafer. Vias with diameters ranging from 100 µm to 300 µm are etched using DRIE to a depth of about 300 µm. This is followed by dry strip of resist and dry removal of Teflon-like residues formed inside the vias during the etching process. This cleaning is very important to insure a clean surface for the next step, which is oxide deposition from tetraethoxysilane (TEOS). The minimum target for oxide thickness along the depth of the via is 150 nm. The next step is to pattern the oxide layer with a resist and to etch the oxide to access the low resistivity silicon underneath. Aluminum is then sputtered onto the wafer. Photoresist is spun and patterned to define the contact pads and the remaining aluminum metal is wet etched followed by removal of the resist. The processed wafer is now bonded to a carrier wafer with a temporary glue

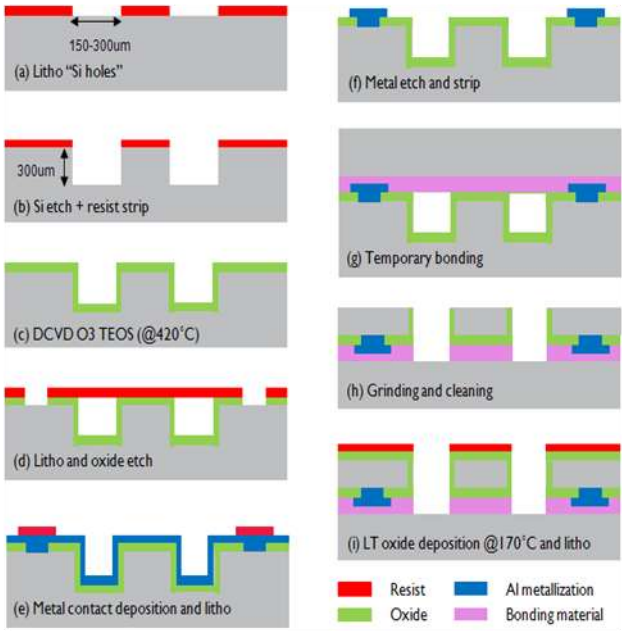

Figure 3: Schematic of the process flow on 200 mm silicon wafers: (a) lithography to define via pattern, (b) deep silicon etch, (c) oxide deposition, (d) lithography to etch oxide to open contacts, (e) metal deposition and lithography to define metal pattern, (f) metal etch and resist strip, (g) temporary bonding to a carrier wafer, (h) grinding and cleaning, and (i) low temperature oxide deposition and photopatternable polymer patterning.

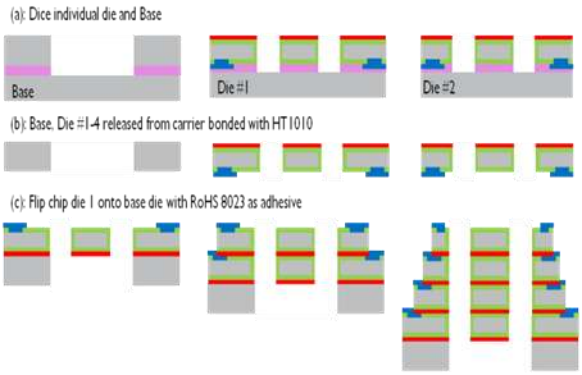

Figure 4: Flip chip process to form the four-layer stacked, electrostatic actuated impingement cooling device: (a) diced base and individual dies, (b) removal of carrier wafer from different dies, and (c) flip chip bonding.

material. The device wafer is thinned down to 150 µm to expose the etched silicon holes thus creating vertical micro channels through the silicon. A low temperature oxide is deposited on the backside of the wafer to provide its electrical insulation and to reinforce the oxide layer on the vertical walls. Afterwards a photopatternable polymer is spun onto the bonded wafer and exposed to define appropriate patterns. This polymer will be used for bonding the various layers of the stack.

The assembly part of the process flow (see fig. 4) proceeds as follows: the wafers are diced in such a way that dies having four different widths are produced, thus allowing for the dies to be stacked on top of each other while still providing the capability to access the metal contact pads on the layers below without using TSV's. The individual dies are debonded from the carrier wafer by using a solvent which removes the temporary glue without affecting the properties of the bonding polymer. The dies are then assembled by flip chip. The first die is bonded onto a base die that will act a reservoir for the cooling liquid. The second, third and fourth die are then assembled with the same procedure. In this way a "tower of Hanoi" structure is created.

Fabrication

In this section we report some important characterization of the fabrication process. Fig. 5a shows SEM images of a via after deep silicon etch and a strip process. The vias are etched in Adixen ICP with a resist mask using the Bosch process. SF_6 gas was used as the etchant while C_4F_8 is used as a passivation gas. The target depth of 320 µm is

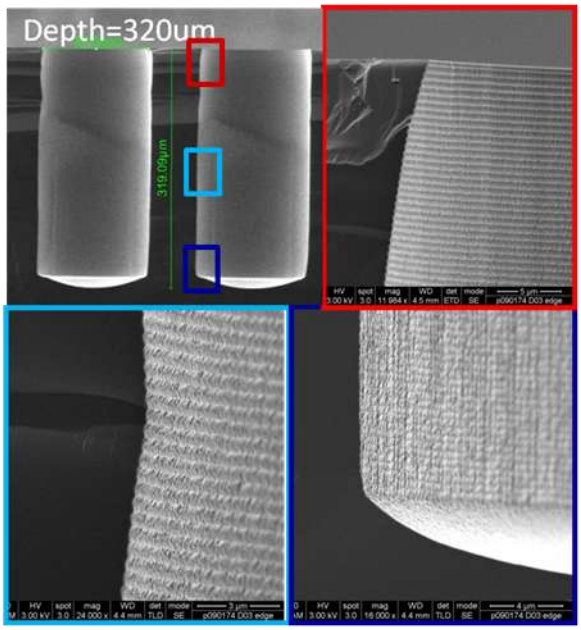

Figure 5: Deep silicon etch and polymer residue removal: a) SEM image showing overview of the via cavity. Close-up images of specific cavity regions are shown in b), c) and d) (respectively top, middle and bottom).

achieved (as seen in Fig. 5a). After etching, a dry strip consisting of CF_4 is implemented to clean the etched surface from the polymer residues deposited during the Bosch passivation step. A clean silicon surface is essential for deposition of the oxide layer inside the vias. Fig. 5b, 5c and 5d shows the zoom images of different parts of the via where the typical scallops resulting from Bosch etching process can clearly be seen. The SEM measurements indicate that the surface is very clean and no residues are present as no charging effect is observed in Fig. 5d. The distortion in the image of the profile of the etched via is an artifact due to sample cleaving.

The next step is the deposition of oxide inside the via. Target thickness on the vertical walls of the vias is 150 nm to 200 nm [18]. TEOS oxide is used. Actual and nominal thicknesses of the oxide layer on the flat, horizontal wafer surface coincide; however, the oxide layer can be thinner on the vertical walls. Initially, a 200 nm oxide layer was deposited on the wafer surface and the thickness was measured at different positions along the via. The resulting measurements are shown in Fig. 6. At the bottom of the via, the oxide thickness is roughly 100 nm, which is below the target oxide thickness. Therefore, the nominal oxide thickness on the wafer surface was increased to 300 nm but little improvement in thickness inside the via was observed. The nominal

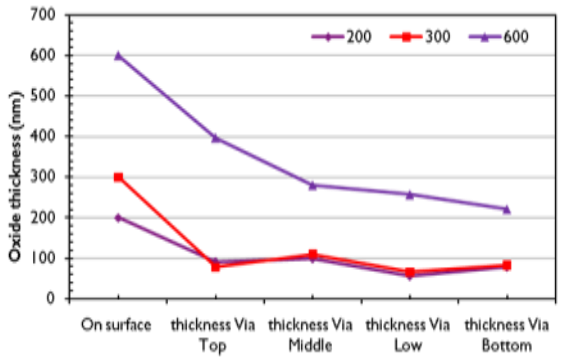

Figure 6: Oxide thickness as a function of different positions inside the via.

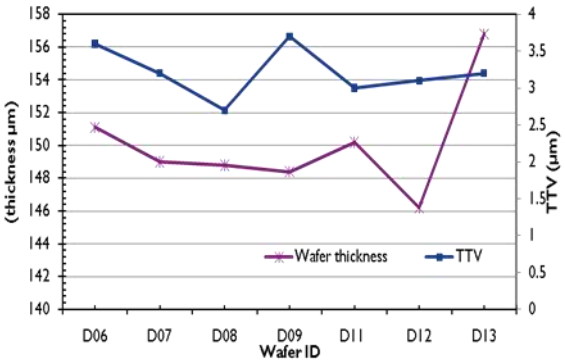

Figure 7: Final device thickness and total thickness variation (TTV) for different wafers.

oxide layer thickness on the wafer surface was then increased to 600 nm; and the minimum target thickness inside the via is achieved (about 200 nm as shown Fig. 6). The graph shows that there is large variation in oxide thickness at different locations inside the via and on the surface. However, as the wafer will be ground down to 150 µm thickness, which is roughly half of the via depth, the range of thickness variation in this region of interest is acceptable.

The next steps are the resist coating and patterning followed by an oxide etch. Due to the large wafer topography the resist spin process must be carefully optimized. It is essential that the walls of the channels are protected during oxide etch for contact opening. A damage of the wall oxide will hinder the functionality of the device. Afterwards, 1 µm of aluminum is sputtered on the wafer and resist is spun and patterned. Aluminum is then removed from the vias and the surface, except for the metal contact and alignment structures. In this case the spinning of the resist is less critical, As coverage does not need to be perfect. In fact, even if some aluminum islands remain on the surface, the device will still be functional. At this stage, the front side processing of the device wafer is completed and backside processing starts.

The wafers are bonded face down on a carrier using temporary glue material in a wafer level-bonding tool. Device wafers are thinned down to a silicon thickness of 150 µm by mechanical grinding. The initial and bulk of the grinding is done with a rough wheel while the final grinding is done with a fine wheel resulting in a polished surface. The final thickness and total thickness variation (TTV) across the wafer are shown in Figure 7. The average thickness for the batch is 150 µm with an average TTV of 3 µm.

During the grinding process, the vias are exposed and the grinding wheel can cause damages at their edge. It is necessary to reduce or eliminate the damage so that during oxide deposition on the other side of the wafer, a conformably coating along the via edges can be achieved. The damage was mitigated through the combination of coarse and fine grinding wheels mentioned previously. Figure 8a shows the top SEM images of a via. There are no grinding residues inside the via that may hinder the deposition of second oxide layer. Figure 8b is a close-up view of the via edge showing that there is little or no damage caused by grinding.

As the thinned wafer is bonded to carrier with a temporary bonding material, the oxide deposition temperature must be lower than 200 ˚C. We have then developed a special recipe that allows depositing CVD oxide at 170 ˚C. To avoid any tool contamination before entering the oxide deposition system, any exposed temporary bonding material must be removed from the wafer. A combination of wet clean and dry strip processes were implemented to remove the polymer, especially at the interface between the device and carrier wafers at the bottom of the vias. The oxide deposition at this lower temperature is non-uniform and a large variation in

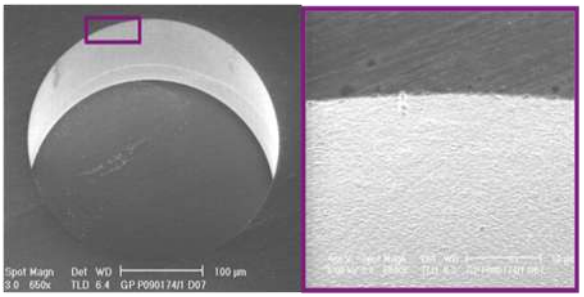

Figure 8: a) SEM images of 300µm diameter via after grinding. b) Close-up of the edge region.

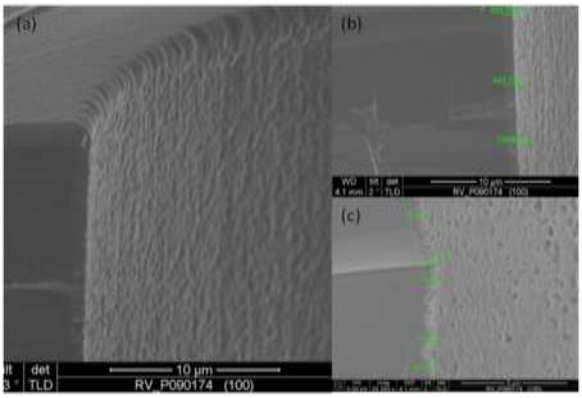

Figure 9: Low temperature oxide deposited on the ground wafer. SEM images show (a) top half of via with oxide covering the corner, (b) oxide thickness in upper half of via, and (c) oxide thickness at the bottom of the via.

oxide thickness from top to bottom was observed as shown in Fig. 9. The deposited thickness at the top surface is 1.5 µm but decreases to roughly 500nm at the middle of the via and remains constant until the bottom. The image also shows that oxide is conformally covering the roughened corner of the via. This was considered as a potential weak point where shorts can results if insulator quality and conformality are not good.

The last part of the full wafer processing is the coating and exposure of polymer material on the ground surface of the device wafer. During the processing of the wafer for the individual layers of the stacked device, the polymer is not cured and can later be used as a bonding material during assembly of the final stacked device. A special, negative tone, photopatternable polymer, Intervia™ Photodielectric 8023, was chosen for this purpose. As it is a negative tone polymer, there is no need to develop the polymer inside the vias. During development, the polymer will just dissolve giving a very clean via inside. Fig. 10a shows the top image of the device wafer with the patterned polymer. Figure 10b shows the cross-sectional SEM image of the via. No polymer is evident inside the cavity.

The final assembly of the electrostatically actuated impingement-cooling device starts with dicing the wafer in four different widths. The length of the dies is fixed at 12.6 mm while the width varies from 13.6 mm for largest die to 10.3 mm for smallest the die. The diced dies are removed from carrier by placing them in a bond removal solvent. Initial investigation on dummy pieces was performed to verify that the debonding solvent does not damage the interlayer bonding polymer. After soaking the

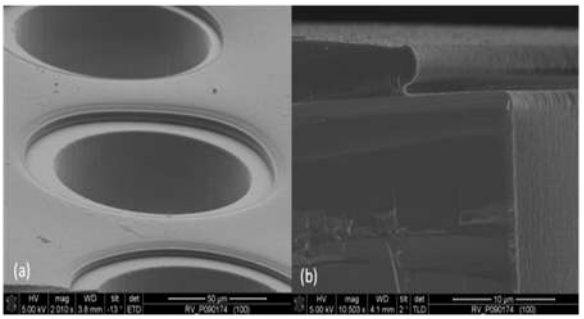

Figure 10: SEM images of photoimageable polymer used as a bonding layer: (a) top view showing the patterned layer and (b) cross-sectional image showing patterned area and deposited oxide inside the via.

dummy die in the solution, no visual deterioration of the polymer was observed.

A flip chip assembly was done to construct the final device. Dummy samples were well bonded after the flip chip operation. The detailed scheme of the bonding process was shown earlier in Fig. 4. The first die with the bonding layer is flip chip faced down onto the base die. The temperature of the bonding is increased for each subsequent bonding and the applied force is decreased as the area of the die becomes smaller. The applied temperature during the flip chip process cures the polymer and at the same time bonds different dies.

Figure 11 shows the final assembly of a four-die module on the base reservoir. The image shows the central region consisting of an array of vertical channel for the droplet flow and metal contact pads for wire bonding at the periphery of each layer.

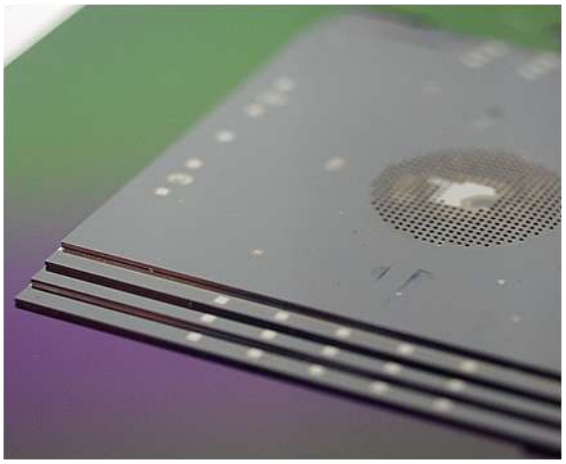

Figure 11: Four die stacked final assembly bonded on the reservoir base.

Preliminary characterization

The first step of characterization consists in verifying the electrowetting properties of the used materials. This can be easily done by placing a droplet of electrically conducting liquid on the top die of the device and measuring the change in contact angle upon application of a potential difference between the droplet and the silicon surface. For these experiments, a 1 M solution of potassium chloride (KCl) in water serves as the electrically conducting liquid.

Fig. 12 shows a 5 μL liquid droplet on the untreated device surface. The contact angle is rather small, about 41°, which is consistent with expectations considering that the device is coated with oxide, a hydrophilic surface. In order for effective electowetting, the contact angle of a sessile droplet on the surface under zero applied voltage should be as large as possible [11]. Therefore, the oxide coated surface is not expected to be a good candidate for an electrowetting device.

In order to increase the contact angle and thus the suitability of the device for electrowetting, the completed test device was coated with perfluorodecyltrichlorosilane (FDTS) in a vapor-phase silanization reaction chamber. Preliminary experiments were then performed on the coated device to assess the performance of the surfaces for electrowetting. The experimental setup for these tests can be seen in Fig. 13. Only a single device layer is used in these preliminary tests. Fig. 13 shows a 5 μL droplet on top of the silanized device. A micromanipulator probe contacts the electrically conductive droplet while another micromanipulator probe contacts the device layer. A change in droplet contact angle can then be observed by applying a potential bias between the two micromanipulator probes where the electrode in contact with the droplet serves as the ground.

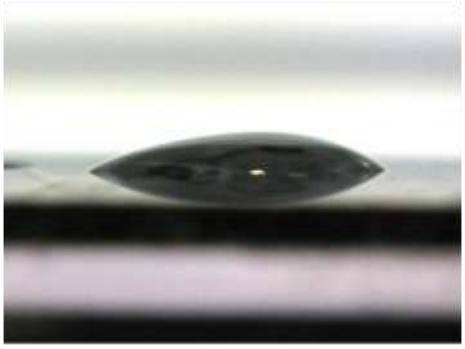

Figure 12: Contact angle of a liquid droplet on the device surface covered with oxide.

Fig. 13a shows the 5 μL droplet under zero applied bias. It is clear from the image that the surface is now hydrophobic with a measured contact angle of 103°. Upon application of a potential bias of 60 V, the droplet contact angle is reduced to 85°. Higher applied voltages appeared to result in the breakdown of the dielectric (*i.e.*, 600 nm of TEOS oxide). According to Moon *et al.* [19], a larger change of contact angle may be desirable for effectively moving liquid droplets by electrical actuation. A larger change in contact angle may be realized by optimization of the oxide layer thickness and quality and/or the use of a more hydrophobic coating [11, 19].

Preliminary experiments have also been conducted on a droplet injected into the channel of the device to see if it can be moved by electrostatic actuation. However, dielectric breakdown occurs at very low voltages (< 5 V) inside the channels of the fabricated device and no evidence of electrowetting is apparent. Improvements to the dielectric layer properties are probably needed before effective electrowetting inside the vertical channels can be realized.

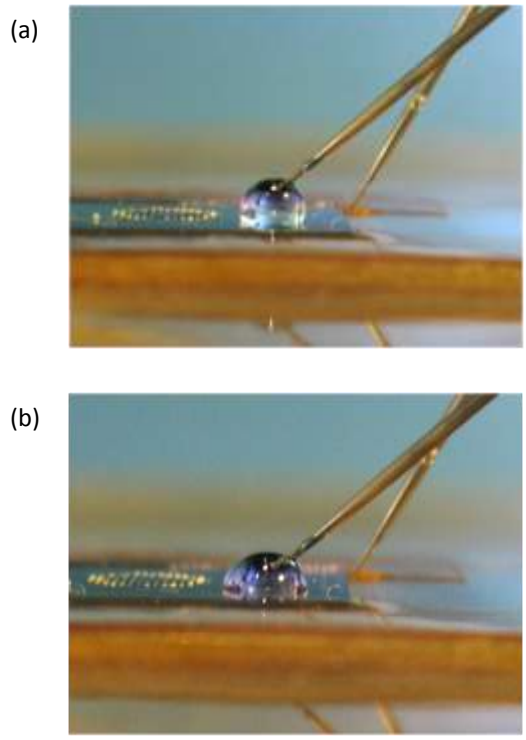

Figure 13: Images of droplet on device surfaces silanized with FDTS: a) zero applied bias and b) 60 V potential.

Conclusions

In this paper we reported on the fabrication of an electrostatically actuated cooling device. We propose a 3D device in which droplets are electrostatically actuated through vertical channels and impinge on an IC surface. The paper mainly addressed the challenges encountered and novel strategies implemented during the fabrication process. The simplified version of the device presented in this paper consists of vertical channels formed by etching through silicon vias and isolating the wafer with an oxide. The final assembly is done by bonding together several dies of different size to create a "tower of Hanoi" structure. In order to enhance electrowetting effect the device surfaces were silanized to make them hydrophobic. Preliminary experimental characterization of the fabricated test devices indicate that optimization of the dielectric and hydrophobic coating are necessary before a fully functional test device can be realized.

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