Design and Demonstration of 40 micron Bump Pitch Multi-layer RDL on Panel-based Glass Interposers

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Abstract
This paper describes the design, fabrication, and characterization of a two-metal layer RDL structure at 40 um pitch on thin glass interposers. Such an RDL structure is targeted at 2.5D glass interposer packages to achieve up to 1 TB/s die-to-die bandwidth and off-interposer data rates greater than 400 Gb/s, driven by consumer demand of online services for mobile devices. Advanced packaging architectures including 2.5D and 3D interposers require fine line lithography beyond the capabilities of current organic package substrates. Although silicon interposers fabricated using back-end-of-line processes can achieve these RDL wiring densities, they suffer from high electrical loss and high cost. Organic interposers with high wiring densities have also been demonstrated recently using a single sided thin film process. This paper goes beyond silicon and organic interposers in demonstrating fine pitch RDL on glass interposers fabricated by low cost, double sided, and panel-scalable processes. The high modulus and smooth surface of glass helps to achieve lithographic pitch close to that of silicon. Furthermore, the low loss tangent of glass helps in reducing dielectric losses, thus improving high-speed signal propagation. A semi-additive process flow and projection excimer laser ablation was used to fabricate two-metal layer RDL structures and bare glass RDL layers. A minimum of 3 um lithography and 20 um micro-via pitch was achieved. High-frequency characterization of these RDL structures demonstrated single-ended insertion losses of -0.097 dB/mm at f = 1 GHz and differential insertion losses of -0.05 dB/mm at f = 14 GHz.

Key words
2.5D interposer, excimer laser ablation, glass interposer, semi-additive process

I. Introduction
Consumer demand for online mobile services is increasing due to the proliferation of smart phones, wearable devices, and Internet-of-Things (IoT). This trend in mobile electronics is driving a need for bandwidth not only in consumer electronics, but also in high performance computing to provide the necessary cloud infrastructure. Wide I/O die-to-die interconnections between devices using 2.5D and 3D architectures are being pursued to address this logic to memory bandwidth need. As a result, the design rules for copper traces on interposers are decreasing rapidly from 3 um lithography at 50 um chip-level interconnect pitch to 1 um lithography at 20 um pitch in the future.

Silicon interposers with side-by-side logic and memory dies have been developed to enable such aggressive package scaling [1], [2]. Stacked silicon interconnect (SSI) and silicon-less interconnect technology (SLIT) have been recently demonstrated by Xilinx for 2.5D integration at 40 um bump pitch, interconnected by sub-micron RDLs using a four-metal layer 65nm back-end-of-line (BEOL) fabrication process. Due to increased fabrication costs, high performance applications utilize silicon interposer architectures. Cost-sensitive applications are leveraging an existing manufacturing architecture to develop organic interposers. The low modulus of the organic core, however, leads to increased warpage, and, combined with surface non-planarity, has limited organic substrates to 5-8 um L/S [3]. Recently Shinko and Samsung have demonstrated thin film wiring layers fabricated directly on top of these conventional substrates to address this challenge [4], [5]. A minimum of 3 um lithography RDLs at 40 um pitch was achieved using chemical mechanical polishing (CMP), photo-vias, and a dry, single-sided semi-additive process flow.
Glass interposers have been proposed and are being developed as a superior alternative to silicon and organic interposers [6]-[8]. Fabrication of these glass interposers using double side, panel-scalable processes can facilitate the necessary die-to-die and off-package bandwidths, while providing a lower cost and higher performance solution when compared to silicon and organic interposers. The higher modulus and smooth surface of glass extends the minimum lithographic ground rules beyond organic substrates, while the low loss tangent helps to achieve lower dielectric losses compared to silicon interposers. Furthermore, process flow does not limit layer assignment. Applying minimum design rules to topside and backside metal layers potentially enables double-sided fine line routing, and thicker metallization using SAP reduces conductor losses in high-frequency transmission lines. Fig. 1 depicts a cross-section schematic of a six metal layer (2+2+2) 2.5D glass interposer where the fine pitch RDLs on top and bottom sides are used to provide ultra-short reach wide I/O die-to-die interconnections, while the RDL layers fabricated directly on glass are used for longer reach or off-interposer high-speed data transmission.

Fig. 1. 2.5D glass interposer cross section schematic with fine pitch build-up and bare glass RDL in a 2+2+2 stack-up.

This paper describes the design, fabrication, and characterization of two-metal layer fine pitch RDLs with dry thin film dielectrics and high speed RDL traces directly on the glass surface—two critical building blocks to enable a 2.5D glass interposer package capable of meeting the high die-to-die and off-interposer bandwidth needs of next generation electronics. Section II describes the design of the two test vehicles. Section III explains the SAP process flow to fabricate RDL directly on the glass panel and on polymer dielectric thin films. Section IV presents the high-frequency characterization results for the fine line and bare glass interconnects.

II. Test Vehicle Design

Two test vehicles delineate the process development of RDL on glass: (a) fine pitch RDL and (b) bare glass RDL.

The aforementioned signal regimes in a 2.5D packaging architecture and their respective enabling technologies prompt these distinctions in test vehicle (TV) design. A wide I/O die-to-die signaling bus requires reduced line and space approaching BEOL design rule and blind micro-via pitch matching the chip level interconnection pitch for die escape at a reduced number of package layers. Off package signal lines, however, do not require these aggressive line densities, but must minimize transmission loss and propagation delay. Routing these high-speed data buses directly on glass can minimize dB/mm losses compared to silicon. The following section describes the stack-up and design rule targets for these test vehicles.

A. Fine Pitch RDL

The fine pitch RDL test vehicle design includes a 2+0+2 stack-up on a 100-300 um thick glass panel as shown in Fig. 2. A symmetric two-metal layer fine pitch RDL design is included on either side of this interposer stack-up. The target polymer thickness of the build-up layers is based on dry thin film thickness ranging from 5-10 um. Using the minimum film thickness, the target copper thickness is 2.5 um in order to maximize metal thickness (reducing conductor losses) while maintaining a high degree of coplanarity between build up layers for fine line lithography yield. The blind micro-via stack-up is determined by the laser ablation process, which determines minimum via size and panel-level alignment tolerance. A fixed via size of 8 um is used to achieve a maximum micro-via aspect ratio of 1:1. Via landing pad size is varied between 12-20 um, while capture pad size is varied between 14-20 um. Minimizing micro-via and pad sizes is critical to increasing die escape routing efficiency as these parameters determine effective lines/mm² along with fine line lithography, which was varied between 1-5 um on both metal layers.

Fig. 2. Fine pitch RDL test vehicle stack-up and target design rules.

B. Bare Glass RDL

The bare glass RDL test vehicle includes a two metal layer stack-up on a 100-300 um thick glass panel as shown in Fig. 3. Design rules for the differential microstrip lines: (a) 155/120 um L/S and (b) 100/54 um L/S are determined using 2D EM extraction as described in [9]. Measurement data in
Section IV is distinguished by the single-ended line impedance according to line width variation where $Z_0 = 60 \Omega$ and $Z_0 = 70 \Omega$ corresponds to $w = 155 \text{um}$ and $w = 100 \text{um}$ respectively. The target glass thickness is fixed based on the line spacing to achieve a line-to-line differential impedance of $Z_d = 100 \Omega$.

Fig. 3. Bare glass RDL test vehicle stack-up and target design rules.

Photoresist film thickness used in the SAP determined a target copper thickness of 5-8 um. In practice, this metal thickness for RDLs on glass will need to be optimized for electrical loss and fine line yield on subsequent build-up layers. The through package via (TPV) stack-up was not critical for this test vehicle as differential line test structures were fabricated on the top metal layer while the bottom metal layer was reserved as a reference layer. Therefore, TPVs were a part of the return path and no signal via were fabricated or characterized.

III. Glass Interposer RDL Fabrication

Both test vehicles are fabricated using a double-side, panel-scalable SAP flow shown in Fig. 4 on 100-300 um thick glass panels of various length and width form factor. The fine pitch RDL test vehicle used a 150 mm x 150 mm panel, while the bare glass RDL test vehicle used a 100 mm x 100 mm panel size. The following sections describe fabrication processes to achieve fine pitch RDLs at 20 and 40 um micro-via pitch. Results given in [9] provide fabrication process details and analysis of bare glass RDL test structures.

In order to form structures less than 10 um lithography using SAP, a high coplanarity is required on the underlying dielectric layer. The first step in fabricating the fine pitch RDL test vehicle is vacuum lamination of an inter-layer dielectric (ILD) on a glass panel that has been treated with a silane layer to increase adhesion between the polymer and glass dielectric layers. This is followed by the first SAP forming the inner metal layer. To maintain the planarity for the second SAP, a second vacuum lamination is followed by a hot press before blind micro-via formation by excimer laser ablation. Test vehicle fabrication is completed after a second SAP. No passivation or surface finish trials are carried out in this study.

1. 5-10 \text{um} dry film lamination on glass core.
2. Semi-additive process (SAP1) to form 2.5 \text{um} thick inner metal layer.
3. 5-10 \text{um} vacuum lamination on inner metal layer followed by hot press for planarization.
5. Top metal layer and micro-via metallization by semi-additive process (SAP2).

Fig. 4. Glass panel semi-additive process flow to form fine pitch RDLs.

The following sections provide more analysis on the process development of micro-via fabrication in two different polymers as ILDs, and describe fabrication results of the two-metal layer test vehicle.

A. Blind Micro-via Laser Ablation and Metallization

In this study, a $\lambda = 248$ nm KrF excimer laser at 1 J fluence is used for micro-via fabrication using a projection ablation scheme, which utilized a quartz mask with sputtered aluminum openings, to increase the process throughput in scaling on a panel level. Micro-vias fabricated in this manner serve as interlayer vias between the top metal layer and inner metal layer shown in Fig. 4. Fig. 5.a.i shows a top view of the drilled vias at 40 um pitch in polymer A. The shape of the vias is circular, indicating no thermal damage during the ablation process. A cross section of the drilled via is shown in Fig. 5.b after seed layer deposition. No significant damage on the bottom copper pad and very small via taper is observed. Using the same fabrication process, micro-vias are
drilled through a 5 um ILD layer consisting of polymer B. Fig. 5.a.ii below shows a 20 um pitch area array on a non-patterned copper plane. In this sample, a topside via opening of 10um is observed with a 5-6 um bottom side opening. As a part of SAP2, this via size is increased by approximately 2 um as a result of desmear.

Fig. 5. (a) Blind micro-via formation in (i) Polymer A and (ii) Polymer B using projection excimer laser ablation and SAP metallization of via after (b) seed layer deposition (Polymer A), and electrolytic plating over (c) Polymer A (d) Polymer B.

Metallization of the micro-via was carried out by electroless copper plating followed by electrolytic copper plating. After desmear of the drilled sample, a palladium catalyzed electroless plating process is applied and 0.5 um thick copper seed layer is formed. Electrolytic plating at t = 40 min is used to achieve fully-filled metallized vias as shown in Fig. 5.c-d at 40-20 um via pitch. Achieving fully filled micro-via at fine pitch is critical for 2.5D and 3D interposer packages to increase die escape routing efficiency using a via-in-pad assembly scheme. Therefore, after SAP, observing voidless via fill and a low degree of dishing in the top metal layer is required for reliable chip-level assembly.

B. Two-metal Layer Fine Pitch RDL

As summarized in Fig. 4, the two metal layer RDL TV is fabricated using a conventional electro-less plating based SAP with differential spray etching to metallize each layer and micro-vias. Dummy mesh was added in the design of each layer to balance the copper distribution. This allowed for uniform copper plating, ensuring decreased panel warpage during build-up fabrication and surface planarity in subsequent ILD laminations. Metal structures are patterned by projection photolithography using a USHIO Inc. UX-44101 tool. Electrolytic copper plating at 1.0 A/dm² and t = 20 min is used to form each metal layer. Fig. 6.a-b shows fabrication results of the inner (SAP1) and top metal (SAP2) layers respectively.

Fig. 6. Fine pitch escape routing on (a) inner metal layer after SAP1 and (b) top metal layer after SAP2. Two metal layer RDL with 3 um lithography at 40 um pitch.
laser u-via processes on (c) Polymer B laminated on low-CTE laminate core and (d) Polymer A laminated on glass core.

Two fabrication trials using the fine pitch RDL TV design are shown in Fig. 6.c-d. Fig. 6.c shows two metal layer fabrication on a 150 um thick low-CTE laminate and polymer B ILD. After micro-via ablation and chemical desmear, the average surface roughness of the 5 um thick polymer B layer on the topside is 78nm as measured by atomic force microscopy (AFM). A low surface roughness along with the aforementioned coplanarity is critical in minimizing SAP feature size. In Fig. 6.c a multilayer RDL with 3 um lithography is achieved. Fig. 6.d shows two metal layer fabrication on a 300 um thick glass panel. Vias with 10 um diameter were filled by plated copper at 2.5 um line width and 2 um and 4 um copper thickness for bottom and top layers respectively.

IV. Characterization of RDL on Glass

The electrical design of a 2.5D glass interposer requires two signaling regimes: (1) die-to-die wide I/O and (2) off interposer high-speed. The die-to-die wide I/O bus requires aggressive RDL design rules as shown in the fabrication results above to increase line density per unit area to achieve the required bandwidth between dies. Off interposer high-speed signaling, however, does not require these aggressive design rules but minimizing transmission loss is most critical for achieving required performance. The sections below describe the high frequency characterization of transmission lines for these signal regimes using a vector network analyzer (VNA).

A. Single-ended Fine Line High Frequency Characterization

Single-ended coplanar waveguide (CPW) transmission lines are designed and simulated on our proposed 2.5D glass interposer. The CPW transmission line requires one metal layer, as shown in Fig. 7. Depending on the polymer and its thickness, the characteristic impedance of the CPW can be adjusted by signal trace width (w in Fig. 7) and the gap between signal and ground (s in Fig. 7).

Ansoft HFSS is used for CPW design parameter validation on glass. Excitation of the transmission line structure used de-embedded wave ports to compute the high-frequency response. The epoxy based polymer used in the model is a 17.5 um thick polymer A ($\varepsilon_r = 3.0$ and $\tan\delta = 0.005$ at $f = 10$ GHz) layer with a glass core of ($\varepsilon_r = 5.3$ and $\tan\delta = 0.005$ at $f = 2.4$ GHz). To minimize the insertion loss, the CPW transmission line is designed to have $Z_0 = 50$ $\Omega$. For this study, the CPW test structure was designed with w from 5 um to 25 um.

Coplanar waveguide fabrication is achieved using a similar SAP flow summarized in Fig. 4. The micrograph of a 5 mm long, 5 um signal width CPW with measurement pad designed for VNA is shown in Fig. 8.a. Due to the fabrication process, however, w is smaller than designed while s is larger due to over etch during copper seed layer removal. This will result in impedance mismatch for the designed CPW transmission lines. A SOLT calibration was performed up to $f = 20$ GHz before measuring the frequency s-parameter response of the CPW transmission line on glass. Design validation required plugging fabricated parameters, w and s, of CPW transmission back into the HFSS model. Fig. 8.b shows the return loss and insertion loss correlation between HFSS simulation and VNA measurement of the 5 mm long CPW. Both the measured return loss and insertion loss are very well matched to the simulation up to 16 GHz, and a measured single-ended insertion loss of -0.097 dB/mm is observed at $f = 1$ GHz. For frequencies above 16 GHz, the deviation between the simulation and the measurement results increased. This is mainly due to the roughness of the copper surface that is not included in the HFSS model. The last step of the SAP is copper seed layer etching, which will etch the copper traces as well as the seed layer. Even with the differential etch, the roughness of the copper traces still increases. At high frequency, the current is distributed near the copper trace surface, and experiences higher resistance due to the surface roughness. Therefore, the measured insertion loss is larger than the simulation at $f > 16$ GHz.

Fig. 7. 3D EM Fine Line CPW wave port model.
Fig. 8. (a) Fine line CPW fabrication on glass panel and (b) measured versus simulated return loss and insertion loss up to \( f = 20 \text{ GHz} \).

B. Differential Line on Bare Glass High Frequency Characterization

Design and simulation of the differential microstrip transmission lines used Q3D extractor and Ansoft HFSS. The 2.5D architecture in Fig. 1 may use these transmission line structures as the high-speed signaling interface. Because of the thin glass panel processing, these lines are fabricated directly on the interposer core and have \( Z_d = 100 \, \Omega \) at 154 \( \mu \text{m} \) minimum line pitch. Decreasing line pitch further while maintaining this differential impedance is possible as the required line density is application dependent (e.g. HDMI, CDFP, etc.). A waveport model is used to simulate differential return (\( S_{d11} \)) and insertion loss (\( S_{d21} \)). Port de-embedding in Ansoft HFSS allows for accurate extraction of electrical performance at variable line lengths. This model assumes copper directly on 130 \( \mu \text{m} \) thick glass (\( \varepsilon_r = 5.0 \) and \( \tan \delta = 0.006 \) at \( f = 10.26 \text{ GHz} \)). Differential line test structures with pitches specified in Fig. 3 are designed at line lengths \( L = 1-50 \text{ mm} \).

The differential line test structures are fabricated directly on glass using an SAP flow similar to the process used for fine line fabrication. This SAP step uses a titanium seed layer to increase adhesion between the RDL and glass panel. High frequency characterization of these structures is performed using a 4-port VNA and SOLT calibration. Fig. 10.a shows the measured differential insertion loss compared to the 3D EM modeling results up to \( f = 16 \text{ GHz} \). Good hardware to model correlation is observed up to \( f = 14 \text{ GHz} \) with deviation at high frequency due to the calibration method.

A useful metric is loss per unit millimeter (dB/mm) to support future electrical design of a high-speed signal bus utilizing a differential signaling scheme. This design metric is extracted from the measured data using \( S_{d21} \) results for line lengths \( L = 5 - 30 \text{ mm} \). Due to a degree of noise in the measured results, a second order polynomial regression is used to fit the measured data. Then, the fitted loss at \( f = 14 \text{ GHz} \) is extracted. This fitted parameter for the various line lengths of interest is shown as dots in Fig. 10.b. A linear regression is then applied where the slope of this linear regression represents the desired loss metric. Differential insertion loss of -0.05 – 0.07 dB/mm at \( f = 14 \text{ GHz} \) is observed for the line variations studied.

Fig. 9. 3D EM Differential MSL wave port model.

Fig. 10. (a) Measured versus simulated insertion loss of differential MSL transmission lines at line lengths 15 mm and 30 mm up to \( f = 16 \text{ GHz} \) and (b) insertion loss at \( f = 14 \text{ GHz} \) at line lengths \( L = 5 - 30 \text{ mm} \).
V. Conclusion

This paper demonstrated glass panel fabrication processes including: (1) bare glass metallization, (2) projection excimer micro-via laser ablation, and (3) advanced SAP to achieve 3 um lithography. Characterization of RDL test structures showed a single-ended insertion loss of -0.097 dB/mm at f = 1 GHz and a minimum differential insertion loss of -0.05 dB/mm at f = 14 GHz. These RDL processes on glass result in a superior electrical performance to enable increased die-to-die and off-interposer bandwidths. Wide I/O die-to-die signaling can be realized at 40 um chip-level bump pitch using the SAP flow demonstrated in the results above. Furthermore, off-interposer bandwidth may be increased using RDLs directly on glass. Demonstrating these RDL technologies using double side, panel-scalable processes show the cost and performance benefits of a 2.5D glass interposer package compared to silicon and organic interposer technologies.

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