A Robust, Composite Packaging Approach for a High Voltage 6.5kV IGBT and Series Diode

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Abstract

The main motivation of this work is to design, fabricate, test, and compare an alternative, robust packaging approach for a power semiconductor current switch. Packaging a high voltage power semiconductor current switch into a single power module, compared to using separate power modules, offers cost, performance, and reliability advantages. With the advent of Wide-Bandgap (WBG) semiconductors, such as Silicon-Carbide, singular power electronic devices, where a device is denoted as a single transistor or rectifier unit on a chip, can now operate beyond 10kV-15kV levels and switch at frequencies within the kHz range. The improved voltage blocking capability reduces the number of series connected devices within the circuit, but challenges power module designers to create packages capable of managing the electrical, mechanical, and thermal stresses produced during operation. The non-sinusoidal nature of this stress punctuated with extremely fast changes in voltage and current, with respect to time, leads to non-ideal electrical and thermal performance. An optimized power semiconductor series current switch is fabricated using an IGBT (6500V/25A die) and SiC JBS Diode (6000V/10A), packaged into a 3D printed housing, to create a composite series current switch package (CSCSP). The final chosen device configuration was simulated and verified in an ANSYS software package. Also, the thermal behavior of such a composite package was simulated and verified using COMSOL. The simulated results were then compared with empirically obtained data, in order to ensure that the thermal ratings of the power devices were not exceeded; directly affecting the maximum attainable frequency of operation for the CSCSP. Both power semiconductor series current switch designs are tested and characterized under hard switching conditions. Special attention is given to ensure the voltage stress across the devices is significantly reduced.

Key words

Wide-Bandgap, Current Switch, High Voltage, Series IGBT and Diode, Silicon Carbide.

I. Introduction

The current switch (series connected switch and diode) has found its application in various current source based converters [1]-[5]. The main advantages of using current-source based topologies can be linked to the fact that these converters usually use less number of active switches, have a more rugged natural protection (owing to the series diode), are well suited for zero-current and zero-voltage based soft switching [6]-[7]. These converters are usually made using thyristors with external commutation circuits, albeit at low switching frequency. The frequency of operation can be pushed to significantly higher values by using faster devices, like IGBTs. With the advent of Silicon-Carbide Devices, singular power electronic devices can now operate beyond 10kV-15kV levels [8]-[11]. This effectively reduces the number of series connected components in the circuit, but drastically increases the dielectric and thermal stresses that develop within the power module. The non-sinusoidal nature of this stress, punctuated with high dV/dt and dI/dt, leads to several steep constraints in terms of parasitic series inductance, shunt stray capacitance, capacitive coupling, and thermal conduction [12].

As previously mentioned, the current switch has an additional diode in series with the regular active switch. Packaging this structure comes with an inherent problem of dealing with peak positive (owing to the switch) and negative (owing to the diode) voltage stress within a span of less than 100µs. This is considerably larger than regular

switches for the same terminal voltage rating. In order to fully understand how these non-conventional stresses affect the current switch packaging, and therefore the overall switch operation, multi-physics simulations has been performed for various layouts of this series diode and regular switch topology based on a material selection that is capable of the required dielectric strength. Various cross simulation results have then been used in an iterative fashion to redesign and analyze the optimized package structure for the final current switch design.

The paper has been divided into several subparts. First, the basic difference of compact package as opposed to discrete assembly is stated. Then two different approaches of fabrication are discussed. Various advantages and disadvantages of both approaches are shown. Thermal analysis and maximum attainable frequency calculation is shown next. To verify the credibility of the work, a compact package is fabricated and tested. Various test results have been enumerated. Finally, the paper is concluded depicting the major critical design parameters and proposed design considerations. Figure 1 shows various packaging components of a standard power module which will be used in the following sections for reference.

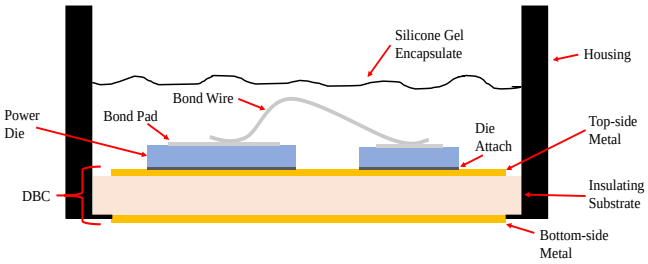

Figure 1: General structure and components of a typical package

II. Composite vs. Discrete Packaging

A power semiconductor current switch, for current source converters, contains a transistor and diode in series. Packaging a power semiconductor current switch comes with an inherent problem of managing peak voltage stress across the transistor and diode within a span of less than 100µs. Series current switches are partitioned into two discrete packages to manage the voltage isolation and thermal dissipation issues encountered when working with high power WBG devices. This series current switch configuration will be referred to as a two package series current switch (TPSCS). Figure 2 shows a mechanical schematic of this assembly. Within each discrete device package, the device is connected to exiting power terminals using parallel wire bonds. Since an individually packaged IGBT is connected in series to a following individually packaged diode, the number of series connected wire bonds equates to the summation of all wire bonds found within the two discrete packages that make up the TPSCS.

Many wire bonds have a negative effect on the packages' electrical performance, and reduces system robustness. By introducing direct IGBT to diode wire bonds within a composite package, rather than having a TPSCS, the number of series connected wire bonds decreases within the series current switch, thereby reducing unwanted voltage stress on the semiconductor devices. Moreover, it has been shown that long term failure modes within power modules are due to the failure of the package interconnects, such as wire bonds and die attach materials, not necessarily device failure.

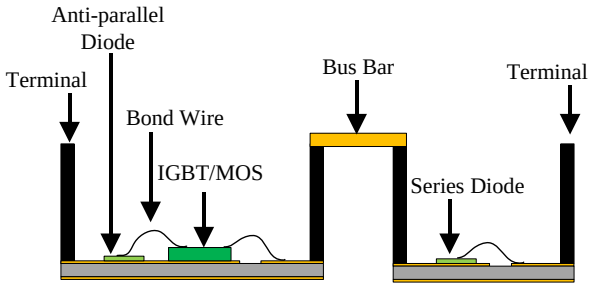

Figure 2: Current switch with series connected discrete modules (TPSCS)

An optimized power semiconductor series current switch is fabricated using an IGBT (6500V/25A die) and diode (6000V/10A), packaged into a 3D printed housing, to create a composite series current switch package (CSCSP). The effects of connecting the series diode and the IGBT in different configurations within the SCSP has been analyzed in regards to improving electrical performance of the CSCSP. Figure 3 shows a mechanical schematic of this structure.

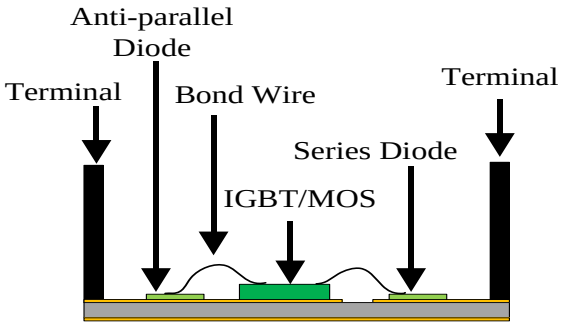

Figure 3: Current switch with series connection, single modules (CSCSP)

III. Primary Topologies of CSCSP

A. Preferred Die and Interconnect Placement

The arrangements of series connection of IGBT and Diode can be done in two broad ways. The Cathode of the diode can be connected to the collector of the IGBT or the emitter of the IGBT can be connected to the anode of the diode. As mentioned in the prior section, the series parasitic inductance in this package usually leads to unwanted stress, thereby leading to unreliable operation. It should be noted that the cathode-collector connected design leads to two

distinct bond wire bridges in the conduction path, thereby considerably increasing the parasitic inductance and resistance of the design. This would also lead to increased probability of module failure in the case of current magnitudes greater than or equal to the fusing currents necessary to burn open the bond wires. The only possible advantage would be owing to the fact that this structure has separate isolated islands for the terminals. This would result in a somewhat more rugged package. Figure 4 shows the fundamental circuit schematic, 3D Model and schematic with extracted parasitic.

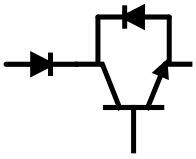

Figure 4(a): Schematic of cathode-collector connected current switch

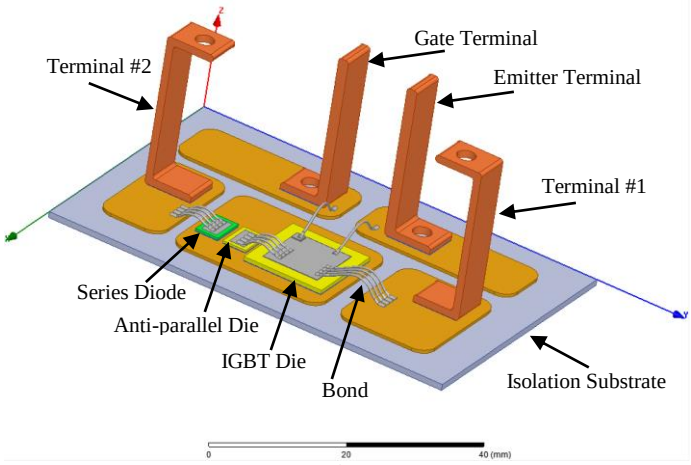

Figure 4(b): ANSYS Q3D rendering of cathode-collector connected model

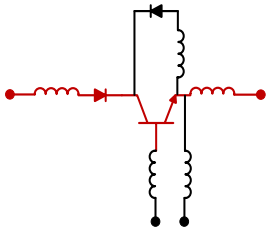

Figure 4(c): Circuit schematic of the cathode-collector connected configuration incorporating parasitic non-idealities

Emitter-Anode connected designs on the other hand leads to a more compact design with just one series connected bond Wire Bridge. This considerably reduces the parasitic parameters and has safer operating conditions as compared to the previous design.

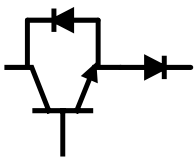

Figure 5(a): Schematic of emitter-anode connected current switch

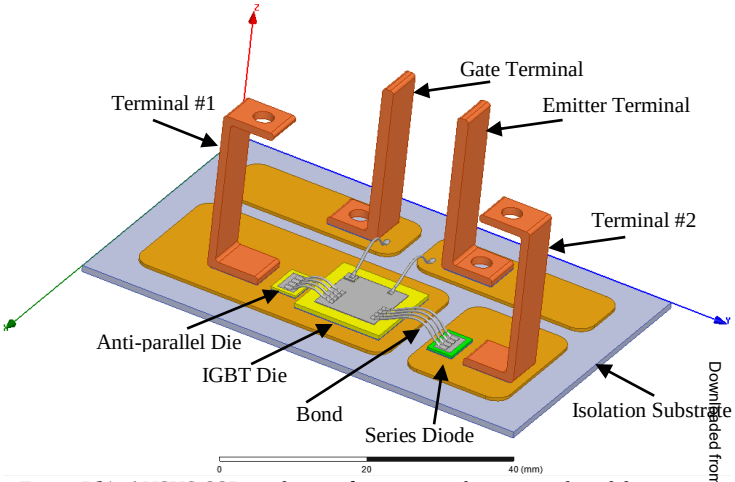

Figure 5(b): ANSYS Q3D rendering of emitter-anode connected model

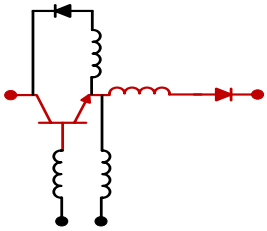

Figure 5(c): Circuit schematic of the emitter-anode connected configuration incorporating parasitic non-idealities

Figure 5 shows the 3D Model depicting the preferred locations of the dies and bond wires for this configuration. From next section onwards, only the configuration shown in Figure 5 is considered.

B. Stacked Bond Wire Topology

Power semiconductor devices have top side metallization pads that do not always allow for the easy accommodation of multiple bond wires which are necessary to achieve the required current carrying capability and provide redundancy. With the advent of SiC and GaN devices, the accessible area has considerably shrunk reducing the cost of material and size of package. Due to the fast dI/dt transitions of these devices, the parasitic constraints are also stringent. One way of handling this is to add stacked bondwires one on top of other. This helps in better utilization of the pad area by providing reduction of inductance, resistance and leads to better thermal performance.

Figure 6 shows a Q3D model of a single stacked bondwire. The value of inductance as a function of frequency is computed for single, double and triple bondwires connected in parallel to get a good understanding of the advantages in terms of reduction of inductance. As shown in Table 1, the reduction of inductance can range from 14%-25% for these cases. Figure 7 shows the physical

manifestation of a stacked bondwire connected to a diode of small metallization area.

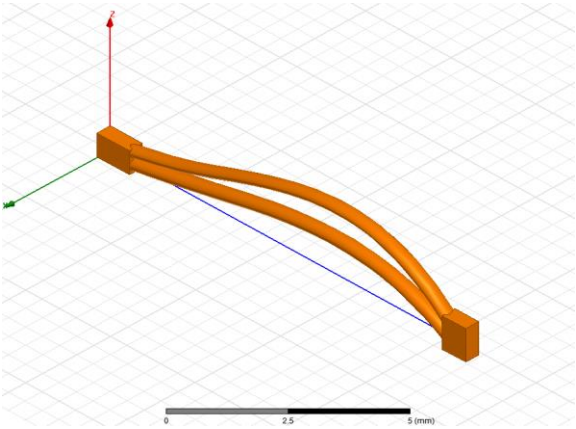

Figure 6: ANSYS Q3D single stacked bond wire (N=1)

Table 1: Wire bond inductance vs. frequency

Freq. (kHz)	N=1		N=2		N=3	
	Single	Stacked	Single	Stacked	Single	Stacked
0.1	8.3168	6.8123	5.9029	4.4167	4.7835	3.3936
100	8.268	6.6409	5.6564	3.7335	4.3419	2.6049
500	7.9685	6.2499	5.2933	3.4867	4.0324	2.4341
1000	7.7992	6.1103	5.1797	3.4250	3.9492	2.3926

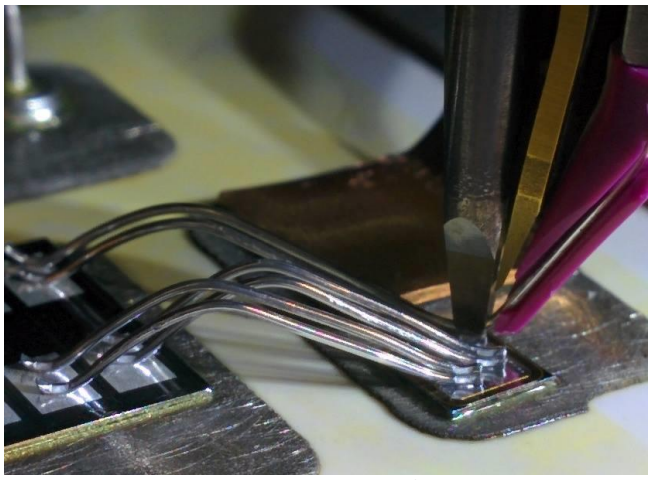

Figure 7: Stacked 15mil Al wire bonds from IGBT to diode

IV. Thermal Study

In order to obtain a basic understanding of initial thermal constraints of the package design, a Heat Transfer in Solids (conduction) study was done using COMSOL Multi-physics software. The thermal simulation analyzed the total power loss of the series current switch package based on the summation of the typical, rated conduction loss and switching loss of both the Si-IGBT and SiC-Diode and I^2R losses of the direct bond copper (DBC), as portrayed by Table 2.

Based on the total power dissipation conditions and the planar cross-sectional areas of the Si-IGBT and series SiC-Diode, appropriate heat source boundary conditions were established for the power die within the package. The Si-IGBT die has a planar cross-sectional area of 13.56mm x 13.56mm, and a die thickness of 0.670mm. The series SiC-Diode die has a cross-sectional area of 3.94mm x 5.70 mm, and a die thickness of 0.387mm. Therefore, specific heat flow rates were calculated for these die dimensions depending on the operating point of study as a function of switching frequency. The frequency dependent heat flow rates for each die were calculated based on the loss data of Table 2 and Equations 1 and 2 below.

*Si-IGBT Loss (f_{sw}) = (Total Rated Switching Loss + Conduction Power Loss)/(Si-IGBT die area) = (0.125J * f_{sw} + 105 W)/(13.56mm x 13.56mm) [W/m^2]* *Eqn (1)*

*SiC-Diode Loss (f_{sw}) = (Total Rated Switching Loss + Conduction Power Loss)/(SiC-Diode die area) = (0.01J * f_{sw} + 40 W)/(3.94mm x 5.70mm) [W/m^2]* *Eqn (2)*

An assumption was made that the ambient temperature on the back-side of the DBC, where a cold-plate would be mounted, has a safe operating temperature of 45℃. During the package fabrication process, a silicone gel will be used as an encapsulate material to cover the top-side of the DBC substrate along with the power semiconductor die, the bottom third of the terminals, and the wire bonds. The silicone gel used in the simulation (Silopren* Gel 6209) has a thermal conductivity of 0.17 W/m-K and a thickness of 2.0 cm in order to electrically isolate the devices and interconnects up past the height of the wire bond loops. The thermal resistance of the silicone gel was calculated to be 0.09375 m^{2}K/W. This resistive boundary layer was taken into consideration within the thermal simulation as well, and was applied to all top-side surfaces within the package that comes into contact with the encapsulate material. Simulations were also done without the silicone gel, simply using the thermal conductivity of air for all exposed top-side surface boundary conditions, and a negligible difference in thermal performance was observed. It should also be noted that the wire bond interconnects were removed from the 3D CAD model within COMSOL due to their negligible effect on the heat transfer compared to the entirety of the package.

The thermal simulation is swept as a function of the overall loss in Si-IGBT and SiC-Diode at different frequencies for different isolation substrate materials. This will enable the maximum attainable frequency constraint for which the loss is same as that which leads to a peak internal temperature of 150℃. According to the data sheets, typical loss data as a function of rated current and voltage is shown in Table 2. Using this table, the overall loss of IGBT and Diode is estimated as a function of frequency, as previously described in (1) and (2). All calculations have been done at V = 3600V and I_c = 20A.

These loss data at different frequencies are used as boundary condition inputs to the COMSOL thermal model of the design. The maximum temperature for each simulation is noted, and the maximum frequency for which the peak temperature is about 150 °C is tabulated. The isolation substrates studied are Alumina, AlN, and BeO. Table 3 shows the material properties of these substrates

Table 2: Typical loss data as a function of rated current, voltage at 150°C

Parameters	Value
Conduction Power Loss of Si-IGBT	105 W
Total Switching Loss of Si-IGBT	1.5e-4*I_C^2+1.8e-3*I_c+0.03 J
Total Switching Loss of Si-IGBT (@ V=3600V and I_c=20A)	0.125J
Total Switching Loss of SiC-Diode (@ V=3600V and I_c=20A)	0.01J
Conduction Power Loss of SiC-Diode	40 W
I^2R Losses (using Aluminum Bond Wires)	36 W

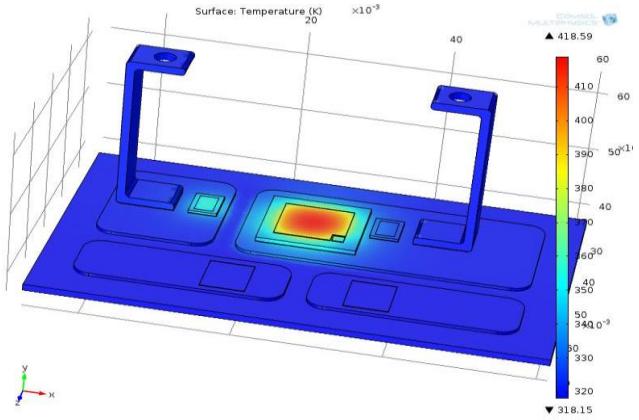

Figure 8: Temperature distribution in the package with alumina substrate

Table 3: Material properties of the studied substrates [16]

Material	Thermal Conductivity [W/m*K]	Heat Capacity [J/kg*K]	Density [kg/m^3]
Alumina	27	765	3970
AlN	165	745	3260
BeO	270	1047	3000

Figure 8 shows the simulation results of the package at the maximum permissible frequency for Alumina. Figure 9 shows the variation of peak temperature as a function of switching frequency. This data can be further used for an optimum converter design. The size and efficiency of an overall converter comprising of power modules, magnetic components like inductors and transformers, and capacitors varies as a function of frequency. Higher frequency operation is preferred as it reduces the size of passive components. The data presented in this paper can hence be used to model a high density power converter of desirable efficiency. It should be noted that BeO and AlN enabled DBCs can elevate the performance envelope of the device beyond 10kHz switching frequency at high voltage operation.

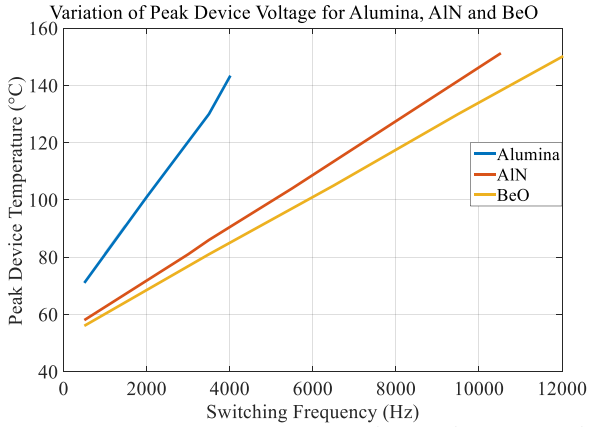

Figure 9: Peak package temperature as a funtion of overall loss of IGBT+diode

V. Hardware Testing Results

Hard-switching tests were performed on the custom, fabricated CSCSP. Figure 10 shows the initial structure of the package. The outer casing is 3D printed for optimized terminal positions. Double Pulse Test has been conducted up to 4000V. Figure 11 shows the hardware test setup. Special care has been taken to make sure the loop inductance of the circuit is as low as possible. The gate driver power supply has high voltage isolation for high side gating.

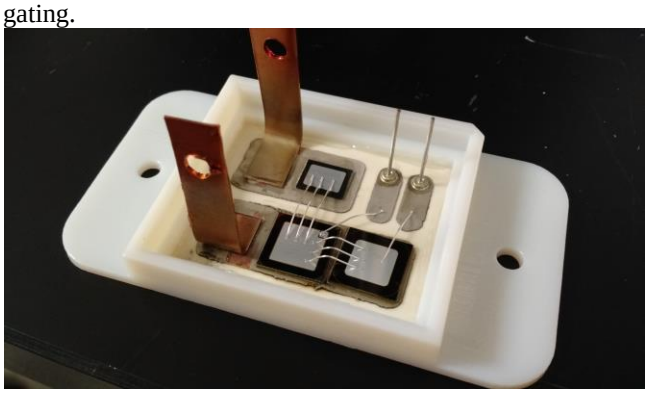

Figure 10: Custom, fabricated CSCSP – DBC based

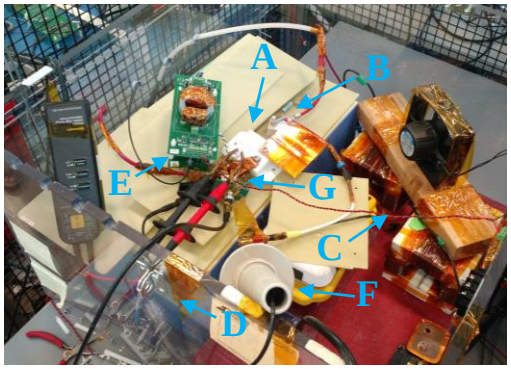

Figure 11: High-V double pulse test setup of CSCSP (A: CSCSP module, B: 10kV/10A SiC JBS diode, C: 8mH inductor, D: 250µF capacitor bank, E: gate driver, F: high-V probe, G: high-BW current probe)

Figure 12 and 13 shows double pulse test results (turn-on, turn-off transitions, respectively) at 2300V and 4000V. As it can be seen, the transitions were smooth with low overshoot voltage and current.

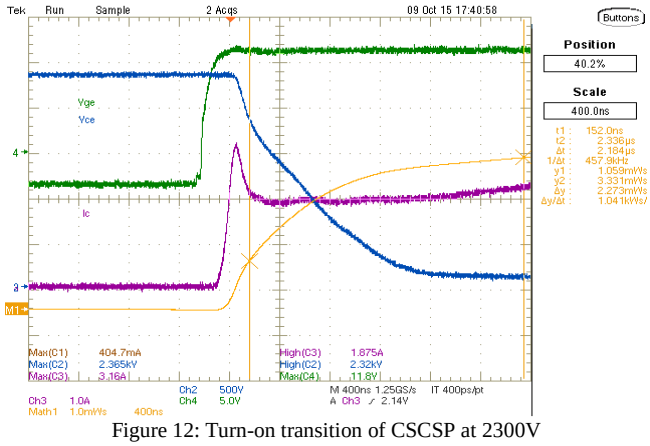

Figure 12: Turn-on transition of CSCSP at 2300V

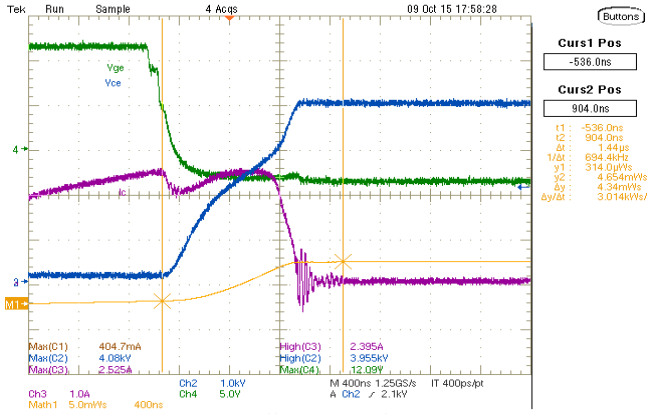

Figure 13: Turn-off transition of CSCSP at 4000V

VI. Conclusion

The main motive of the digest is to demonstrate various package design considerations to accommodate series connection of high voltage Si-IGBT (6500V/25A Die) and SiC-Diode (6000V/10A die). The advantages of connecting the emitter to the anode, as opposed to cathode to collector, are shown in terms of effective series parasitic inductance. An initial design of the package has been fabricated and test. The test results look very promising up to 4000V in terms of lower losses and device stress (voltage and current overshoot). The primary output of this work would be to put forward a set of detailed design considerations for packaging a high voltage current switch.

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