# Application of Low-*k* Liner for Stress and Capacitance Control in Cu-TSV

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## Abstract

Through silicon via (TSV) is commonly fabricated by high aspect ratio deep silicon etching, lining with dielectric layer for electrical isolation and super-conformal filing with copper. It has been reported that Cu-TSV can exert thermo-mechanical stress on Si due to coefficient of thermal expansion (CTE) mismatch. This stress can result in undesired device mobility variation and structural reliability. In addition, TSV parasitic capacitance has the most predominant impact on the circuit operation. It is therefore imperative to reduce the TSV stress and capacitance. One solution is to use low-*k* dielectric as the liner since it has much lower elastic modulus and effective permittivity. In this work, low-*k* dielectric is successfully integrated in TSV as a liner. The implications on TSV stress, capacitance and leakage current are discussed. Due to its smaller elastic modulus (~7.2 GPa), the selected low-*k* carbon-doped oxide acts as a compliant layer to cushion the Cu-TSV stress on the Si compared with conventional oxide (75 GPa) by plasma enhanced chemical vapor deposition. This effectively reduces the near-surface compressive stress in Si by >25% compared with the conventional liner which is more rigid. Since the low-*k* liner has an effective dielectric constant of ~2.8, it is found that the integration of the low-*k* liner reduces the TSV capacitance by ~26% as compared with the conventional oxide liner. In summary, this work has provided evidence of the technical merits of a low-*k* material to mitigate the undesired Cu-TSV induced stress in the surrounding Si and the related parasitic capacitance.

## Key words

Capacitance, low-*k* dielectric, thermo-mechanical stress, through silicon via (TSV).

## I. Introduction

Through silicon via (TSV) has emerged as an essential enabler for the next generation of integrated circuits and systems for continuous performance growth ("More Moore") and functional diversification ("More than Moore"). It is expected to augment Moore's Law scaling and deliver higher degree of functionality in 3D or 2.5D IC. TSV is commonly fabricated by high aspect ratio deep silicon etching, lining with dielectric layer for electrical isolation and super-conformal filing with copper [1] hence forming a MOS structure [2]. It has been reported that Cu-TSV can exert thermo-mechanical stress on Si due to CTE mismatch. This stress can result in undesired device mobility variation [3] and interconnect distortion [4]. In addition, TSV parasitic capacitance has the most predominant impact on the circuit operation [5]. It is therefore imperative to reduce the TSV stress and capacitance. One method is to implement TSV with smaller diameter in order to reduce the Cu volume and surface. Since the TSV length (i.e. the Si thickness of the stacked layers) does not scale very well due to challenges in thin wafer handling, one ends up with higher aspect ratio and void free Cu filling process becomes a challenge. In addition, the effective resistance of Cu-TSV increases rapidly. One potentially useful solution is to use low-*k* dielectric as the liner since it has much lower elastic modulus [6] and effective permittivity [7]. In this work, low-*k* dielectric is successfully integrated in TSV as a liner. The implications on TSV stress, capacitance and leakage



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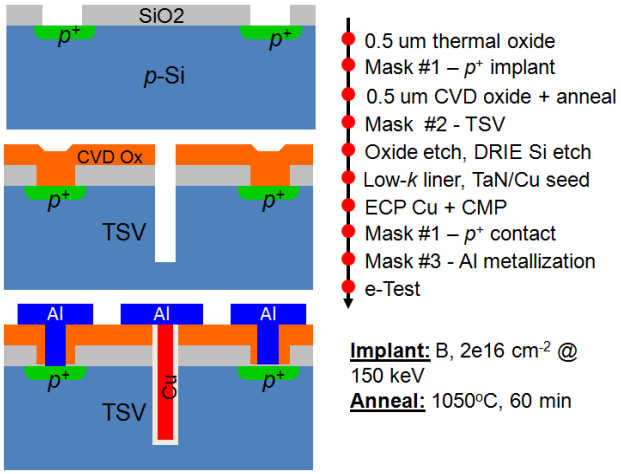


**Fig. 1** Process flow for TSV test structure fabrication. The structure includes a Cu core as gate, liner, and a $p^+$ contact as ground.

current are discussed.

## II. TSV Fabrication and Modeling

TSV (∅=5μm) with an aspect ratio of 1:2 are designed and fabricated on 8'' p-Si wafer using a process flow schematically shown in Fig. 1. This aspect ratio is chosen for ease of fabrication and is sufficient to study the properties of the liner. The TSV is etched by using a BOSCH process in a deep reactive ion etcher (DRIE) using oxide hard mask. Plasma enhanced deposited oxide (PETEOS) as control and Black Diamond low-*k* liners are deposited in PECVD chamber at temperature 400 and 350°C, respectively, with good conformity. Subsequently tantalum (Ta) barrier and Cu seed are sputtered followed by super-conformal Cu ECP filling. The Cu overburden is then removed by chemical mechanical polishing (CMP). Contact holes are opened on oxide layer and Al is deposited and patterned to form contact pads for electrical probing. Note that $p^+$ contacts are made by implantation from the surface for electrical probing.

## III. Results and Discussion

### *A. TSV Fabrication*

TSV with low-*k* liner is fabricated with conformal step coverage. No void or delamination is observed in the Cu core after filling as shown in the scanning electron microscopy (SEM) image in Fig. 2. The chemical composition of Si, low-*k* (carbon-doped oxide, SiOC), and Cu is verified by the corresponding EDX profiles as shown in Fig. 2.

### *B. Stress Modeling and Measurement*

Finite element analysis in Fig. 3 shows the biaxial stress in Si induced by single Cu-TSV along a distance from the TSV edge. Compressive stress is expected in Si as sample is cooled from 200 °C (stress free) to 25 °C. It is clear that low-k liner, due to its smaller elastic modulus (~7.2 GPa), acts as a compliant layer to cushion the Cu-TSV stress on

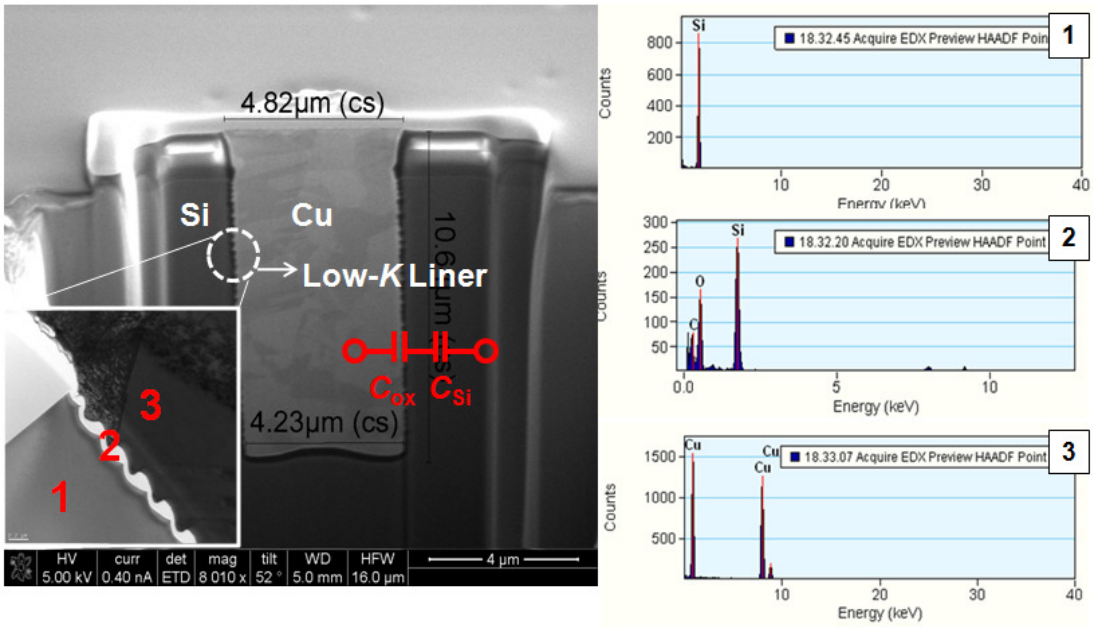


**Fig. 2** FIB images of TSV with diameter of ~4.8 μm and depth of ~10.6 μm. Cu is filled as the core conductor and low-κ dielectric (SiOC) liner is deposited conformally using PECVD at a temperature <400 °C. The EDX signal of each layer (1=Si, 2=Low-κ, 3=Cu) is shown on the right.



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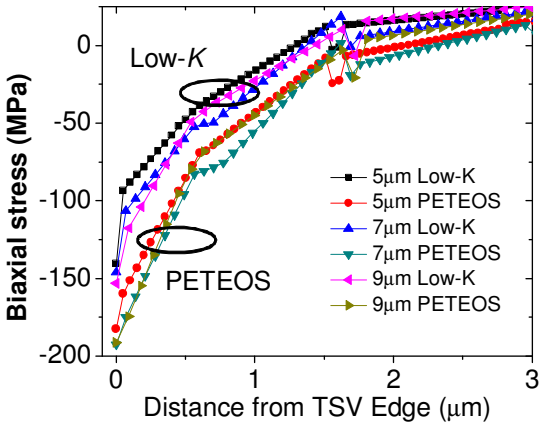


**Fig. 3** (*FEA Simulation*) Thermo-mechanical stress exerted by Cu-TSV on Si as a function of distance from the edge of TSV. The stress free temperature is set at 200 °C and the system is cooled down to 25 °C. The Elastic Modulus for PETEOS and low-*k* is 75 and 7.2 GPa, respectively.

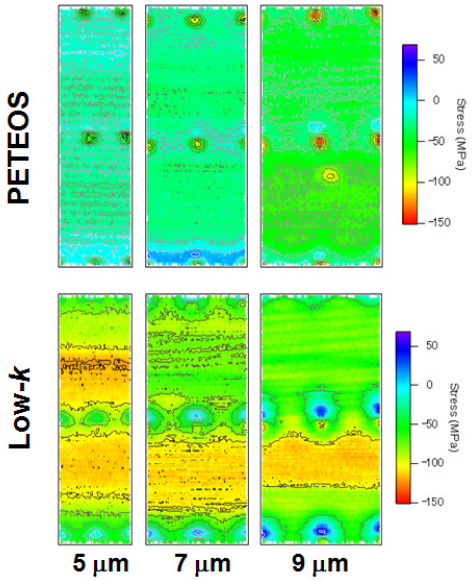


**Fig. 4** Biaxial stress mapping of the Si based on micro-Raman spectroscopy (λ=488nm). Each scanning area consists of 3 TSV in a row with varying diameter and pitch.

the Si compared with PETEOS (75 GPa). This relaxes the keep-out zone requirement. High resolution micro-Raman spectroscopy (λ=488nm) is used to verify the stress exerted on Si by TSV rows (3 TSV in a row) with varying diameter/pitch of 5/5, 7/7 and 9/9 μm. The stress map is presented in Fig. 4. In Fig. 5, stress profile along the TSV row is summarised. It is verified that when low-*k* liner is used, lower compressive stress is exerted by Cu-TSV on

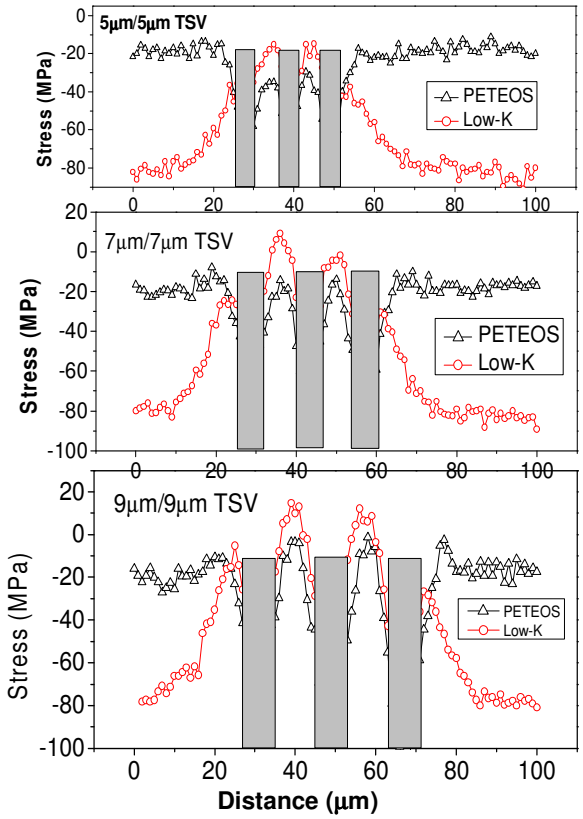


**Fig. 5** Si stress profile along TSV rows from Raman measurement. Each row contains 3 TSV with similar TSV pitch and diameter. The stress profiles show that low-*k* liner is more compliant and can cushion stress exerted by Cu-TSV on the Si (between TSV) more effectively than PETEOS. (*Note: Si stress outside of TSV row is due to the respective liner thin film residual stress on Si. Low-k has larger CTE mismatch with Si, hence larger stress).*

the Si between the TSV.

*C. Electrical Modeling and Measurement*

Fig. 6 shows the measured CV curves for both PETEOS liner and low-k liner at an average thickness of ~205nm. The capacitance changes from accumulation to depletion as the bias voltage increases demonstrating typical p-Si behaviour. The effective dielectric constant of the low-k material is estimated to be ~2.88. The TSV capacitance value (in accumulation) is lowered by ~26% by replacing PETEOS (*k*=3.9) liner with low-k liner. In Fig. 7, *CV* curve of low-*k* liner shows a small reduction in the effective *k* value under various annealing conditions which are applied to control the leakage current (Fig. 8). Annealing is also effective in reducing the density of fixed charge ($Q_f$) as seen from the negative shift in the flat-band



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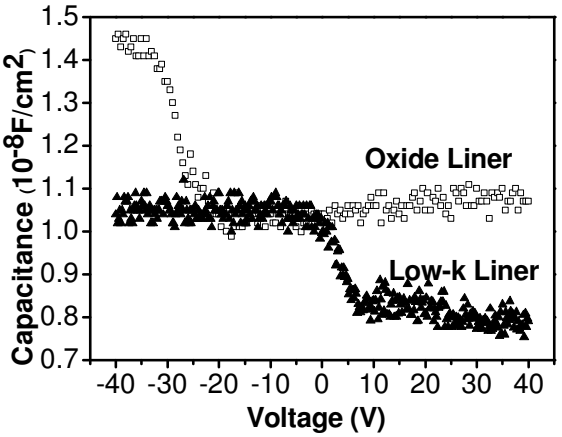


**Fig. 6** *CV* measurement (100 kHz) on TSV structures formed using PE-TEOS oxide liner and low-κ liner. A ~26% reduction in capacitance is obtained by replacing PE-TEOS liner with low-κ liner.

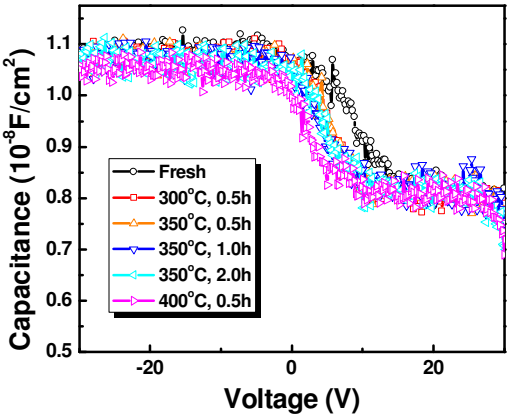


**Fig. 7** *CV* characteristic under various annealing conditions. The flat-band voltage is shifted to the left signifying a reduction in negative fixed charge density. The *k* value changes slightly from 2.88 to 2.85 (300°C and 350°C annealing) to 2.80 (400 °C anneal).

voltage ($V_{FB}$) to ideal value of -0.27V. IV measurement is performed to evaluate the leakage of the dielectric liner and the leakage current at 2MV/cm is presented in Fig. 8. Low-*k* suffers from much higher leakage current as compared with PETEOS liner. Leakage current resistance is further improved by annealing in forming gas ($N_2/H_2$). Anneal at 350°C/2h or 400°C/0.5h is effective to reduce the leakage current to a level comparable with PETEOS. The k value is monitored after anneal to detect any significant change. Based on results in Fig. 7, the *k* value is maintained at an acceptable value after annealing: 2.88

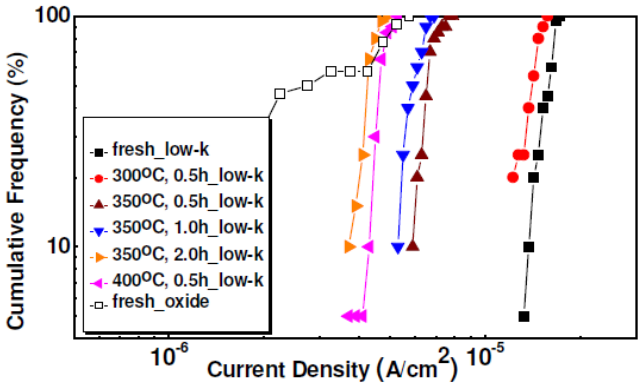


**Fig. 8** *IV* measurement on TSV structure and the corresponding leakage current. Fresh low-*k* liner suffers from high leakage of 1.6e-5 A/cm$^2$ at mid-distribution. Proper anneal can reduce the amount of leakage current (at mid-distribution) to a level similar to that of PE-TEOS oxide.

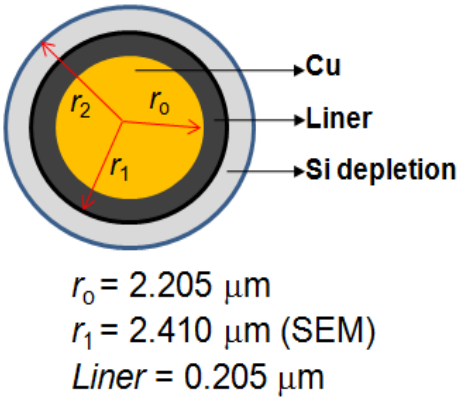


**Fig. 9** TSV forms an embedded MOS structure in the Si substrate and its parasitic capacitance shows distinct accumulation and depletion regions depending on gate (Cu core) voltage and frequency. The minimum capacitance ($C_{min}$) is a series combination of dielectric capacitance ($C_{ox}$) and silicon depletion capacitance ($C_{dep}$).

(fresh), 2.85 (300 and 350°C) and 2.80 (400°C). This slight decrease is beneficial in terms of lower parasitic capacitance.

The measured capacitance values are compared with analytical data based on MOS model [2] (Fig. 9 and Table I). A small discrepancy is seen and this is attributed to the non-uniformity in the liner thickness in actual TSV structure arising from process induced sidewall roughness.

## IV. Conclusion and Summary

It is beneficial to keep the TSV stress and parasitic

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**Table I** Comparison between liner and minimum capacitance value (per unit length) based on analytical calculation and *CV* measurement (for TSV dimension in Fig. 9). Dielectric thickness is set at 205 nm and the substrate doping, $N_a$, is 1e16 $cm^{-3}$.

| | PE-TEOS (/cm) | Low-*K* (/cm) |
|---|---|---|
| Liner Capacitance $C_{ox} = \frac{2\pi\varepsilon_{ox}}{\ln\left(\frac{r_1}{r_0}\right)}$ | 24.4 pF<br>22.1 pF (*CV*) | 17.5 pF<br>15.9pF (CV) |
| Si Depletion radius ($r_2$) $\frac{qNa}{2\varepsilon_s}\left(r_2^2 \ln\frac{r_2}{r_1} - \frac{r_2^2 - r_1^2}{2}\right) = 2\phi_F$ | $r_2$ - $r_1$= 265 nm | $r_2$ - $r_1$= 265 nm |
| Si Depletion Capacitance $C_{dep} = \frac{2\pi\varepsilon_s}{\ln\left(\frac{r_2}{r_1}\right)}$ | 62.4 pF | 62.4 pF |
| $C_{min}$ $C_{min} = \left(\frac{1}{C_{dep}} + \frac{1}{C_{ox}}\right)^{-1}$ | 17.5 pF<br>15.6 pF (*CV*) | 13.7 pF<br>12.1 pF (*CV*) |

capacitance as low as possible for reliability and performance. Low-*k* material is used successfully as TSV liner to reduce TSV stress and a ~26% reduction in capacitance is obtained. However, the leakage current must be carefully controlled.

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