

Chip Last Fan Out as an Alternative to Chip First

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Abstract

Smart phones & other portable devices have dominated Semiconductor growth, and drive IC packages smaller, lighter & thinner, and they continue to integrate more functions in that smaller volume. Besides SOC solutions driven by design houses or system companies, we have seen more packages of Quad Flat Non-lead (QFN), wafer level CSP (WLCSP), and system in package (SIP) being widely used in these smart phones & mobile devices.. Fan out WLCSP (FOWLP) has great potential to be the next new package for the smart phone mobility application.

Two factors have driven fan out WLCSP (FOWLP) package technology in the last few years. The first is the advancing technology nodes which allow the shrinkage of die, allowing more die per wafer. However this comes at the cost of reduced package area for I/Os such as solder ball interconnects. The second and potentially more important factor relates to the demand of the market for more functions. Not all silicon functionality benefits from these advanced nodes, and merely adds to the cost of the die. This has driven the designers to partitioning of desired functionality into multiple die, which in turn requires effective interconnection of these separate die. The packaging technology that has evolved to solve these two situations has been Fan Out Wafer Level Packaging (FOWLP).

Up to date FOWLP used chip first processing, in which the bare die was molded into a wafer shaped carrier with die pads exposed. Typically sputtering is used to provide interconnects to the die pad followed by patterned electroplating of redistribution lines (RDL) to “Fan Out” the next level interconnect pads to regions that can extend on to the molded material beyond the die perimeter. These processes require the use of relatively expensive semiconductor front end classes of equipment and are tailored to handle the reconstituted molded plastic wafers.

We will describe a new alternative to chip first FOWLP, an alternative which meets the needs of a large percentage of the applications requiring a packaging technology such as FOWLP. This new package has been in production in ASE for over a year, and uses a “Chip Last” approach to the problem of increasing useable interconnect pad area. Die which have been bumped with Copper(Cu) Pillars are mass reflowed onto a low cost coreless substrate, followed by over molding which also serves as the die underfill. The Cu pillars allow direct connection to die pads at 50 μm pitch or below, negating the requirement for RDL formation on the die. The use of embedded traces allows for fine lines and spaces down to 15 μm or less, and bonding directly on to the bare Copper. The Cu Pillars are bonded to one side of the Copper trace, and the solderballs or LGA pads are directly on the opposite side of the Copper. This makes the substrate to be effectively only as thick as the Copper used in the traces, and allows the final package to be as thin as 400 μm . Since this uses existing high volume packaging infrastructures, more complex assemblies including multiple die, inclusion of passive components, and 3D structures can be easily implemented. We have designated this package structure “Fan Out Chip Last Package (FOCLP)”

For higher end applications we will show the ability to use a high density substrate process for use in more demanding chip last fan out packages

Key words

Chip First, Chip Last, Fan Out, Wafer Level Package

I. Introduction

Nearly all semiconductor packaging makes use of some form of fanning outward, as the die pad connections are typically fanned out to either leadframes, substrate pads or solder ball connections. An exception is Wafer Level Chip Scale Packages (WLCSP) which are limited to the actual die area, and by this limitation can only be fanned inward. However, the term “Fan out” in recent years has become associated with a form of packaging in which the die is typically reconstituted into a larger molded plastic “wafer” and subsequently processed similar to a WLCSP to “Fan out” the die pad connections to solder ball connections in an area larger than the Silicon die surface area. The majority of these products are manufactured by embedding the die first, with the “fanning out” redistribution layer or layers produced after chip embedding. This type of package technology is often described as a Fan Out Wafer Level Package (FOWLP). This, by definition, is a “Chip First” manufacturing process flow. “Chip First” FOWLP is a process where die are first embedded in mold compound with Redistribution circuitry formed after molding, as shown in Fig.1.

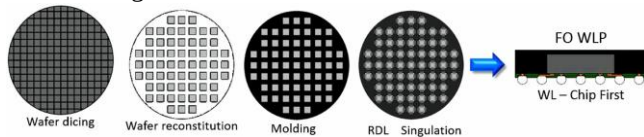


Fig.1 Chip First Process Flow

In contrast, the term “Chip Last” describes a Process where die are first bumped, and then flip chipped onto existing Redistribution circuitry, as in Fig. 2.

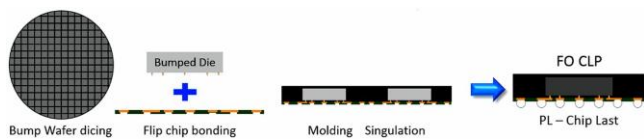


Fig.1 Chip Last Process Flow

II. Drivers for Fan Out

The reasons for using fan out packaging rather than more traditional packaging are mainly for the size constraints imposed by mobile devices, to minimize both X & Y dimensions and thickness of the package.

WLCSPs are the smallest package, but there are reasons that this technology is not always applicable.

As technology nodes advance, die shrinkage is possible

while feature sizes are reduced. However, as the die shrink, the available die surface area may be insufficient for the solder ball array pattern. In this case, fan out provides the additional surface area required, while maintaining the smallest package size, as shown in Fig. 3.

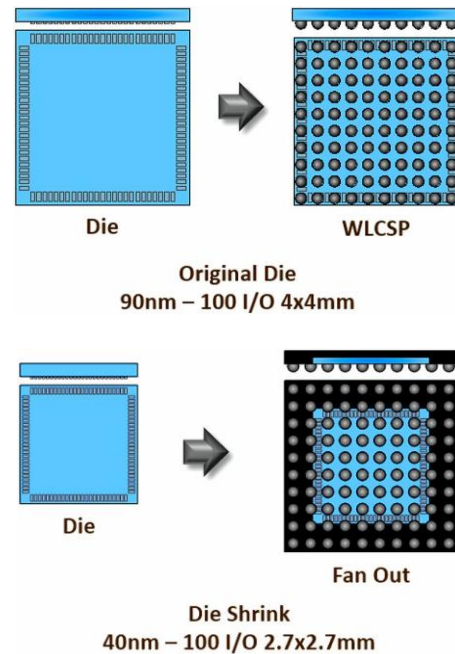


Fig.3 Single Die Fan Out

The consumer market demands more functionality integrated into a single package. With advanced technology nodes, the higher wafer cost and time to market, designers are beginning to partition the design of die from different nodes or different sources.

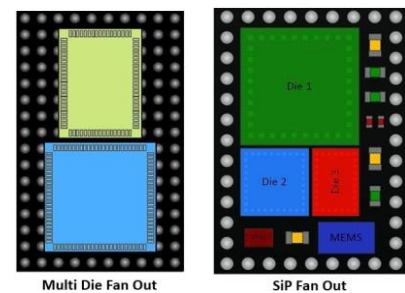


Fig.4 Multi Die & SiP Fan Out

This requires the effective integration of multiple die into small size systems in package (SiP). Fig. 4 shows examples of multiple die fan out and SiP fan out with die and passives combined into the fan out structure.

III. Chip First Fan Out

The process flow for a wafer level chip first product typically utilizes a modified WLCSP line with the addition of specialized equipment for the artificial wafer reconstitution process. Fig. 5 shows a simplified process flow for chip first fan out.

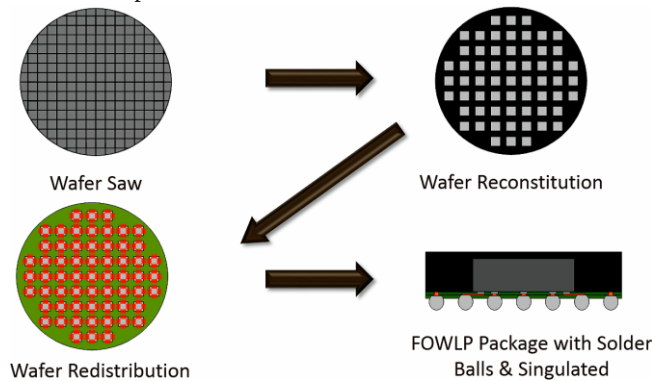


Fig.5 Typical Chip First FOWLP flow

This flow requires a considerable capital investment in wafer level processing equipment for volume manufacturing capacity.

As a result of the wafer reconstitution process, three major difficulties encountered during the manufacturing process are (1) die positional shift due to initial bonder inaccuracies, (2) die movement during molding, and (3) warpage of the plastic wafer.

With chip first processing, the die are placed prior to the redistribution trace formation. As a result, any yield loss during the trace manufacturing results in the loss of good die. For relatively simple packages today, this yield factor is controlled to good tolerable level. As the complexity of the packages increases along with higher trace layer counts, and for advanced nodes, the demand for stringent manufacturing process control and yield learning adds significantly to product and process development challenges, with potential impact to time to market and product cost. We expect that with multiple die in one package the impact will become even more significant. Efforts are underway to implement different versions of Chip First Fan Out packages that utilize panel processing rather than wafer level processing. This would allow for more efficient utilization of processing equipment, and lower cost structures for manufacturing. Materials and equipment are still being developed and optimized for panel processing, as the handling requirements for panels are significantly different than the established wafer processing technologies.

IV. Chip Last Fan Out

We began the implementation of the eWLB chip first fan out process in 2007, and were in production with an 8" wafer line from 2009 to 2012, at which time we discontinued production.

In this paper we shall present an alternate solution to this chip first wafer level fan out process (FOWLP). The solution that we implemented is a chip last process flow. For chip last fan out, all of the trace or RDL routing is formed before the die are placed. This allows the individual package trace patterns to be inspected prior to die placement. As a result, die are placed only on known good circuit patterns. This can result in higher final yields and lower die losses due to trace pattern defects.

We have combined low cost materials and processes to develop a Panel Level chip last alternative to wafer level chip first fan out. Fig. 6 shows a graphic representation of the materials and process factors that combine to provide a new low cost Flip Chip (FC) chip last fan out package that we have denoted as "Fan Out Chip Last Package".

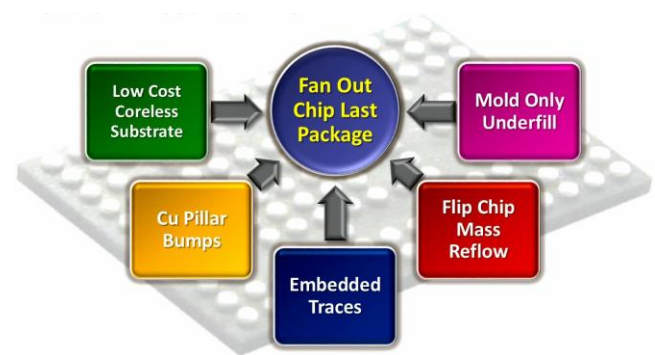


Fig.6 Typical Chip First FOWLP flow

The key to this panel level package is the substrate that provides all the trace or RDL routing described in the previous paragraph. We are able to achieve this with a very simple, low cost coreless substrate that uses embedded traces to enable fine lines and spaces as well as fine pad pitch for Copper Pillar attachment in a panel format. Fig. 7 shows a drawing and actual cross section of the substrate. It is a single layer of Copper with dielectric on one side for isolation and trace embedding.



Fig.7 Coreless Substrate with Embedded Traces

Die are first bumped with Copper pillars, and then assembled to the substrate using a simple mass reflow process, followed by a mold only Underfill and over mold process. This combines the most cost effective material sets and process flows to produce a low cost, very thin chip last fanout package, which has a very good high volume manufacturing track record, as shown in Fig 8.

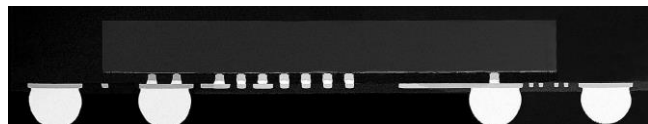


Fig.8 FOCLP Package

If we look closely at the structure, as shown in Fig 9, we can see that the Copper pillars are bonded to the top side of the single 15 μ m Copper layer, while the package solder balls are bonded to the underside of the same Copper layer. This means that the substrate is effectively just the thickness of the Copper layer, with the dielectric layer not influencing the package thickness. For this technology, the Copper thickness can range from 15 μ m to 50 μ m thick.

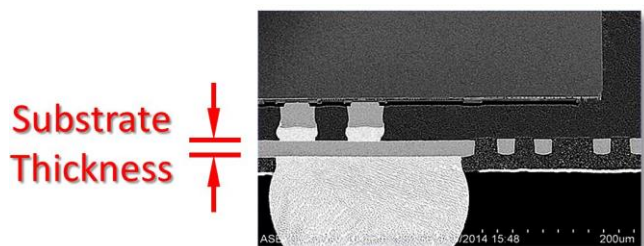


Fig.9 FOCLP Bonding on Copper Layer

Typical dimensions for the FOCLP are shown in Fig. 10. The illustration on the left is not drawn to scale, it is for reference only.

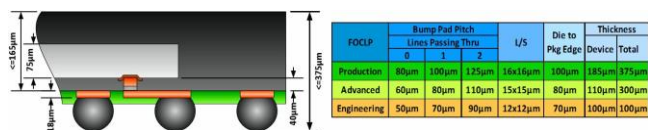


Fig.10 Typical FOCLP Dimensions

The minimum thickness for processing wafer level chip first packages is typically strongly influenced by the warpage of the reconstituted wafer and the difficulties of handling and processing highly warped thin wafers in the wafer processing equipment. They are very sensitive to the ratios of mold compound to die volume. In the FOCLP process warpage is not an issue during thinning. Fig 11 shows the relative thicknesses of FOWLP and FOCLP packages, drawn to scale. The drawing on the left shows the original

eWLB FOWLP package thickness, with the improved “thin” eWLB FOWLP next to it at 0.50mm thickness. As can be seen, the FOCLP can be made significantly thinner, and with a newly developed thinning process, 0.1mm package thickness without the solder balls has been demonstrated.

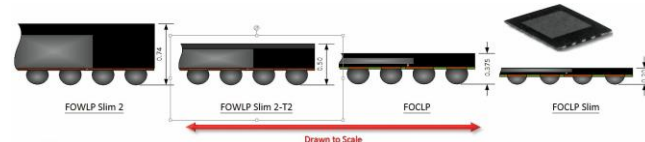


Fig.11 Typical FOWLP & FOCLP Dimensions

In addition to die, any passive components can also be mounted on the substrate using standard SMT assembly. With FOWLP, only passives with Copper cap terminations can effectively be used, limiting the availability of components, and resulting in increased component cost. With FOCLP, combining multiple die and passives can be used to implement System in Package (SiP) assemblies as shown in Fig. 12, shown before molding for clarity.

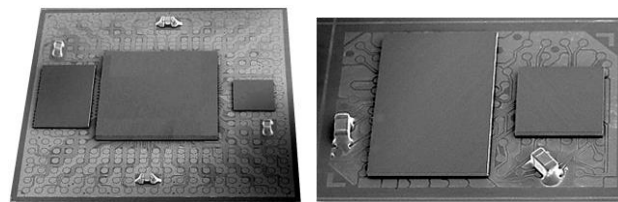


Fig.12 FOCLP with Multiple Die & Passives

One of the main advantages of this panel level FOCLP package is that all of the routing trace circuitry is produced in panel form. It uses traditional substrate/circuit board manufacturing equipment and process flows

Panel Size: 510x410 mm (209,100mm²) X 2 Sides

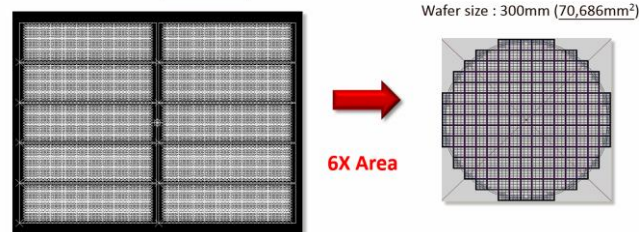


Fig.13 FOCLP Panel Trace vs FOWLP Wafer RDL

This is able to produce the RDL traces at substantially lower cost than using wafer level equipment and processes, as is used in FOWLP. Fig. 13 shows the relative area of the two processes. The option now exists to produce an equivalent package using either FOWLP or FOCLP technologies, as shown in Fig. 14.

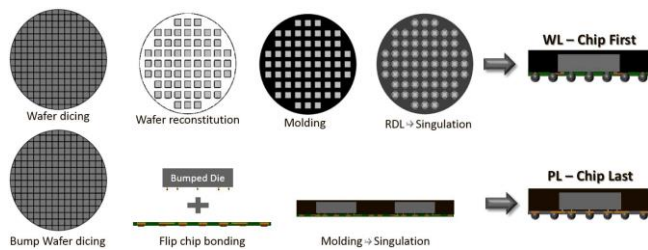


Fig.14 FOCLP & FOWLP Produce Same Packages

Another advantage of the FOCLP technology is that since it is basically an FCCSP, any manufacturing process and structure that is in production today for Flip Chip can be used for this package technology. Fig. 15 shows some of the range of package types that can be manufactured today using existing process techniques.

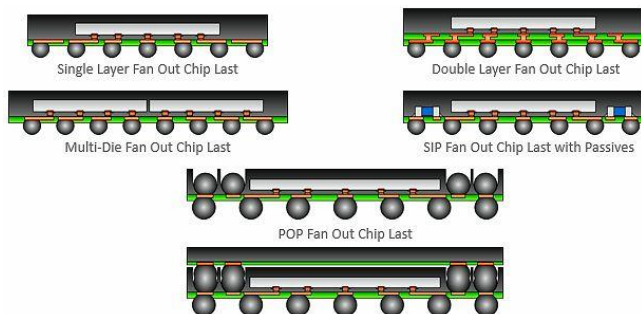


Fig.15 FOCLP Package Variations

Although the FOCLP was intended for applications “fanning out” the die pad connections, it can also be used for certain “Fan In” applications. In situations where the die for WLCSPs is relatively large, for example, more than 6mm on a side, the chip last approach can give a competitive product. As WLCSPs approach 6x6mm, the cost goes up, as there are less packages produced per wafer processed, and the required reliability performance becomes more difficult to achieve. A chip last version would require a perimeter of mold compound determined by the die edge to package edge dimension, currently around 100 μ m, resulting in a package approximately 200 μ m larger than a WLCSP. However, as there is more interest recently in side wall molded protection, this is included in the chip last Fan In (FICLP) design, as shown in Fig. 16.

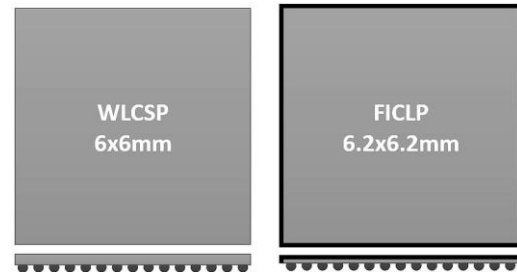


Fig.16 Fan In Version of Chip Last Package

The fan in chip last package can have thicker Copper for higher thermal and current handling capabilities, as well as be thinner than current WLCSP structures.

FOCLPs currently in production have Lines/Spaces (L/S) of 15/15 μ m, with engineering builds at 12/12 μ m L/S, and we expect this technology can be extended to 8/8 μ m L/S. For more advanced packages that may require L/S down to 2 μ m, the same chip last approach is being used with wafer level processing.

Wafer level chip last packages have the same variations of structures as we have shown for the panel version, as can be seen in Fig. 17.

We shall report the Wafer Level Chip Last development in a separate paper.

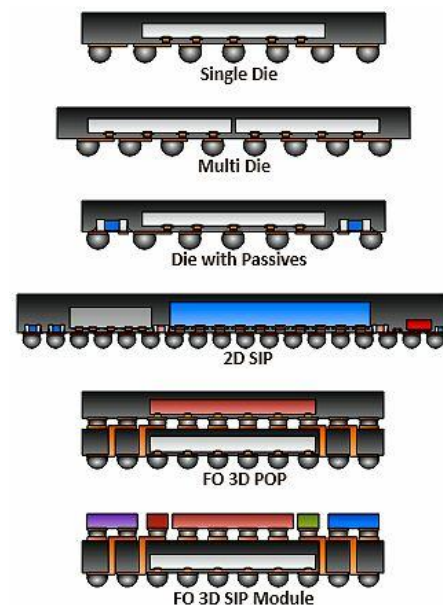


Fig.17 Wafer Level Chip Last Package Variations

V. Conclusion

Chip Last Fan Out has become a viable alternative to the Chip First Fan Out structures, and shows a number of advantages:

- 1) In high volume manufacturing since 2014
- 2) Low cost coreless substrate
- 3) Uses existing FCCSP production equipment and processes, no additional capital investment
- 4) All structure variations are in high volume production; multi-die, passives, POP, SiP
- 5) Can be thinner than FOWLP or WLCSP
- 6) Applicable for Fan Out or Fan In applications
- 7) Higher current & thermal handling capabilities – thicker Copper available

It enables the evolution of small, low cost packaging for mobile and IoT applications from WLCSP to more complex SiP structures, Fig 18.

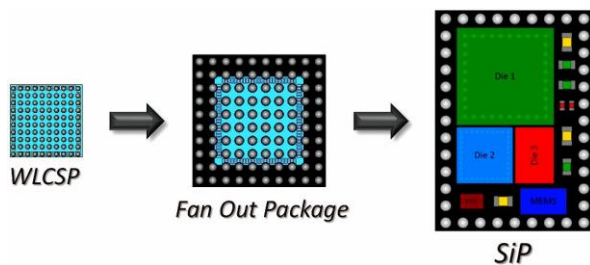


Fig.18 Evolution for Mobile Applications

In summary, we have two potential parallel paths for Fan Out solutions, each applicable for specific customer applications and requirements, Fig 19.

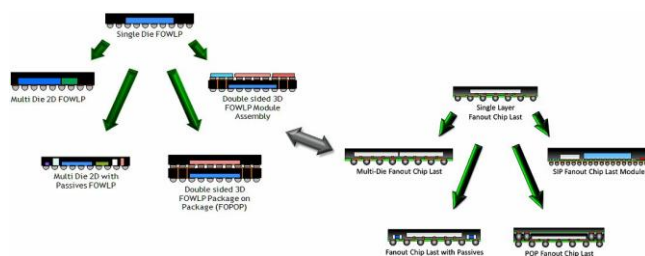


Fig.19 FOWLP & FOCLP Multiple Paths

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