The Growth of Advanced Packaging: An Overview of the Latest Technology Developments, Applications and Market Trends

R. Beica, A. Ivankovic, T. Buisson, S. Kumar, J. Azemar
Yole Developpement
75 cours Emile Zola
Villeurbanne, 69100 France
Ph: +33-472-830-196; Fax: +33-472-830-183
Email: beica@yole.fr

Abstract

The semiconductor industry, for more than five decades, has followed Moore's law and was driven by miniaturization of the transistors, scaling the CMOS technology to smaller and more advanced technology nodes while, at the same time, reducing the cost. The industry is reaching now limitations in continuing this scaling process in cost effective way. While technology nodes continue to be developed and innovative solutions are being proposed, the investment required to bring such technologies to production are significantly increasing. To overcome these limitations, new packaging technologies have been developed, enabling integration of more performing as well as various type of devices within the same package.

This paper will provide an overview of current trends seen in the industry across all the packaging platforms (WLCSP[1], FanOut[2], Embedded Die[2], Flip Chip[3] and 3DIC[4]). Challenges, applications, positioning of the different packaging technologies by market segments (from low end to high end applications) and changes of the markets and drivers, growth rates and roadmaps will be presented. Global capacities and demands and the landscape of the packaging industry will be reviewed. Examples of teardowns to illustrate the latest packaging techniques for various devices used in latest products will be included.
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Keywords

Advanced packaging, wafer level packaging, fan-in, fan-out, TSV, 3DIC, embedded technologies, flip chip, forecast, and roadmaps

I. Introduction

The semiconductor industry, for more than five decades, has followed Moore's law and was driven by miniaturization of the transistors, scaling the CMOS technology to smaller and more advanced technology nodes while, at the same time, reducing the cost. The industry is reaching now limitations in continuing this scaling process in cost effective way. While technology nodes continue to be developed and innovative solutions are being proposed, the investment required to bring such technologies to production are significantly increasing.

To overcome these limitations, new packaging technologies have been developed, enabling integration of more performing as well as various type of devices within the same package.

A significant level of activities is currently taking place in advanced packaging, from development and innovation of new technologies to introduction to the market and commercialization. This is driven by the need of further miniaturization (smaller form factor and lightweight technologies, lower profiles), increased performance (higher pin count devices, higher speed, wider bandwidth capability, lower power consumption, etc.), increased functionality (integrating disparate technologies, devices within the same package) and lower cost.

Today, there are several different approaches available in the industry when it comes to advanced packaging, such as: platforms using encapsulation based technologies (MEMS and sensors, wafer level optics), packages where electrical redistribution is performed within the die (fan-in) or outside the die (fan-out), embedding dies within organic substrates, flip chip bumped packages using an intermediary substrate and stacked devices using through-silicon-via interconnect technologies. The suitability of each of these platforms and market adoption will depend on the final product and application needs.

II. Market Drivers and Evolution of Advanced Packaging

The computing trends have evolved over the years from wired based to wireless systems, driven by increasing needs of mobile applications, and more recently, the emergence of internet of things and cloud. As a result, products have evolved not only in terms of volumes produced and sold, but also in diversity of products developed to address the requirements of various applications, from consumer, to industrial, medical, transportation, defense and aeronautics, etc. If performance and somewhat cost, as shown in figure 1, were the primary success parameters considered for main-frame computers, later cost becoming critical especially with adoption of computing into the consumer market, with increasing needs of mobility and connectivity, the complexity in requirements, in terms of key success parameters, have increased. Beside cost and performance, now equally important are parameters such as lower latency and increased bandwidth density, low power consumption and small form factor.

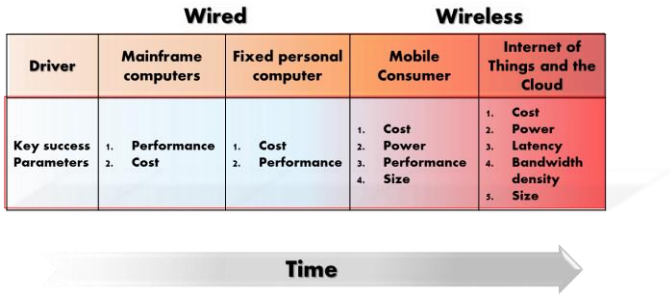

Figure 1: Key Success Parameters [5]

If miniaturization of the features have evolved quite rapidly on the ICs (silicon side), enabled also by Moore's Law, the processing capabilities and reduction of features on the PCB side have advanced at much slower rate. As a result, as shown in figure 2, the gap between the features and pitch sizes on the ICs and PCBs, over the years, have increased creating new opportunities for the packaging community to develop innovative solutions and address this gap. The incorporation of more advanced IC substrates, building multiple layers and redistribution lines, fanning out the interconnects to accommodate increased I/Os, replacing wirebonding with alternative technologies such as bumping and Cu pillars to further enable smaller pitch sizes, stacking dies using more advanced interconnect such as through-silicon vias for increasing performance and enabling heterogeneous integration and miniaturization, embedding dies into the substrate to address security concerns and form factors and packaging multiple dies or packages within the a system are some of the major packaging trends seen in the industry over the years that laid the foundation of new advanced packaging platforms.

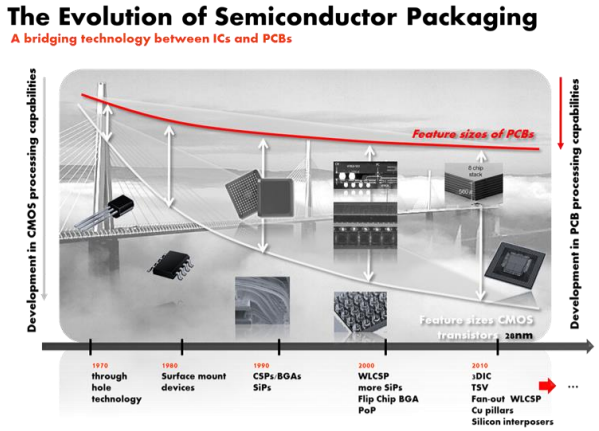

Figure 2: The evolution of Semiconductor Packaging. A bridge between ICs and PCBs [1]

II. Advanced Packaging Platforms

The Advanced Packaging technologies have increased in complexity over the years, transitioning from single to multi-die packaging, enabled by 3-dimensional integration. As shown in figure 3, there are several advanced packaging platforms today with high interest in the industry:

- *QFNs:* although this type of package have a low level of complexity (by some may not necessarily be considered an "advanced" packaging solution), is a very mature platform, with low cost and reliable. One of the main applications, especially for the most advanced QFNs, is RF Packaging, due to also its flexibility in handling various materials and enabling high frequency packages.
- *Fan-in:* also a mature technology fan-in wafer level packages (also known as wafer level chip scale packaging WLCSP), continue to have an important presence between the various packaging platforms. Due to its low cost and form factor, there is no surprise that several organizations continue to adopt this platform for devices with less performance needs (lower I/Os) or further try to improve and develop new solutions based on this platforms to extend its applicability to higher I/Os.
- *Fan-out:* an advanced packaging platform that is embedding devices in molded compounds enabling redistribution of the interconnects beyond the die size, thus way enabling incorporation of higher number of I/Os and applicability of this platform to a wide range of devices and markets. Although a platform which has already been adopted in production for a few years, it is still considered an

emerging market, with several players entering the market with their own proprietary solutions.

- *Flip-chip:* an older technology, firstly introduced in 1960 by IBM, has significantly evolved since its adoption. It is using an advanced substrate and redistribution lines to enable higher number of I/Os than typically will be obtained with lower cost platforms such as fan-in. Interconnect metallurgy used for flip-chip packages ranges from solder bumps (initially leaded but strongly transitioning to phase out the lead due to environmental concerns and regulations), Cu pillars (enabling further pitch reduction) and gold bumps.
- *2.5D and 3DIC:* stacking dies either using or not an interposer continues to be at the fore-front of the industry as one, if not the most advanced packaging technology. It has been adopted in production for CMOS Image Sensors and MEMS for several years already, followed by FPGA products and more recently memories and GPUs. It has shown to have the ability to significantly increase the bandwidth density, reduce power consumption and form factor compare with traditional packaging technologies.
- *Embedded die:* embedding dies in substrates has the objective of enabling higher integration by placing the die within the substrate layers, taking advantage of the low manufacturing cost of the organic substrates. Although a promising platform, due to several challenges, such as multi-sourcing, lower yields in general with substrate manufacturing, new supply chain, etc – it has not reached high volume adoption yet, however, the industry is currently working on removing these challenges and move this platform to wider market adoption.

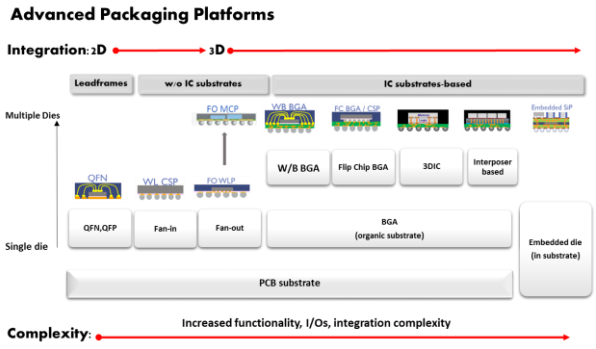

Figure 3. Advanced Packaging Platforms [3]

Several packaging technologies are available in the industry today to address a wide range of market requirements, from low to mid and high-end markets. When choosing the packaging technology, typically the most mature and established platforms will be considered at first, and even extended, if that possibility exists, as it currently happening with fan-in platform, before new technologies are adopted.

III. What Are The Highest Growing Advanced Packaging Platforms?

Increased performance and functionality, miniaturization and low cost are all key drivers for Advanced Packaging. Which packaging platform is winning, will be highly impacted by market trends, the high volume applications, availability of packaging technologies to meet market drivers and the necessary supporting supply chain to support its manufacturing. From the main advanced packaging described, Yole continue to see a high interest in fan-in, fan-out, flip-chip and 3DIC. Embedded die is a promising platform, however, the remaining challenges will continue to keep this platform still at a small volume in the near future.

High volume applications will continue to be consumer based products (smartphones, Internet of Things, starting with wearables). In a recent teardown analysis of the top smartphones, performed by SystemPlus Consulting (part of Yole Group), it was found that, in average 30% of the packages are still using fan-in (as shown in figure 4):

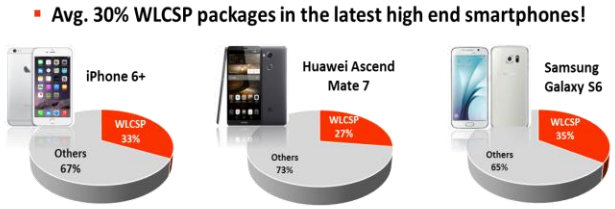

Figure 4: WLCSP in the latest high end smartphones (SystemPlus Consulting)

It is not really a surprise that such a high percentage it is still held by fan-in; this platform has a strong appeal due to its unmatchable advantages such as reduced form factor and low cost. These are the main reasons several players are trying to further extend the applicability of this platform to newer application.

As a result of a recent global market study performed by Yole Developpement, it was found that demand for fan-in is reaching available capacity. Fan-in market in 2014 was close to $3 billion and is expected to further grow, with an 8% annual growth rate, in the next 5 years. Besides analog and mixed signal devices, which are the dominant ones being packaged using this platform, wireless and more recently, new applications such as MEMS and CMOS Image sensors have adopted fan-in. Automotive radar and

gas sensors have been identified as new applications on the horizon.

One of the main disadvantages with fan-in packaging is limiting the I/Os to the size of the die, therefore this platform is more suitable for small packages with low I/Os. When higher number of I/Os are needed, alternative packaging platforms, such as flip-chip, fan-out, 3DIC are needed.

Flip chip assembly technologies (which consist of a die flipped and connected to an IC substrate) have been around for a couple of decades already. Due to several benefits that it brings, such as ability to accommodate high I/O numbers, fine pitch interconnections with superior electrical and thermal performance across various devices, this packaging technology has been widely adopted across various markets. A recent market study of the flip chip market performed at Yole Developpement is showing that the interest of the industry in flip-chip will continue. The market is estimated to reach a $25 billion market value by 2020, supported by wide adoption of Cu pillar technology. The market will be driven mainly by mobile-wireless, consumer and computing applications, including LED and CMOS Image sensor adoption and further growth.

When looking at the cost of making a flip chip, the largest cost (around 35%) is attributed to the substrate (as shown in figure 5)

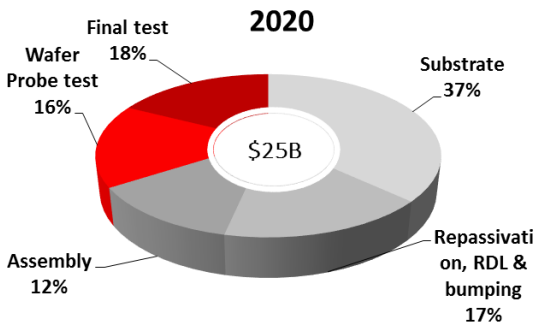

Figure 5. Flip Chip cost structure estimation for 2020 [3]

Besides cost, the substrate also contributes to the total thickness of the package, therefore, alternative technologies that could incorporate higher I/Os within thinner packages and lower cost, will challenge this market. This is what currently is happening with the fan-out technology. Initially developed by Infineon (known as eWLB technology) and Freescale (RCP technology), fan-out has evolved in many more varieties, with the entrance of the major OSATs and foundry (TSMC). The fan-out technology is based on embedding a die into a molding compound and redistributing the I/Os to the outside of the die. The redistribution lines can be achieved either before or after attaching the die using a chip last or chip first approach respectively. Current products using fan-out are mainly based on eWLB technology (a chip first approach), licensed and produced by two main OSATs: STATS ChipPAC and Nanium. With the entrance of ASE, SPIL and Amkor with a chip last approach, as well as Deca Technologies and TSMC with a chip first approach, the competing landscape of this market it intensifies. Fan-out market expected to become a very dynamic and high growth market in the next few years. TSMC preparation for mass production of their fan-out technology (inFO) for Apple's A10 processor, starting in mid-2016 are driving large capital investments. The entrance of TSMC in this market will also significantly impact the market growth, as shown in figure 6, a recent update of the fan-out market forecast performed at Yole:

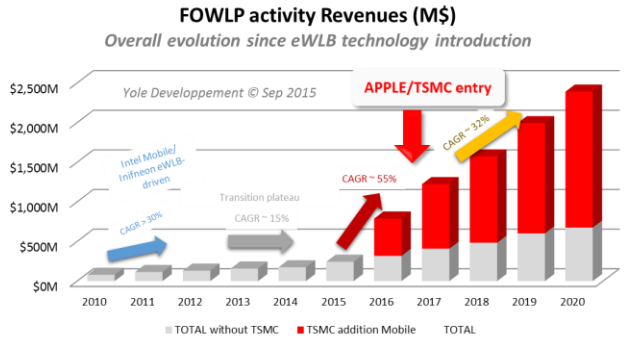

Figure 6: Fan-Out Market Forecasts (2010-2020) [6]

Estimated to be a market of only $174 million value in 2014, with the increase in adoption and entrance of TSMC, the fan-out market is expect to have the highest growth out of all the packaging platforms, exceeding $2 billion market by 2020.

Another emerging advanced packaging technology with high interest in the industry is 3D integration (3DIC). 3D Integration is a vertical stacking of devices using through-silicon-via (TSV) interconnect for both mechanical and electrical connections. The two major architectures using 3D Integration with TSV interconnects are 2.5D (using a silicon or glass interposer) and 3D IC (devices are stacked without using interposer). 3D integration with TSVs can bring several benefits when compared with 2D or 3D packaging using traditional interconnect and packaging technologies (wire-bonding or package on package). It enables higher memory bandwidth, lower power consumption, reduced form factor and cost. Although cost is still a concern, especially for cost sensitive applications, it is expected to bring cost advantages as well, once adoption at larger scale and higher volumes are reached. [7]

Adoption of TSVs have started with CMOS Image Sensors, which continues to be the main application using 3D stacking and TSVs. Initially using a simply via last through-silicon via interconnect for front-side imagers, it has transitioned to back-side imagers and hybrid imagers where the pixel now is connected using full filled vias with

the digital signal processing unit, as shown in the figure 8 below:

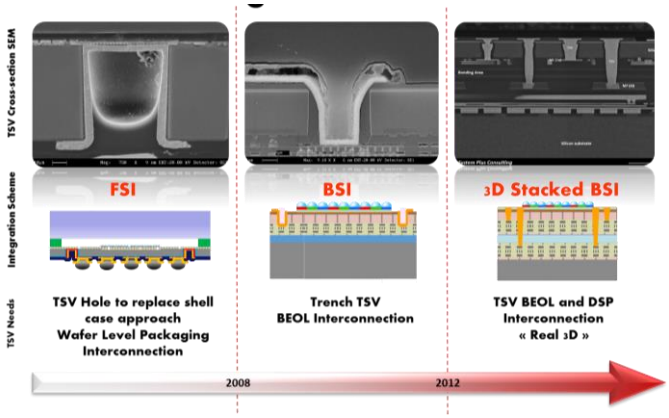

Figure 8: TSVs for CMOS Image Sensors [7]

After CMOS IS, 3DIC has been adopted for MEMS, with several players devleoping their onw technologies, FPGA with Xilinx and Altera and more recently various memory makers starting production, mainly for high-end applicatoins, high performance computers and servers.

Recent announcements from AMD entering production of the first GPU using the high memory bandwidth developed at SK Hynix, nVidia expected to follow in 2016, Intel entering production in 2016 with the first processor using a stacked memory (in this case the hybrid memory cube from Micron) are all encouraging activities showing promise of wider market adoption of 3DIC. In terms of market value, it is expeted to reach close to $14 billion market by 2019, mainly driven by CMOS Image Sensors for the consumer market and followed by industrial and telecom. [4]

IV. Conclusions

A great variety of packaging platforms are available today. All the packaging platforms are expected to continue to grow, Fan-out and 3DIC being the ones expected to have the highest growth rates.

Fan-in, with a stable growth, will continue to be driven by low cost needs and introduction of new consumer applications with low pin-count.

Flip-chip, although a growing platform, is expected to loose overall market share especially to fan-Out but also 3DIC. Cu Pillar will continue to be the dominant flip chip metallurgy.

Fan-Out, a very promising platforms is estimated to have the highest growth. Currently using wafer infrastructure, can move to panel manufacturing in the future.

2.5D & 3DIC has finally starting production across a wider range of devices and adoption of this technology is expected to further grow.

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