C4 EM and CPI Reliability Benefits and Process Challenges of FBEOL Integration Changes Implemented in Lead-free C4 Products

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Abstract

The introduction of low-k & ultra-low-k dielectrics, lead-free (Pb-free) solder interconnects or C4's, and organic flip-chip laminates for integrated circuits have led to some major reliability challenges for the semiconductor industry. These include C4 electromigration (EM) and mechanical failures induced with-in the Si chip due to chip-package interactions (CPI). In 32nm technology, certain novel design changes were evaluated in the last Cu wiring level and the Far Back End of Line levels (FBEOL) to strategically re-distribute the current more uniformly through the Pb-free C4 bumps and therefore improve the C4 EM capabilities of the technology. FBEOL process integration changes, such as increasing the thickness of the hard dielectric (SiNx & SiOx) and reducing the final via diameter, were also evaluated for reducing the mechanical stresses in the weaker BEOL levels and mitigating potential risks for mechanical failures within the Si chip. The supporting white-bump, C4 EM and electrical/mechanical modeling data that demonstrates the benefits of the design and integration changes will be discussed in detail in the paper. Some of the key processing and integration challenges observed due to the design and process updates and the corresponding mitigation steps taken will also be discussed.

Key words

Chip Package Interactions, C4 Electromigration, Far Back End of Line Process and Design Enhancements, Lead-free Solder Bumps

I. Introduction

Chip package interactions (CPI) related mechanical failures and electromigration (EM) have been the major reliability failure mechanisms in the IC industry for the past several generations. The need for faster, lower cost and smaller devices with higher performance and power requirements has required changes in the chip fabrication and assembly processes that can further exacerbate these reliability issues from node-to-node. For example the introduction of the mechanically weaker low-k and ultra-low-k (ULK) dielectrics for lower capacitance, improved device speed and better signal integrity is one such change that has been done recently that drastically impacted the structural integrity of the assembled chip during reliability testing [1]. Other structural and material changes, such as increasing die size, finer wiring and C4 (controlled collapse chip connection) solder interconnect pitch, more stressful lead-free solder bumps, and the use of organic laminates to support the high performance and lower cost requirements of the newer Si technologies has led to both weaker and more highly stressed parts that are susceptible to early mechanical failures due to solder fatigue, delamination and cracks in the underfill and in the weaker BEOL interlayer dielectrics (ILD) [2-5]. Also, the high power requirements for certain specialized applications of the IC devices has led to the need for increased current carrying capability per solder bump which, if left unmitigated, could lead to early EM failures of the UBM/lead-free C4 bumps due to non-uniform current distributions and increased localized Joule heating.

This paper discusses the design and process integration changes done in the last Cu metal level and the far back end of line (FBEOL) levels in a 32nm technology for improving the CPI performance and C4 EM performance of packaged

modules. Electrical and mechanical modeling done for the early assessment of the process and design changes that were to be implemented for improving the reliability of the 32nm Si chip are discussed in detail. A summary of the reliability data for modules built with the new design and process integration and details of one of the integration challenges faced during the early stages of the unit process development are also reviewed.

II. Predictive Mechanical and Electrical Modeling

A. Mechanical Modeling

Finite element analysis (FEA) was done to predict the impact of the FBEOL hard dielectric (SiNx & SiOx) thickness, the final polymeric passivation via diameter and thickness on the mechanical stresses generated in the weaker BEOL levels built with ultra-low-k (ULK) and low-k dielectric films.

The three dimensional FEA model that is used for predicting the BEOL mechanical stresses assumed a typical large die size chip with eleven BEOL metal levels of which 2 metal levels are in low-k dielectric, 7 metal levels are in ULK dielectric and the remaining metal levels are in oxide. The total thickness of the oxide including the FBEOL dielectric is assumed to be about 3um. Fig. 1 depicts the schematic of the chip stack used in the 3D FEA model.

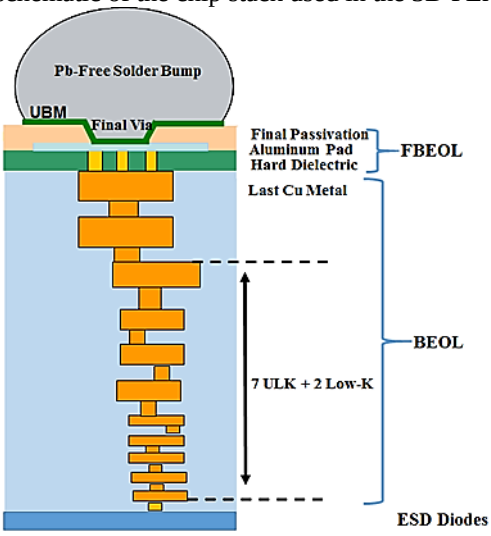

Fig 1. Schematic of the Chip stack used in FEA modeling

The chip is joined to a multilayer organic laminate under typical reflow conditions which involves cool down from the lead-free solder melting temperature to room temperature. The outputs of the model are the peeling stress and principal or cracking stress in the ULK levels underneath a single lead-free solder bump located at the corner of the chip. The peeling stress represents the stress needed to cause a delamination or adhesion fail between the ULK material and the cap underneath or above it, while cracking stress refers to the risk of cohesive fail of the ULK dielectric. Fig. 2 shows the global/local modeling approach that has been used for the prediction of the mechanical stresses in the BEOL ULK levels.

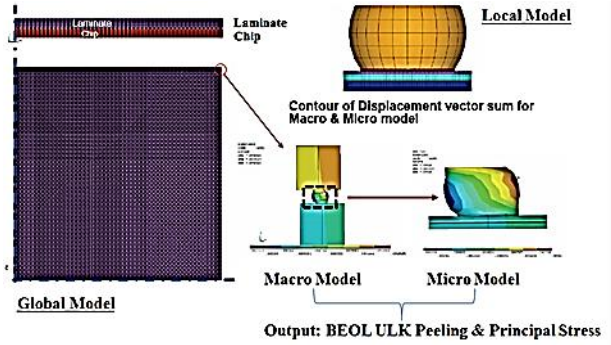

Fig 2. Global & Local Model approach for predicting BEOL ULK stresses

The plot in Fig. 3 shows the effect of increasing the FBEOL hard dielectric thickness on the peeling (adhesive) and principal (cracking) stresses in the ULK levels at a constant passivation via thickness and diameter. The plot shows that both peeling and cracking stresses in the weaker ULK/Low-k BEOL layers are reduced with increasing hard dielectric thickness. When the hard dielectric thickness is increased from 0.5 to 1.4 (relative values) the principal and peeling stresses in the ULK level reduce by 4% and 2% respectively. Further reduction in the stresses by 23% (principal) and 18% (peeling) is observed when the hard dielectric thickness is increased by 2.2 (relative value). All the stress values used in the Fig. 3 are normalized to the peeling stress value for a relative hard dielectric thickness equal to 1.

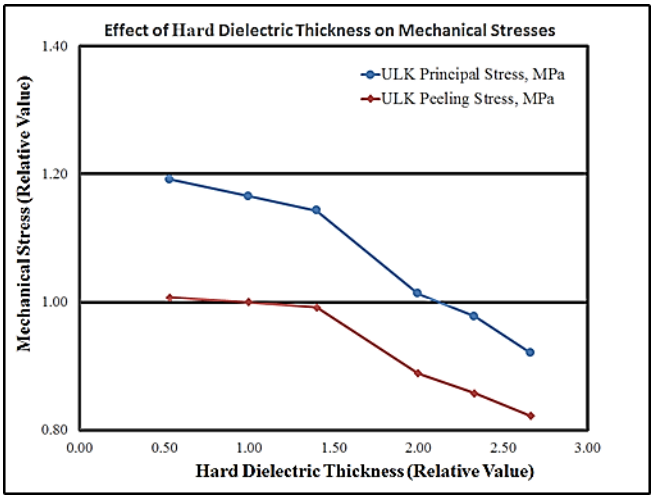

Fig 3. Mechanical Stress in ULK levels as a function of FBEOL Hard Dielectric Thickness

Figs 4 and 5 show the effect of the final passivation via (FV) diameter and thickness on the BEOL ULK stresses.

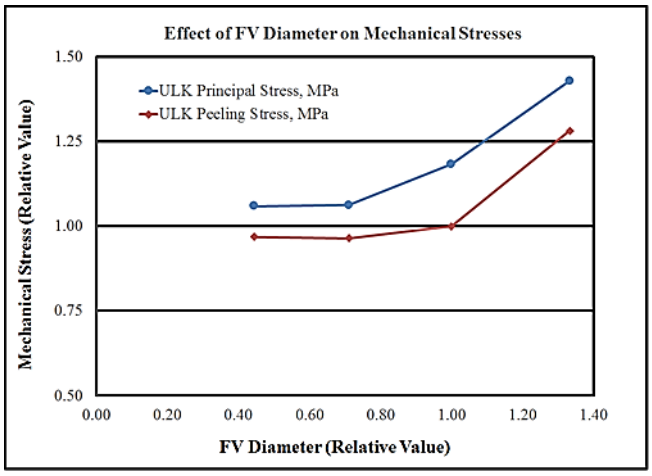

Fig 4. Mechanical Stress in ULK levels as a function of FBEOL Final Passivation Via (FV) Diameter

With a reduction in the FV diameter the ULK principal and peeling stresses are observed to decrease as depicted in Fig. 4. Both principal and peeling stresses drop by 25-26% when the FV diameter is shrunk by 50%. However shrinking the FV diameter further (>50% reduction) doesn't seem to have any more impact on the ULK stresses. Similarly, the peeling and principal stresses reduce with thickening of the final passivation material (Fig. 5). Principal and peeling stresses reduce by 20% and 36% respectively when the relative value of the passivation thickness is increased from 1 to 3.3. However thickening the final passivation by more than 3.3 (relative thickness value) has no further effect on the principal stresses, while the peeling stress increases by about 10%.

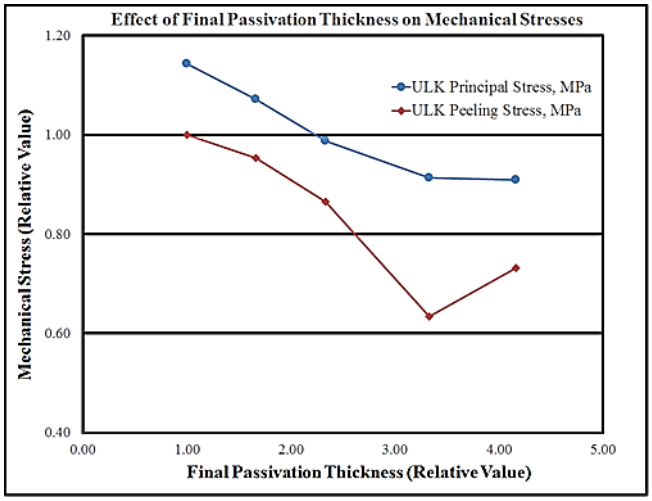

Fig 5. Mechanical Stress in ULK levels as a function of FBEOL Final Passivation Thickness

B. Electrical Modeling

Electrical FEA modeling was done to determine the most optimal designs for the BEOL last Cu metal (LM) pad and the FBEOL hard dielectric via to produce a more uniform distribution of current at the intermetallic interface between the under bump metallurgy (UBM) and solder bump interface. This in turn would help improve the C4 EM performance of the chip when joined to the laminate. Fig. 6 shows the contour plots for the old and new designs. As seen in the contour plots the current distribution is more uniform at the UBM/solder bump interface for the new design in comparison to the old design.

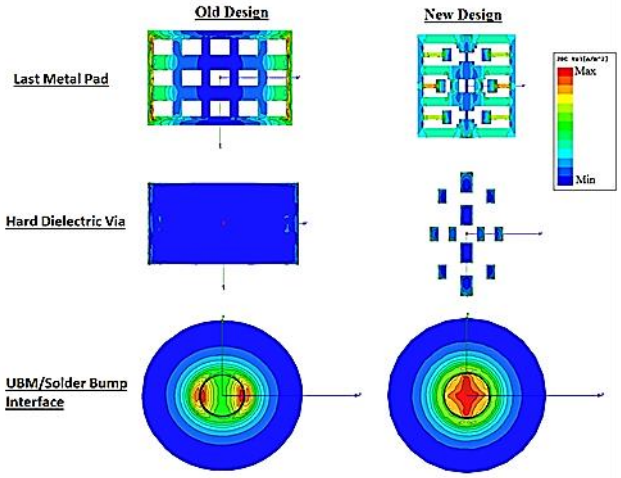

Fig 6. Contour plots comparing current density distribution between the old and new designs at the last Cu metal pad, hard dielectric via and the UBM/solder bump interface

The plots in Fig. 7 show the current density distribution across the UBM diameter in both X and Y directions at the UBM/solder intermetallic interface. It shows that the distribution of the current density is more uniform across the critical interface in both X and Y directions for the new design compared to the old design. The old design has several peak current density points in both X and Y directions, occurring primarily at the edge of the final passivation via. The peak current density induced hot spots occurring at the via corners can lead to localized joule heating which could potentially lead to early EM failures at the UBM/solder interface. In the new design the current is strategically directed to spread more uniformly through the center of the final passivation via thus eliminating any localized joule heating at the solder bump/UBM interface.

The contour plots in Fig. 6 and the current density distribution plots in Fig. 7 indicate that the new designs at the last Cu metal pad and the hard dielectric via help to distribute the current more uniformly which in turn should improve the EM performance of the chip.

The diameter of the final passivation via also plays a critical role in the optimal spread of current through the final via into the UBM and solder bump. Fig. 8 shows the effect of changing the final passivation via diameter on the maximum current density at the solder bump/UBM interface. The plot shows that with up to a 20% reduction in the via diameter there is no change in the maximum current density at the critical UBM/solder bump interface. With a reduction in via diameter by 50% the current density increases by about 5%. However when the final passivation via diameter is further reduced by 60% and 80% the current density increases rapidly by 23% and 75% respectively. Thus shrinking the via diameter by more than 50% could lead to current crowding and localized joule heating at the solder/UBM interface leading to earlier EM failures.

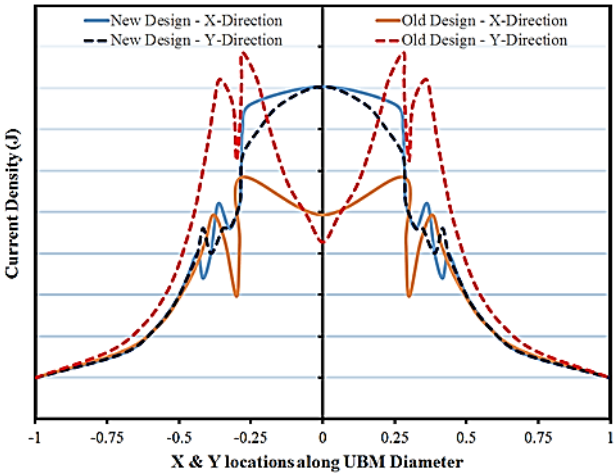

Fig 7. Current density distribution along UBM diameter (X & Y locations) for new and old designs

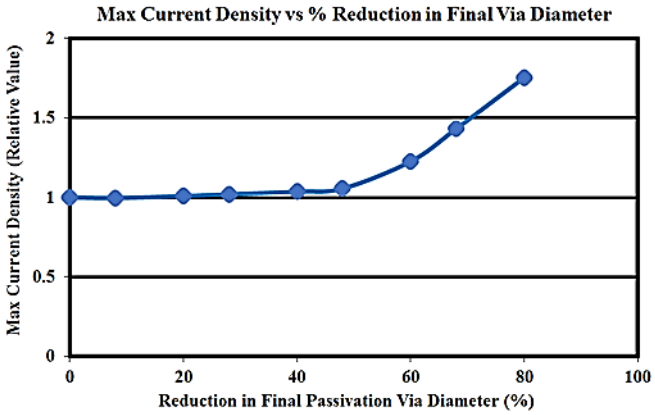

Fig 8. Effect of reducing the final via diameter on maximum current density at UBM/solder interface

III. FBEOL Design and Process Enhancements

For the 32nm node, the FBEOL process integration and design changes were made based on the predictions from the mechanical and electrical modeling for improved C4 EM and CPI performance.

Based on the electrical modeling, the last Cu metal pad and hard dielectric via designs were changed to strategically distribute the current more uniformly through the UBM/solder interface in order to eliminate hot spots that could lead to early EM failures. Furthermore, the redesigned hard dielectric via was filled with Cu by a single damascene process to reduce the resistivity of the Cu filled via and thus help with more uniform distribution of the current into the Al pad, UBM and solder bump.

For improving the mechanical robustness of the Si chip and mitigate any detrimental stresses generated during chip join (flip chip attach) to the laminate from damaging the weaker BEOL layers the hard dielectric thickness was increased by 162% in comparison to prior technology nodes. Fig. 3 shows that increasing the hard dielectric relative thickness from 0.5 to 1.4 reduces the BEOL ULK principal stresses by about 4% and peeling stresses by 2%. The total hard dielectric thickness was not increased further in order to avoid long dielectric deposition times which will impact fab cycle time and also manufacturability of the process. The hard dielectric film used was made compressive by controlling the deposition parameters and deposition rate. Having a thick compressive hard dielectric film also helps to mitigate wafer bow during downstream processing. Fig. 9 shows the final wafer bow measurements done on wafers with the (i) process of record integration thin hard dielectric and thin final passivation (ii) new process integration scheme consisting of thick compressive dielectric with thin final passivation and (iii) integration scheme consisting of thick hard dielectric with thick final passivation. The process of record hard dielectric is a tensile film. As shown in the bar graph the proposed new FBEOL integration consisting of a thick compressive hard dielectric reduces the wafer bow by 67%. The thick final passivation wafer has a 2um thicker passivation in comparison to the wafers with the thin final passivation. As shown in the bar-graph the 2um thicker final passivation increases the bow by about 17% and so it is not desirable to increase the thickness of the final passivation, even though modeling had suggested reduced mechanical stresses at the weak BEOL layers with a thicker film. Excessive wafer bow with thicker passivation films could lead to downstream processing and manufacturability issues due to increased risk of wafer breakage and tool break-downs.

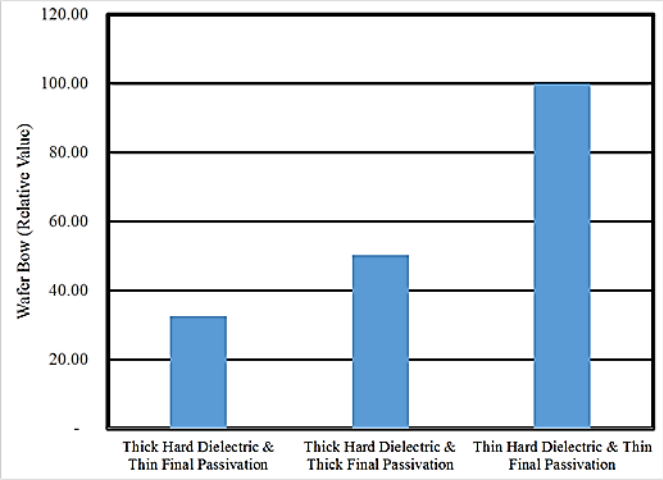

Fig 9. Final Wafer bow (relative value) for Thick & Thin Hard Dielectric and Final Passivation

IV. Reliability Data

A. Chip Package Interaction

Mechanical white bump testing was done on a large die test vehicle to verify the benefits of thickening the hard dielectric for mitigating stresses from the weaker ULK and low-k BEOL levels. The large die test vehicle that was chosen for the white bump testing was built with at least one ULK level and more stressful solder bumps consisting of a thick Cu UBM and lead-free Sn-Ag C4 bumps. The diced chips were joined to the organic laminate under reflow conditions that were chosen to increase the white bump stress. This was then imaged under a Scanning Acoustical Microscope (CSAM) to detect failing C4 bumps. Bumps that have discontinuities or delamination will appear as "White Bumps" in the CSAM images. Fig. 10 shows the plot of percentage modules with white bumps for the case of thick and thin hard dielectric and final passivation. The plot shows that the number of modules with white bumps is reduced from 72% to 18% when either the hard dielectric thickness is increased by 1.25um or when both the hard dielectric thickness and final passivation thicknesses are increased. The thick final passivation is about 2um thicker than the thin final passivation post cure. The ULK material used in the BEOL stack of the modules used in this testing had inherent defects and weakness that made it more sensitive to mechanical failures. This provides a logical explanation for 18% of modules having white bump failures, despite the FBEOL improvements.

Table I is the summary of the CPI data collected since the implementation of the new designs at the last BEOL Cu metal and FBEOL hard dielectric levels along with the process integration updates made such as thicker and compressive hard dielectric and damascene process for metallization of the hard dielectric via. All the modules that were used for CPI testing were subjected to pre-conditioning prior to stressing as per JEDEC standards.

The CPI testing comprised of three accelerated test conditions (a) deep thermal cycles (DTC), (b) temperature, humidity and bias (THB), and (c) high temperature storage (HTS). All 3 tests were done under standard JEDEC conditions. Electrical readouts to monitor continuity and leakage were done before and after pre-conditioning and also at regular intervals on various CPI sensitive structures added to the die and organic laminates. The details of the CPI stress conditions are explained in [6]. The table shows that the parts built with the new designs and process updates have no CPI failures as predicted in the mechanical modeling section.

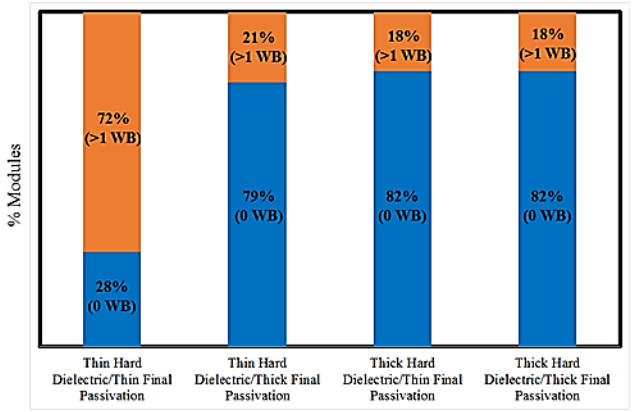

Fig 10. Percentage of modules with white C4 bumps for modules built with (a) thin hard dielectric/thin final passivation, (b) thin hard dielectric/thick final passivation, (c) thick hard dielectric/thin final passivation and (d) thick hard dielectric/thick final passivation

Test Vehicle Details					CPI Data		
Die Size	C4 Pitch	Total Levels of Cu	ULK	Low-K	DTC	THB	HTS
400mm^2	148um	11	N	Y	0/300	0/180	0/164
420mm^2	148um	11	Y	Y	0/45	0/30	0/30
600mm^2	185um	13	N	Y	0/300	0/100	0/100
660mm^2	185um	15	Y	Y	0/45	0/30	0/45

Table I. Summary of CPI Data with new last metal pad & hard dielectric via designs and updated process integration

B. C4 Electromigration

The C4 EM data for modules built with the old design and new design at the last Cu BEOL and FBEOL hard dielectric levels is shown in Fig. 11. As shown in the probability plot the EM performance of the new design is better than the old design.

The improvement is attributed to the design changes as described in the electrical modeling section along with some additional changes made on the solder bump stack such as incorporation of Cu pedestal in the under bump metallurgy (UBM) stack and increase in the percentage silver content of the lead-free solder bumps. These changes have allowed an uplift in the maximum current carrying capabilities of the IBM solder interconnect for high performance ASIC and microprocessor applications.

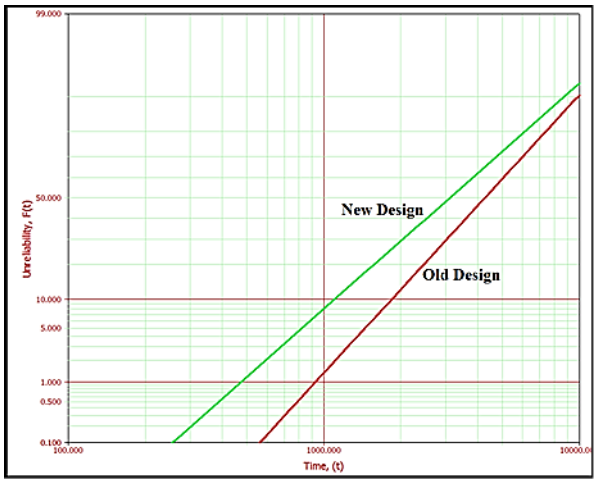

Fig 11. Comparing C4 Electromigration performance of modules built with new and old last Cu metal pad and hard dielectric via designs

V. Process Integration Challenges

Several process challenges were faced during the implementation of the changes that were recommended based on the mechanical and electrical modeling.

The first set of modules that were built with the design and process integration changes discussed in sections II and III had mechanical white C4 bump failures after the standard chip join process. A cross-section of the failed module (Fig. 12) showed delamination between the last BEOL Cu level and the FBEOL hard dielectric. Furthermore, the corners of the via etched in the FBEOL hard dielectric had some amount of undercut which potentially acted as the failure initiation point. Several etch optimization experiments were done by adjusting the power and the flow rate of the gases used during etch and the post etch clean process to fix the undercut at the hard dielectric via corners. Ten modules built with chips that were fabricated with the optimized etch process showed no mechanical failures after DTC. The Si chips used for generating the reliability data in Table I were also built with the new hard dielectric etch process.

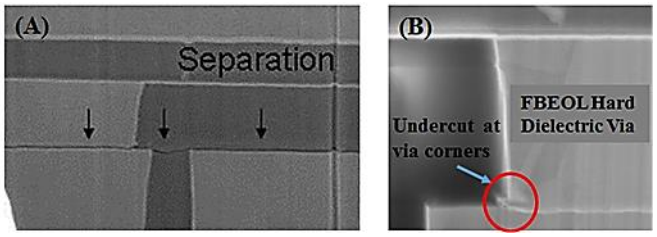

Fig 12. FIB cross-section of the (A) failing module showing separation between the last Cu metal and FBEOL hard dielectric via (B) undercut at the hard dielectric via corners which was attributed to the un-optimized etch process

VI. Conclusion

In this paper mechanical and electrical FEA modeling was carried out to determine the effects of design and process changes done in the last Cu metal pad and FBEOL in order to improve the CPI and C4 EM performance of products in 32nm technology. Reliability testing was done to show there were no CPI issues due to the changes implemented and also demonstrated improved C4 EM performance in comparison to the old design and process. A hard dielectric etch issue was detected early on during unit process development which led to mechanical weakness within the chip was resolved. Limited DTC testing was done to show no mechanical failures with the optimized etch process.

Acknowledgment

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