Study on electromigration in flip chip lead-free solder connections with 40 µm or 30 µm diameter on thin film ceramic substrates

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Abstract

Electromigration comprises one of the processes affecting the long-term reliability of electronic devices; it has therefore been the focus of many investigations in recent years. In regards to flip chip packaging technology, the majority of published data is concerned with electromigration in solder connections to metallized organic substrates. Hardly any information is available in the literature on electromigration in lead-free solder connections on thin film ceramic substrates.

This work presents results of a study of electromigration in lead-free (SAC305) flip chip solder bumps with a nominal diameter of 40 µm or 30 µm with a pitch of 100 µm on silicon chips assembled onto thin film Al_2O_3 ceramic substrates. The under bump metallization (UBM) comprised of a 5 µm thick electroless nickel immersion gold (ENIG) layer directly deposited on the AlCu0.5 trace. The ceramic substrates were metallized using a thin film multilayer (NiCr-Au(1.5 µm)-Ni(2 µm) structure on the top of which wettable areas were produced with high precision by depositing flash Au (60 nm) of the required diameter (40 µm or 30 µm).

All electromigration tests were performed at the temperature of 125 °C. Initially, one chip assembly with 40 µm and one with 30 µm solder bumps was loaded with the current density of 8 kA/cm² for 1,000 h. The assemblies did not fail and an investigation with SEM revealed no significant changes to the microstructure of the bumps. Thereafter seven chip assemblies with 40 µm solder bumps and five assemblies with 30 µm bumps were subjected to electromigration tests of 14 kA/cm² or 25 kA/cm², respectively. Six of the 40 µm-assemblies failed after 7,000 h and none of the 30 µm-assemblies failed after 2,500 h of test duration so far. Investigation of failed samples performed with SEM and EDX showed asymmetric changes of microstructure in respect to current flow. Several intermetallic phases were found to form in the solder. The predominant damage of the interconnects was found to occur at the cathode contact to chip; the Ni-P layers there showed typical columnar Kirkendall voids caused by migration of Ni from the layers into the solder. Failure of the contacts apparently occurred at the interface between Ni-P and solder.

In summary, the results of the study indicate a very high stability of lead-free solder connections on ceramic substrates against electromigration. This high stability is primarily due to a better heat dissipation and thus to a relatively low temperature increase of the ceramic packages caused by resistive heating during flow of electric current. In addition, the type of the metallization used in the study seems to be more resistant to electromigration than the standard PCB metallization as it does not contain a copper layer.

Key words

Electromigration, Flip Chip, Packaging, Lead-free, Ceramic substrate

I. Introduction

Flip chip solder bumping continues to provide a proven and reliable way for interconnecting semiconductor devices (e.g. Si chips) with external circuitry (e.g. printed circuit boards). The ongoing miniaturization of components, larger wafers, thinner packaging, higher levels of integration and environmental legislation pose the major challenges to this packaging technology. They are met by applying progressively smaller solder balls composed of lead-free alloys, which are soldered in ever-shorter distance (pitch) to each other. However, the small dimensions of the solder joints raise concerns in respect to their reliability. In

particular, the performance of interconnects under electromigration (EM) stressing has become a focus in recent years. The majority of published data on electromigration in flip chip lead-free solder joints relates to interconnects on organic substrates (PCBs). There is hardly any information available on electromigration in lead-free solder joints on ceramic substrates; high Pb solders are still used today for interconnects on ceramic [1]. This work presents for the first time results of a comprehensive study of electromigration in lead-free (SAC305) flip chip solder connections with a nominal diameter of 40 µm or 30 µm with a pitch of 100 µm on silicon chips assembled onto thin film Al_2O_3 ceramic substrates.

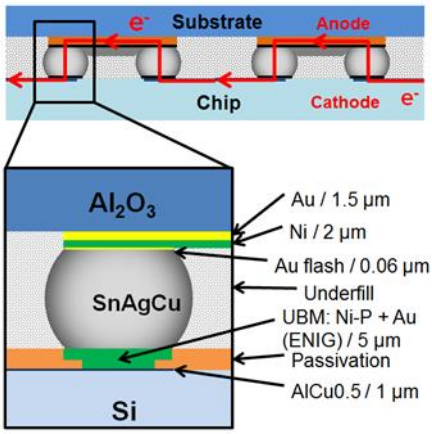
II. EXPERIMENTAL

The test samples and their fabrication have been described in detail in [2-4]. Specially designed, 10 mm x 10 mm x 0.8 mm large silicon chips were assembled onto thin film ceramic (Al_2O_3) substrates by automatic placement and consecutive reflow soldering. The chips had integrated daisy chain connections along their edges for solder spheres of 40 µm or 30 µm, respectively, and a pitch of 100 µm. The total number of IO's amounted to 360 or 352 for the chips with 40 µm or 30 µm solder spheres, respectively. The solder employed for the spheres was Sn96.5Ag3Cu0.5 (SAC305) alloy. Fig. 1 shows the schematic build-up of interconnects. The under bump metallization (UBM) comprised of a 5 µm thick electroless nickel immersion gold (ENIG) layer, which was directly deposited on the AlCu0.5 trace. The Al_2O_3 ceramic substrates were metallized using a thin film multilayer (NiCr-Au(1.5 µm)-Ni(2 µm) structure on the top of which wettable areas were produced with high precision by depositing flash gold (60 nm thickness) of the required diameter (40 µm or 30 µm).

In all the electromigration tests reported here, test samples were placed in an oven which was heated to a constant temperature of T_{oven} = 125 °C. The daisy chains were stressed with a constant current *I*, the current density *J* of which was calculated by dividing the applied current by the area of the UBM metallization of the chip. Individual samples were continuously monitored by an online system during the duration of the tests. The failure criterion has been defined as an open in the daisy chain.

Initially, one sample each with 40 µm or 30 µm solder joints was tested for 1,000 h with the applied current of 101 mA or 57 mA, respectively, i.e. the current density was equal to 8 kA/cm² in both samples. After the test, metallographic cross sections were prepared along the middle of the daisy chains for microscopic investigation.

Optical microscopy and SEM have been supplemented by EDX analysis.



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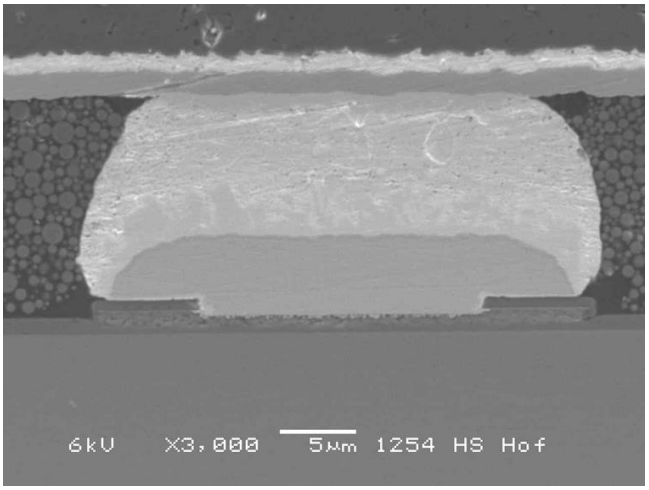

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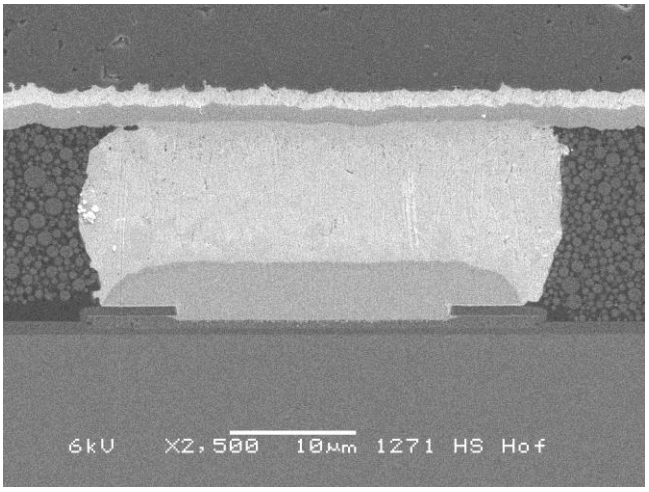


(c)

Figure 1: (a) Schematic view of the cross section of interconnects on ceramic substrates used in this study indicating the direction of electron flow; SEM pictures of a solder connection with 30 µm (b), magnification 3,000X, and with 40 µm (c), magnification 2,500X, solder bumps in initial state (Top: ceramic substrate. Bottom: silicon chip).

Seven samples with solder joints of 40 µm diameter were then stressed with the current of 178 mA, leading to the current density of 14 kA/cm², for the total of 7000 h. Failed samples were subsequently sectioned for microscopic investigation after the test. Before this EM test, temperature increase above the daisy chains due to current flow of different magnitude was manually measured and recorded. Finally, five samples comprising 30 µm solder joints were subjected to EM stressing with the current of 178 mA. The current density was thus equal to 25 kA/cm²; the test was conducted for 2,500 h so far. Unfortunately, these samples had only partially intact daisy chains. Thus, the samples were contacted only along one of the edges of the chips, giving the total length of the daisy chains of only 88 IO's. Table 1 summarizes all test conditions used in this study.

Table 1: Summary of test conditions

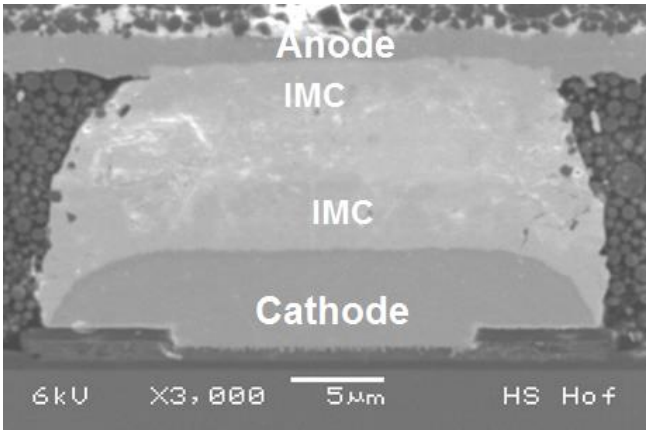
Test No.	T_{oven} °C	Bump Dia. µm	IO count	*I* mA	*J* kA/cm²	Duration H
I	125	40	360	101	8	1,000
		30	352	57	8	
II	125	40	360	178	14	7,000
III	125	30	88	178	25	2,500

It should be noted, that the current density of 25 kA/cm² remarkably exceeds current densities for flip chip solder connections usually reported in the literature.

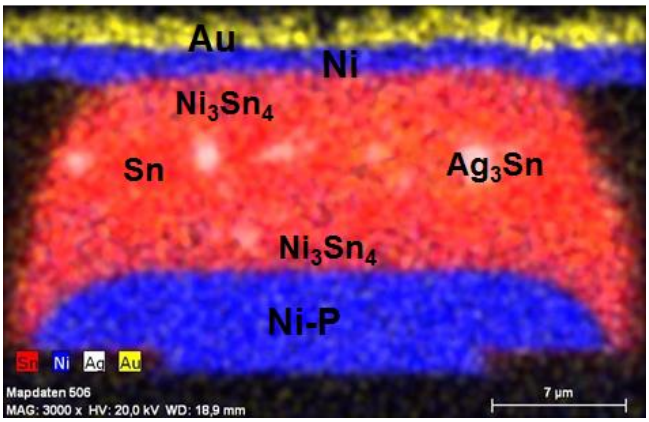
III. Results

The initially tested samples, at the current density of J = 8 kA/cm², sustained the EM stressing without failure. Fig. 2 presents the result of microscopic investigation with a scanning electron microscope (SEM). Fig. 2a depicts a secondary electron image of an exemplary bump with the nominal diameter of 30 µm after 1,000 h EM test. Fig. 2b shows the so-called element mapping on the same bump. No significant damage to the microstructure or deleterious interdiffusion of the elements can be seen in Fig. 2. The distribution of elements resembles in principle that after reflow. No severe damage caused by electromigration could be found after 1,000 hours test time.

EM test conditions: temperature of 125 °C and current density of 25 kA/cm², are regarded as severe. Failure times reported in literature are in the range of 100 h. Therefore it was rather surprising that none of the samples tested in the third test, with 30 µm solder joints, failed after 2,500 h of stressing with the current of 178 mA (current density of 25 kA/cm²). Metallographic investigation conducted on these samples will be presented at the conference.



(a)



(b)

Figure 2: SEM image ((a), magnification 3,000X) and element mapping (b) of a cross section of a flip chip with 30 µm solder spheres on thin film ceramic after 1,000 hours EM test with 8 kA/cm^2 at 125 °C oven temperature.

Six of seven samples tested in the second test (40 µm bumps, I = 178 mA, J = 14 kA/cm²) failed during 7,000 h of test. The average time to failure was estimated using the Weibull distribution. Fig. 3 shows a Weibull plot of failure probability against time to failure for our test results. The mean time to failure (MTTF) was estimated to be equal to 4,800 ±750 h.

The electromigration tests of chips with 30 µm bumps were still in operation at manuscript deadline. Results of failed samples with 30 µm bumps will be presented at the conference.

Fig. 4 displays the results of the measurement of the temperature increase at the surface of the chips caused by resistance heating. The temperature increased nearly linearly with the applied current by an increment of approximately 2 degrees every 25 mA. A current of 178 mA generated a surface temperature increase of about 18 °C, measured with an infrared camera as well as a thermocouple.

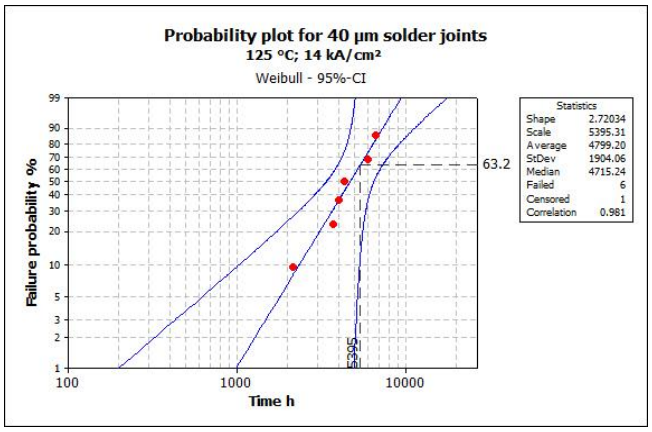


Figure 3: Weibull plot of EM lifetime data for chips with 40 µm SAC305 solder bumps at 125 °C nominal temperature with 14 kA/cm² current density.

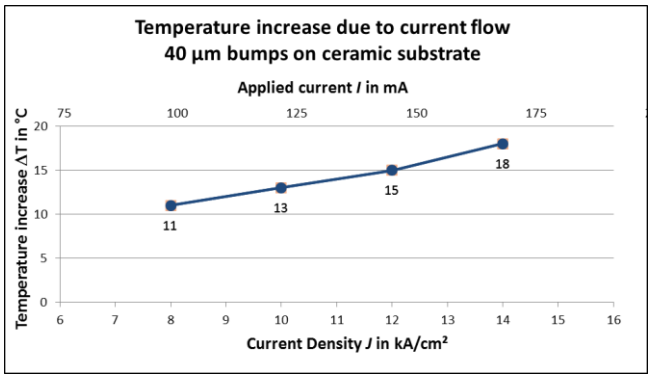
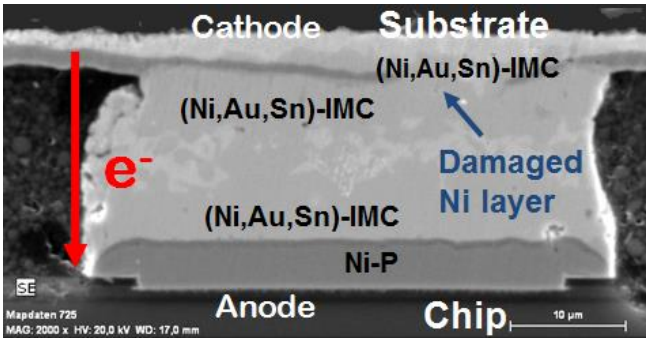


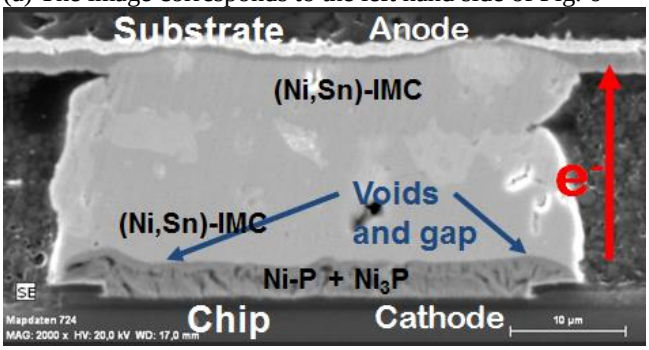
Figure 4: Temperature increase due to resistance heating measured on the surface of a chip with 40 µm solder joints.

Fig. 5 shows a typical secondary electron image of a pair of adjacent 40 µm large solder joints in a sample in which daisy chain failed after 6,022 h of testing (at nominal temperature of 125 °C, applied current of 178 µA or current density of 14 kA/cm²). It is apparent, that the most severe damage has occurred at the cathode contact to chip in the Ni-P metallization layer (right bump). Many columnar (or lamellar) voids in the UBM and a very narrow gap at the interface between the solder and the Ni-P layer can be recognized there. The Ni metallization layer at the cathode contact to substrate (left bump) is damaged as well: a discontinuity, a local dissolution has formed between the solder and the Au layer.

Fig. 6 shows the distribution of Ag, Sn, Ni and Au in the solder joints depicted in Fig. 5. It can be seen, that the electromigration stressing has led to an unsymmetrical distribution of elements. The solder at the right hand side of the images contains more Ni and nearly no Au as compared to the other bump. The bumps have a layered build-up, which is characteristic to a formation of intermetallic compounds (IMC).



(a) The image corresponds to the left hand side of Fig. 6



(b) The image corresponds to right hand side of Fig. 6

Figure 5: SEM images of a typical pair of adjacent ((a) "left" and (b) "right") solder bumps in a sample, which failed after 6,022 h of test.

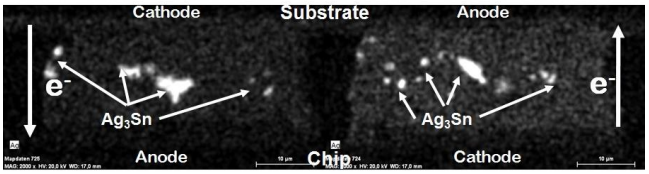


Figure 6a: Distribution of Ag in solder joints of Fig. 5.

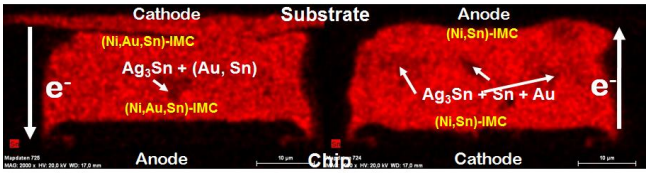


Figure 6b: Distribution of Sn in solder joints of Fig. 5.

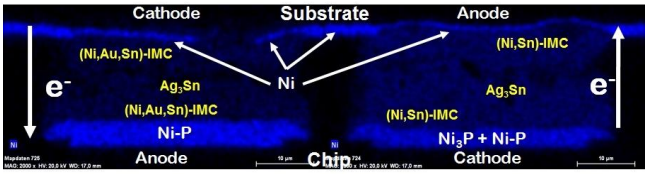


Figure 6c: Distribution of Ni in solder joints of Fig. 5.

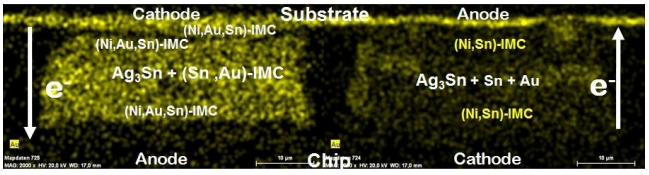


Figure 6d: Distribution of Au in solder joints of Fig. 5.

The compositions in different areas were investigated in SEM with the help of energy dispersive spot analyses. The overall results of these analyses have been marked in the figures. In the Ni-P layer at the cathode contact to chip, increased concentration of P was measured; in some places the presence of the Ni_3P IMC could be assumed. The next layer had a composition close to Ni_3Sn_4 IMC. The same composition was also found at the opposite end of the solder bump. In the center, a Sn rich layer, which contains grains of Ag_3Sn IMC and small amounts of Au, is present. The Ni-P layer at the anode contact to chip did not show any substantial change of its initial composition of Ni and P (concentration of approximately 9 wt. % P). Above this layer there is a layer with the composition of approximately 14 - 17 at. % Au, 20 -40 at. % Ni and 50 – 60 at. % Sn. The same composition has been found also at the opposite end of this solder bump. The layer in the center contains Ag_3Sn IMC grains and its composition closely resembles the $AuSn_2$ IMC.

IV. Discussion

Electromigration (EM) is a diffusion-controlled process that results in mass transport of metal atoms in the presence of electrical current. Solder joints can fail due to EM-induced voiding, Joule heating-enhanced dissolution of under bump metallization (UBM) or substrate metallization, interfacial reactions, thermomigration (TM) induced mass transport, and mechanical stress-related degradation of solder interconnects. All these failure mechanisms occur simultaneously, so that it is usually impossible to distinguish between them. Electromigration occurs at high current density. In respect to solder joints, high current densities occur locally at the entry sites of electrons into the solder corners (see Fig. 7).

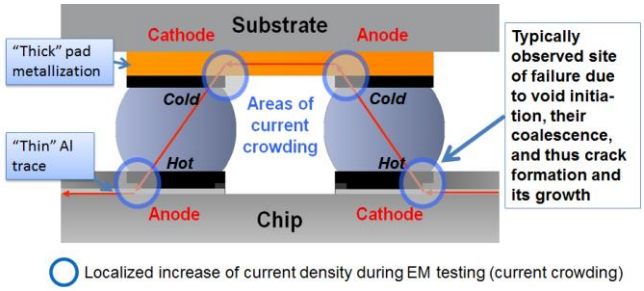


Figure 7: Current crowding and Joule heating in flip chip solder joints.

This is described in the literature as a "current crowding" phenomenon [5]. In addition, on the chip's side, current flows through "thin" Al pads with somewhat higher electrical resistance, which in turn causes a higher temperature increase due to Joule heating there. Due to these two aspects (current crowding and higher temperature at the chip (UBM) side) it is generally observed that EM damage in solder joints is most severe at the cathode contact to chip; this is where solder joints would usually fail [5].

Interfacial reactions between Ni-P, Ni, Au and lead-free solders, in which Sn is the major constituent, have been investigated by many researchers and are well described in the literature, e.g. [6, 7]. The reactions are very complex; only a simplified picture is thus presented here. It is commonly observed in aging experiments that a Ni_3Sn_4 IMC forms at the interface between Ni and Sn. An $AgSn_2$ IMC is often found to form between Au and Sn. Ni-P layers in contact with Sn solders gradually dissolve by diffusion of Ni into Sn of the solder. Columnar Ni_3P IMC, separated by elongated Kirkendall pores, develop in the Ni-P layer as result, see Fig. 14. In solder, Ni forms the Ni_3Sn_4 type IMC. If Au is also present in the system, it can be incorporated into the Ni_3Sn_4 IMC, eventually forming the ternary compound $AuNi_2Sn_4$. Once all of Ni-P has transformed into Ni_3P, a new Ni_2SnP IMC may rapidly grow at the expense of Ni_3P.

At large, the results of our study fit in well with the findings described in the literature. The most pronounced damage has occurred at the cathode contact to chip and this is where the chips have failed. In contrast to the results reported in the literature, however, we did not see any catastrophic reduction of the thickness of the Ni-P layer due to formation of Ni_2SnP IMC. Such catastrophic consumption of the Ni-P metallization is observed when Ni-P was deposited on a Cu layer. Cu seems to promote the dissolution of Ni-P layers and their catastrophic thinning [8, 9]. In our study, we have observed a development of a very narrow separation (gap or crack) at the interface between UBM and solder or inside the UBM, respectively (see Fig. 8). This gap was eventually responsible for the chip failure: an open in the daisy chain. The gap was so small that on cooling down to room temperature failed samples were conducting the applied current again. Fig. 8 shows a fully developed separation through an entire bump.

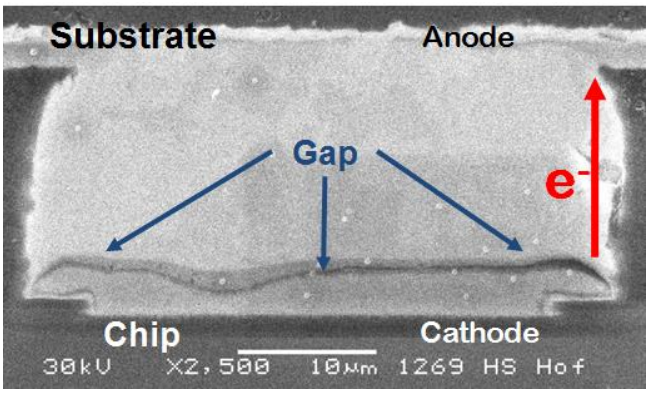


Figure 8: SEM image of a cross section of a chip with 40 µm bumps after 6022 hours EM test with 14 kA/cm^2 (the gap caused the electrical failure of the daisy chain).

It is apparent from the results of microscopic investigation, that the polarity of EM stressing influenced the severity of dissolution of the Ni-P and the Ni layers.
Fig. 9 depicts a cross section of sample with 40 µm solder joints showing Nickel dissolution at the substrate side.

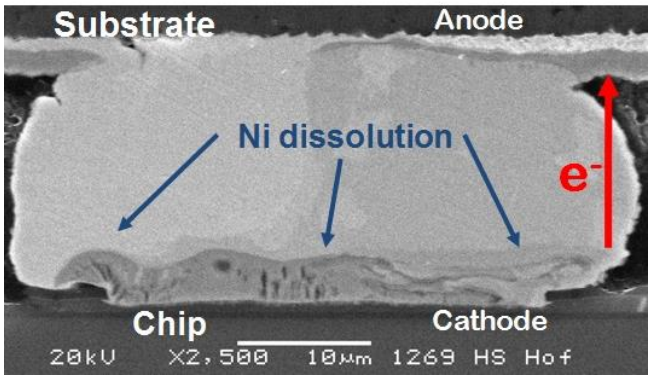


Figure 9: Cross section of a 40 µm solder bump after 2,160 hours EM test with 14 kA/cm^2. Columnar Ni_3P IMC, separated by elongated pores, can be seen.

The dissolution is strongest at the cathode contact to chip (Ni-P layer) or substrate (Ni layer). The diffusion of Ni atoms into the solder is enhanced in the direction of electron flow [10, 11]. This dependency explains the different IMCs seen in our solder joints. EM enhanced diffusion of Ni from the Ni-P layer into the solder in the right hand side bump of the Fig. 6 and the Fig. 5b (cathode contact to chip, bottom right of the figures). At the same time, EM hindered the diffusion of Ni from the Ni-layer into the solder in the same bump (anode contact to substrate, top right of the figures). In result, the Ni-layer (anode contact to substrate) did not dissolve; the only IMCs found in the solder were thus of the type Ni_3Sn_4. These IMCs formed layers along the Ni and Ni-P metallization layers and there was a Sn rich layer in the centre of the solder joint.

Similar IMC layers would have been found in the left hand side solder bump of the Fig. 6 and the Fig. 5a if the Ni layer there (cathode contact to substrate, top left of the figures) had not been locally dissolved. The dissolution, which was obviously enhanced by the EM, led to diffusion of Au from the pad metallization into the solder bump. There, it reacted with the Ni_3Sn_4 IMC layers and the Sn rich layer in the centre. As a result, complex IMCs containing Au, Ni and Sn, presumably $AuSn_2$, $(Au, Ni)_3Sn_4$ and $AuNi_2Sn_4$, have formed. This scenario phenomenologically explains the unsymmetrical distribution of elements in the solder joints.

The most interesting findings, however, concern the resistance of the solder joints to electromigration. Unfortunately, there seems to be hardly any literature on the stability of lead-free solder joint on ceramic substrates. For the sake of comparison, the result of our previous study on electromigration in lead-free bumps on conventional PCBs can be taken into account. The study used the same chip design; the diameter of the bumps was however equal to 60 µm or 50 µm [9]. Among other conditions, EM tests there were conducted at a temperature of 125 °C with applied currents of 141 mA (current density of 5 kA/cm²) for 60 µm bumps or 157 mA (current density of 8 kA/cm²) for 50 µm bumps, respectively [9]. The MTTF for these conditions were experimentally determined to amount to 1,120 h for chips with 60 µm solder joints or 2,416 h for chips with 50 µm bumps, respectively. These values are considerably shorter that the MTTF of 4800 h for the chips with 40 µm solder joints on ceramic substrate tested in this study at a temperature of 125 °C and with a current of 178 mA (current density of 14 kA/cm²). This finding indicates a very good stability of our lead-free solder joints against electromigration. There might be several reasons for this stability. One major cause is certainly related to a lower temperature increase of the bumps on ceramic substrates due to better heat dissipation. Lower bump temperatures slow down the speed of diffusion of the elements in solder joints and prolong the lifetime of solder connections according to Black's equation [13], [14]. Ceramic substrates possess higher heat conductivity than PCBs; consequently they dissipate heat more effectively. The temperature increase measured on chips assembled on PCBs amounted to 20 °C for the current of 141 mA (60 µm bumps) and to 28 °C for the current of 157 °C (50 µm bumps) [9]. From Fig. 6 it can be estimated, that a current of 157 mA would cause a temperature increase of only about 15 °C on chips with 40 µm solder joints on ceramic substrates. It is worth noting, that the current density would then correspond to approximately 12 kA/cm². Yet another cause could be related to the type of metallization used in this study. Neither on the ceramic, nor at the chip side, were Cu layers utilized to provide electrical contact to the solder joints. It is known, that Cu contributes to dissolution of Ni and Ni-P layers and, once in contact with Sn, causes a rapid consumption of solder joints [9, 10]. The absence of Cu layers in our test coupons thus increases the life time of the interconnects.

Finally it should also be mentioned here, that, prior to the EM tests, assemblies with equal structure were subjected to thermal cycling tests [12]. Only one (of eighteen) sample with 40 µm solder joints failed after 4,268 temperature cycles and no additional failures occurred for up to 15,000 cycles -55/+155°C according to MIL-STD883. Flip chips with 30 µm solder bumps sustained 1,000 temperature cycles -55/+155°C according to MIL-STD883 without failure (end of test) [12]. The results emphasize the good overall stability of lead-free solder joints on thin film ceramic substrates.

V. CONCLUSIONS

The study investigated thoroughly for the first time electromigration performance of lead-free flip chip solder joints with the diameter of 30 µm or 40 µm assembled on thin film ceramic substrates. The solder joints showed a very good resistance to electromigration stressing. The cause of the excellent performance is seen in a low temperature increase of the solder bumps on thin film ceramic substrates due to good heat dissipation. The heat generated by current flow (Joule Heating) can be more efficiently dissipated by thin film ceramic than by PCBs. Another cause is concerned with the composition of the UBM and pad metallization used in this study: copper layers were not part of the build-up. There was no possibility for Sn from the solder to react with large amounts of Cu and form harmful (Cu, Sn)-IMCs [14].

The investigation of the microstructure of the solder joints in failed samples revealed a formation of different IMCs and an unsymmetrical distribution of elements due to electromigration. The samples failed at the cathode contact to chip, as expected. An "open" in the daisy chain was caused by a development of a narrow gap at the interface between solder and Ni-P metallization (Fig. 8). (Ni, Sn)-IMCs of the Ni_3Sn_4 type were found to predominantly grow in the solder. These IMCs formed layers surrounding the Ni-P and Ni metallization. In-between these layers, there was a Sn rich layer in the centre of the solder joints. This is also where grains of Ag_3Sn IMC were localized. EM caused a preferential dissolution of N-P and Ni layers at the cathode contact to chip and to substrate, respectively. Dissolution of the Ni-P layer and crack formation has eventually led to an open. The (local) dissolution of the Ni layer at the cathode contact to substrate caused sometimes (e.g. not in every bump) diffusion of Au from the substrate metallization into the solder. In result, (Au, Ni, Sn) - IMCs, presumably $(Au, Ni)_3Sn_4$ and $AuNi_2Sn_4$, as well as $AuSn_2$ in the centre of the bump, have formed.

In summary, our study indicates, that lead-free flip chip solder connections on thin film ceramic substrates withstand electromigration damage very well. The findings my help to develop better and much more reliable flip chip electronic assemblies especially for avionics and other high reliability applications [15].

Acknowledgment

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