# High Reliability and High Performance 30µm Through-Package-Vias in Ultra-Thin Bare Glass Interposer

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## Abstract
This paper presents, for the first time, the thermo-mechanical reliability and the electrical performance of 30µm through package vias (TPVs) formed by Corning in ultra-thin low-cost bare glass interposers and metallized directly by sputter seed and electroplating. In contrast to glass interposers with polymer coated glass cores reported previously, this paper reports on direct metallization of thin and uncoated glass panels with fine pitch TPVs. The scalability of the unit processes to large panel sizes is expected to result in bare glass interposers at 2 to 10 times lower cost than silicon interposers fabricated using back end of line (BEOL) wafer processes. The thermo-mechanical reliability of 30µm TPVs was studied by conducting accelerated thermal cycling tests (TCT), with most via chains passing 1000 cycles from -55°C to 125°C. The high-frequency behavior of the TPVs was characterized by modeling, design and measurement up to 30 GHz.

## Key words
TPVs (Through-Package-Vias), glass interposer, reliability, electrical performance

## I. Introduction
The increasing need for high reliability, high performance and low-cost interposers is driven by two emerging applications: (a) high bandwidth 2.5D and 3D logic-to-memory interconnections, and (b) RF modules for 4G long term evolution (LTE) and 5G mobile networks. Glass, due to its tailorable coefficient of thermal expansion (CTE) and excellent electrical insulation, has been proposed and demonstrated as a superior alternative to silicon interposers for these two applications. Through-package-vias (TPVs) in glass are a key technology building block for such interposers, and via sizes are projected by the ITRS roadmap to scale down to 30µm diameter and 60µm minimum pitch by 2017 for highest I/O density, and reduced parasitic inductance and capacitance [1]. It is necessary to validate the thermo-mechanical reliability and the electrical performance of small TPVs in thin glass interposers.

The thermal characteristics and performance of fine pitch TPVs drilled by Corning were studied [2], but no detailed TCT data was provided. The electrical behavior of TPVs in glass has also been reported [3], but the measurements were limited to frequencies below 10 GHz, which is not sufficient for the aforementioned two applications. More importantly, the process developed for glass interposers in [2, 3] is similar to the process for wafer silicon interposers, which is not expected to meet the cost target for glass interposers. The use of double-sided panel processes involving laminated polymer films on glass to improve handling, followed by drilling TPVs by laser techniques, have been previously reported [4, 5]. The approach presented in this paper differs significantly from the polymer laminated glass TPVs, focusing on direct metallization of TPVs in bare glass. Such an integration process method is application to a number of bare glass TPV formation techniques.

The new process approach in this paper uses physical vapor deposition (PVD) or sputtering to form a conductive seed layer on bare glass with TPVs followed by a standard double-sided semi-additive plating (SAP) process consisting of lithography and copper electroplating steps. The adhesion of copper on the smooth glass surface was confirmed by 90° peel strength testing prior to fabrication of two metal layer glass interposers for reliability and electrical characterization. Two types of glass test vehicles with 30µm TPVs in 100um bare glass were designed based on this

proposed process: one with daisy chains for thermo-mechanical reliability testing and one with electrical transmission lines having via transition for high-frequency testing. The daisy-chain test vehicle was fabricated and subjected to 1000 cycles of accelerated thermal cycling test (TCT) between -55°C and 125°C (JEDEC Standard JESD22-A106B Condition C), while the electrical test vehicle was simulated up to 30 GHz showing very low parasitic inductance and negligible loss.

## II. Process

*A. Adhesion Evaluation*

The smooth glass surface was observed by atomic force microscopy (AFM) with an average surface roughness less than 1 nm. Smooth surfaces are preferred to minimize roughness-induced conductor losses, and this is fulfilled as because the surface roughness is well below 209 nm, the skin depth of Cu at 100 GHz [6]. Another benefit is in performing fine-line lithography, because the UV light will not be diffracted by the smooth surface.

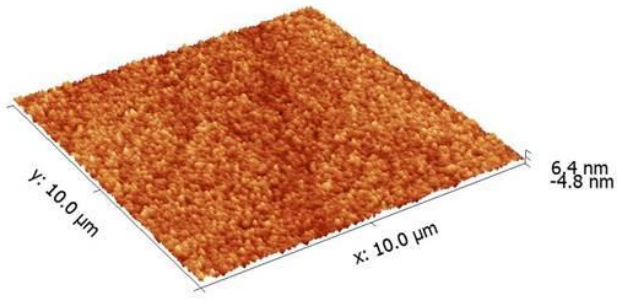



**Figure 1.** AFM image of smooth Corning glass surface.

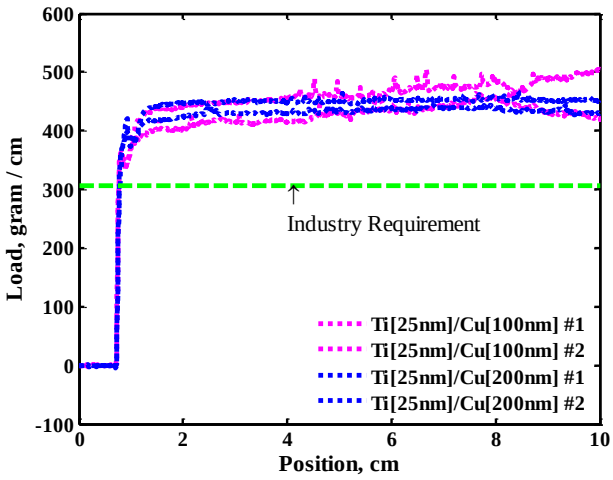



**Figure 2.** Peel strength of 10 µm copper on smooth glass using 90° peel test.

The adhesion of copper to such a smooth surface is challenging due to insufficient contact area of copper to the glass surface. It is already known that sputtering Ti as an intermediate layer to glass and Cu can achieve good adhesion in the semiconductor industry. Thus, sputtering Ti and Cu is exploited to metallize the smooth glass and electrolytic plating is used to increase the copper thickness to 10 µm. Finally, 90° peel testing was conducted to quantitatively evaluate the adhesion of sputtered metal to the glass surface. Two types of seed layers are sputtered: 1) 25 nm Ti / 100 nm Cu and 2) 25 nm Ti / 200 nm Cu. The peel strength results are depicted in Fig. 2, where we can read that for both sputtered seed layers the peel strength is around 450 g/cm, which is above the current industry requirement for 10 µm thick Cu. Therefore, sputtering is used here for glass metallization because that it can achieve good adhesion.

*B. Process Flow*

Here, a new process approach is proposed for ultra-thin bare glass interposers, which combines lost-cost large-panel sputtering and commonly used double-sided substrate semi-additive process (SAP). As discussed in the previous section, sputtering is exploited to address adhesion challenges in this new process. Fig. 3 shows the process flow for fabricating two-metal-layer bare glass interposers by the newly-proposed process approach. It starts with bare glass with TPVs drilled by the glass supplier followed by Ti/Cu sputtering to produce the conductive seed layer. Then, dry film photoresist is laminated on both sides of the substrate and each side is patterned by UV light. After developing the photoresist, electrolytic plating is performed to increase the copper thickness in the exposed regions. Striping the photoresist and etching away the seed layer concludes the process of building two-metal-layer structures.

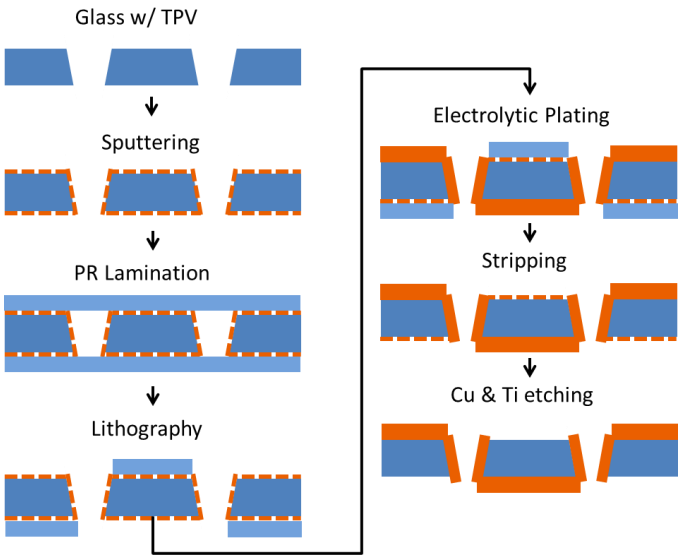


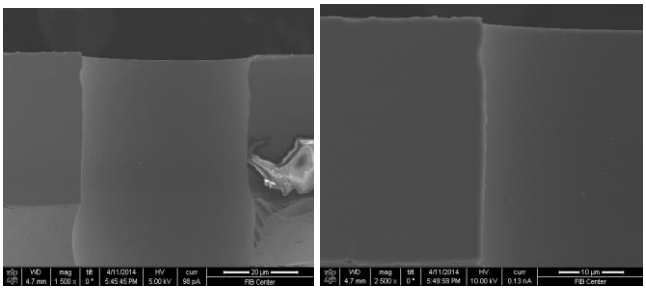

**Figure 3.** Process flow for fabricating two-metal-layer bare glass interposers by typical double-sided substrate semi-additive process.

Using this new process, two types of glass test vehicles with 30µm TPVs in 100um bare glass were designed: one with daisy chains to evaluate thermo-mechanical reliability and another one with transmission lines having via transition to test the high-frequency performance. Detailed discussion on these test vehicles will be presented in Session III and IV.

## III. Reliability

Despite potential advantages of glass interposers described in previous sections, the brittle nature of glass creates concerns related to the thermo-mechanical reliability of TPVs in glass. These concerns stem from two issues: 1) defects created on the TPV sidewalls during via formation and 2) thermomechanical stresses induced by the CTE mismatch between copper and glass.

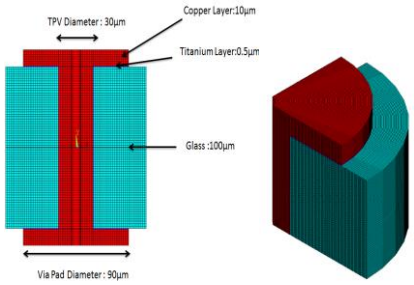
In order to address the first issue, the via formation method was evaluated by analyzing TPV sidewalls. Defects on via walls should not be big, which might cause crack formation in glass, and via sidewalls should be rough to a certain extent for adequate adhesion between the seed layer and glass. Fig. 4 shows SEM images of via sidewalls. From this picture, it is seen that sidewall is smooth and free of noticeable defects.



(a) (b)

**Figure 4.** TPV side wall observation after mechanical dicing

In order to address the second issue, a finite element model of TPVs was created and simulated in Ansys™ to assess the effect of various parameters on thermo-mechanical stresses. The TPV cross-section used in finite element simulations is shown in Fig. 5. Due to the symmetry of the structure, a quarter of TPV was modeled with axisymmetric option. Thermal cycling load between -55°C and 125°C was applied to the model. A bilinear kinematic hardening model was used for copper, whereas titanium and glass were assumed as linear elastic. Material properties are summarized in Table I. A sample simulation result is shown in Fig. 6 along with deformed TPV shape.

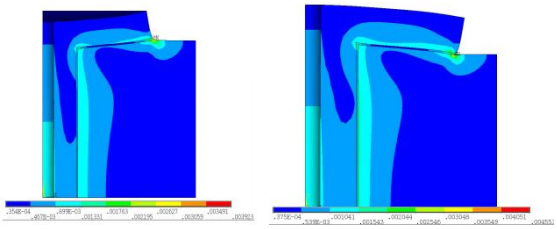



(a) (b)

**Figure 5.** TPV (a) cross-section and (b) quarter model for simulations

Table I. Material properties.

| | Elastic Modulus( GPa) | Poisson's Ratio | CTE (ppm/°C) |
|---|---|---|---|
| Glass | 63.6 | 0.23 | 3.17 |
| Ti | 116 | 0.32 | 8.6 |
| Cu | 121 | 0.3 | 17.3 |

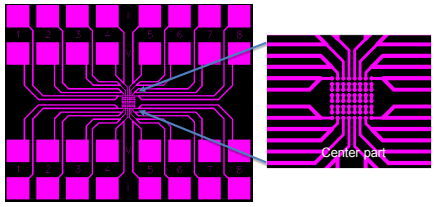


(a) (b)

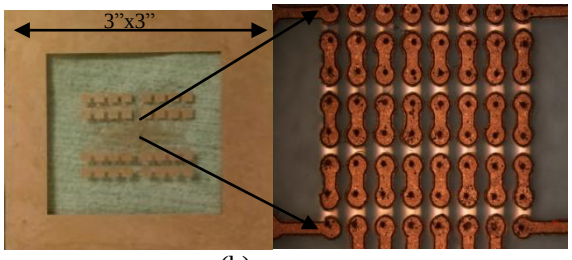
**Figure 6. (**a) TPV stresses at extreme cold and (b) hot temperatures during cycling.

Plastic strain in copper was chosen as a metric that impacts lifetime of the TPV, and tensile stress in glass was chosen as a metric that might cause cracking of glass. From simulation results it was found that plastic strain in copper increases with decreasing glass thickness when other geometric parameters are kept constant. This presents another challenge for using thinner glass. Furthermore, tensile stresses in glass increase with copper thickness, which might increase chances of crack formation. In both cases, however, accumulation of plastic deformation in copper per cycle was very low (approximately 0.005) indicating high fatigue life time and that TPVs are expected to survive 1000 thermal cycles. As a result, TPVs without major defects and with adequate adhesion of copper to glass are expected to be reliable.

In order to experimentally verify the thermo-chemical reliability of TPVs in glass, the test vehicle shown in Fig. 7 was fabricated. The test vehicle is based on 8x8 TPV arrays connected in a daisy chain pattern with contact pads for 4-point resistance measurements. TPVs had a diameter of30 µm at 100 µm pitch and the glass thickness was 100 µm. In order to achieve whole via coverage, relatively thick Ti/Cu seed layer was sputtered, leading to approximately 500 nm Ti thickness and 1 µm Cu thickness.




(a)




(b)

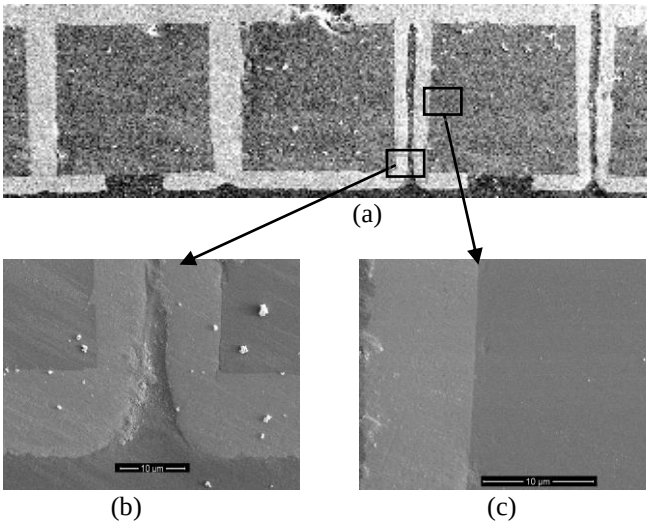
**Figure 7.** (a) Layout of test vehicle (b) Fabricated test vehicle

Test vehicles were subjected to accelerated reliability tests and the test conditions are summarized in Table II below.

Table II. Reliability test conditions.

| | |
|---|---|
| Preconditioning | • Bake 24h at 125°C<br>• 60 °C ,60% RH for 40hours (MSL-3)<br>• 3 times reflow 260 °C peak |
| Thermal Cycling | • -55 °C,125 °C 1000 thermal cycles<br>• 15 minutes dwell time at each Extreme (JEDEC JESD22-A104) |

The 4-point series resistance of daisy chains of 8 TPVs was monitored and a 10% increase from initial resistance was selected as the failure criterion. In total twenty daisy chains comprised of 160 TPVs were subjected to thermal cycling. Resistance measurements are conducted at certain intervals up to 1000 thermal cycles. All daisy chains passed 1000 thermal cycles without significant changes in resistance as expected from simulations. A passed TPV array is shown in Fig. 8. It was observed that there were no cracks in glass or failures related to brittleness of glass. Additionally, there were no major cracks observed in copper that might impact resistance measurements.



(a)

(b) (c)

**Figure 8.** (a) Cross-section of TPV array (b) TPV corner region (c) TPV sidewall after 1000 thermal cycles.

After thermal cycling there was no significant warpage of glass, which was expected from the high dimensional stability of glass. Additionally, we did not observe any failures related to TPV.

## IV. Electrical Performance

*A. TPV Loop Inductance*

The structure for retrieving the loop inductance of TPV is shown in Fig. 9, which consists of a signal via and a return via. These two vias are shorted by a metal plane that is assumed to have negligible inductance. The via diameter is 30 µm and the via pitch varies from 60 µm to 240 µm with 60 µm increment. Using Cascade GS probes, the reflection

coefficient ($S_{11}$) of the structure was be measured with a vector network analyzer (VNA).

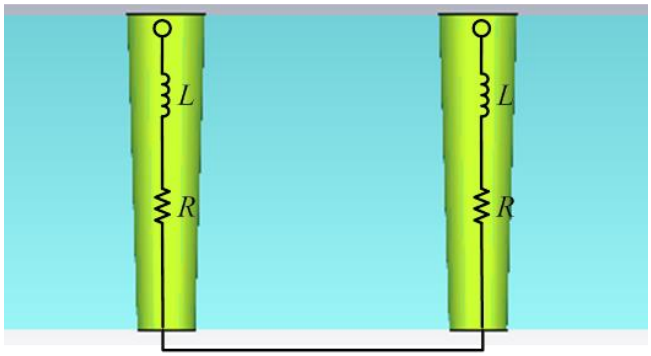



**Figure 9.** Cross section of the ground-signal via pair and its equivalent circuit.

The approximated inductance of a single via can be retrieved from the reflection coefficient $S_{11}$ by the method described in [7]. The input impedance, converted from $S_{11}$ can be expressed as $Z_{11} = 2\ (R + j2\pi fL)$, where $R$ is the via resistance and $L$ is the via inductance. The imaginary part of the input impedance is plotted against frequency in Fig. 10, and the via inductance retrieved is plotted against frequency in Fig. 11. The slope of curves in Fig. 10 is the inductance. From both figures, it can be observed that as the pitch increases from 60 µm up to 240 µm, the loop inductance ramps from 30 pH to 62 pH. This is because larger pitch results in larger loop area which captures more magnetic flux. Therefore, bringing the return via closer is always preferred to reduce the loop inductance.

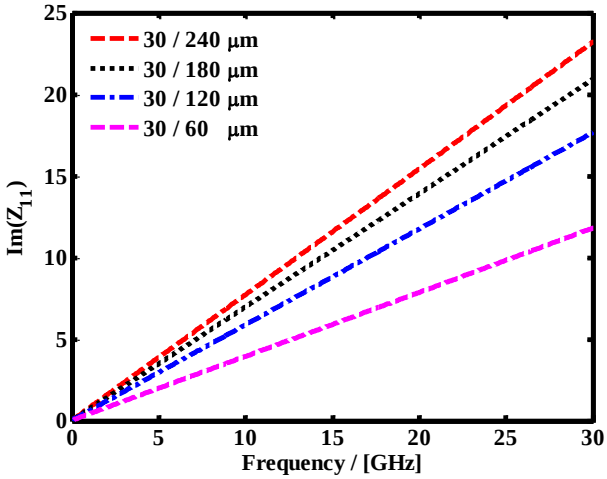



**Figure 10.** Imaginary part of the input impedance against frequency by 3D EM solver.

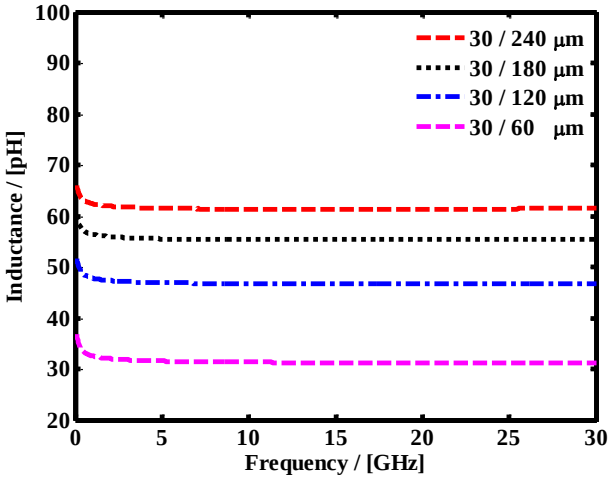



**Figure 11.** Retrieved inductance of a single via against frequency by 3D EM solver.

*B. Single-Ended Coplanar Waveguide Channel*

Due to the low loss of the glass substrate, the single-ended channel has high bandwidth and renders very high-speed data rates. A typical ground-signal-ground (GSG) coplanar waveguide (CPW), shown in Fig. 12, was designed and simulated by a 3D EM solver. Here, three CPW channels with different lengths, namely 0.6 mm, 0.8 mm and 1.2 mm, were studied. The line width was set to be 25 µm and the line space was 175 µm, while the TPV diameter was 30 µm and the pitch was set to be 200 µm.

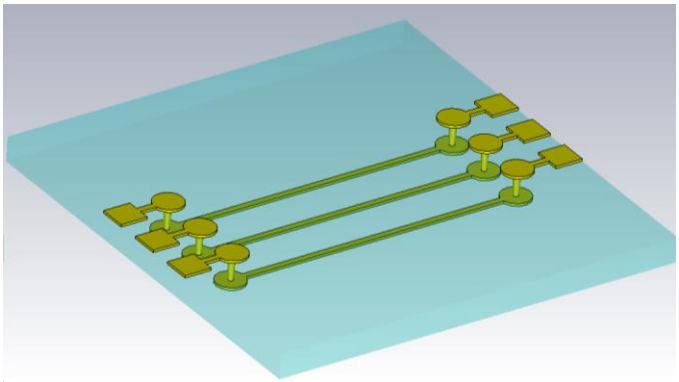


**Figure 12.** Prospective view of the designed Ground-Signal-Ground coplanar waveguide (CPW) channel.

Frequency-domain simulation was performed using the 3D EM solver – CST that numerically computes the structure with finite element method. The insertion loss $|S_{21}|$ is presented in Fig. 13, where we can conclude that the 3-dB bandwidth for 0.8 mm and 1.2 mm is 24 GHz and 16.7 GHz,

respectively, and the one for 0.6 mm is beyond 30 GHz. The bandwidth can be extended if the impedance of the line is matched to 50 Ω. Based on the simulated results, it can be found that the loss is still dominated by the conductor losses instead of the dielectric loss from glass due to the low loss of glass.

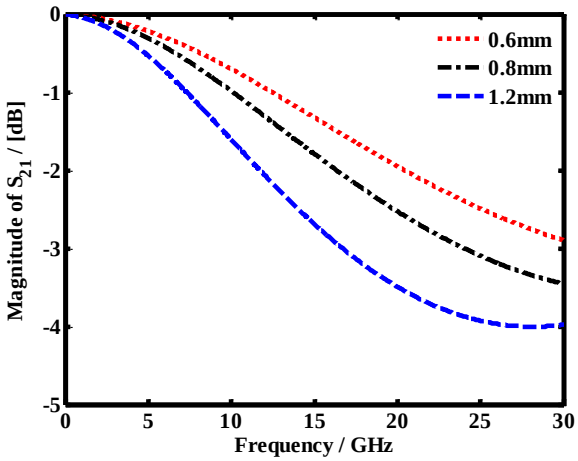



**Figure 13.** Simulated $|S_{21}|$ for single-ended CPW channel with various lengths.

Time-domain eye diagram simulation indicates that even 1.2 mm channel is capable of transmitting data at 20 Gbps, as shown in Fig. 14. The pseudo-random bit sequence (PRBS) has a rising and falling time of 20 ps and amplitude of 1 V. A quantitative study showed that the eye height is about 0.76 V and eye width is around 47 ps. The peak-to-peak time jitter is about 3.33 ps. Overall, the clearly open eye diagram shows the superior performance of the glass channel.

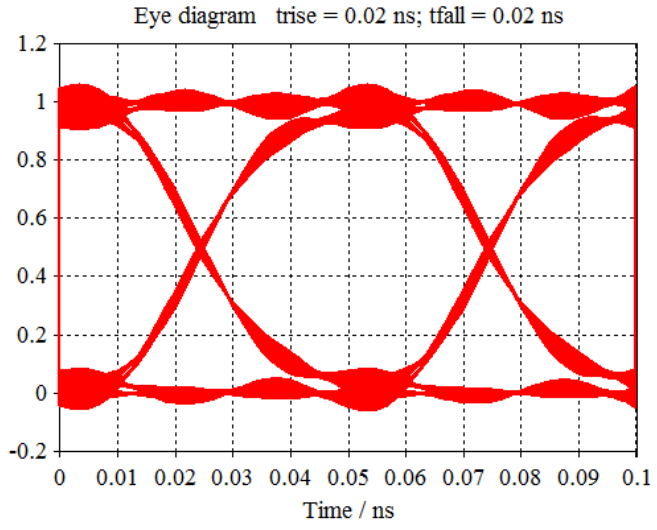



**Figure 14.** Simulated eye diagram for 20 Gbps pseudo-random bit sequence (PRBS) in the case of 1.2 mm single-ended CPW channel.

## V. Conclusion

A new double sided integration process for the metallization of TPVs in thin and bare glass panels based on sputtered seed layers was demonstrated for glass interposers targeted at two major applications, namely, high bandwidth logic-memory interposers, and 4G/LTE and 5G RF modules. Vias with diameter of 30 µm and pitch of 60 µm were successfully formed and metallized in 130 µm thin glass panels. The via chains in fabricated test vehicles passed 1000 thermal cycles from -55C to 125C, and electrical simulations indicate low inductance and loss up to 30 GHz, establishing the superior thermo-mechanical reliability and the excellent electrical performance of bare glass interposers directly metallized by sputtered seed layers and semi-additive copper electroplating.

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