Si Vapor Chamber Integrated with Through Silicon Via for 3D Packaging

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Abstract

We demonstrate an etched silicon vapor chamber integrated with a through-silicon via (TSV) for 3D packaging. The Si vapor chamber chip enables low mismatch in the thermal expansion coefficient of a Si-LSI chip and provides a new heat dissipation path for 3D-LSI inter layer cooling. For the first prototype of the vapor chamber, an outside 33-mm × 33-mm chip consisting of a 25-mm × 25-mm area for the vapor chamber, a wick structure 30-μm high, and a vapor passage 100-μm high is developed. In-situ observation of the behavior of the working fluid through the cover glass and heat transfer enhancement is successfully demonstrated. The improvement rate of thermal resistance is 7.1% compared to a test chip without working fluid. Next, the fluid flow of a second vapor chamber prototype consisting of the first prototype integrated with a TSV structure using a Si pillar of 150-μm diameter is investigated. Thermal resistance and droplet observation conducted to evaluate the influence of the TSV. The operation of the vapor chamber is confirmed when a Si pillar is arranged to a coarse pitch of more than 500 μm. A droplet is generated and the vapor passage is partially obstructed. However, the droplet eventually degenerated and the performance of the vapor chamber is maintained. When the Si pillar is arranged to a fine pitch of 200 μm, the entire vapor passage is blocked during the liquid charging process, and no improvement is observed in the thermal resistance of the chip.

Key words

Electronics cooling, Silicon vapor chamber, 3D-Package, TSV

1. Introduction

Three-dimensional (3D) packaging technologies are receiving more attention for system performance enhancements, due to their higher interconnect densities and shorter interconnect lengths. Thermal management is important for high performance and reliability in the design and development of modern 3D packaging technologies. When a 3D stacked chip becomes thinner, the influence of a localized hot spot in the logic layer becomes larger. The hot spot causes chip destruction because of an increase of leakage current by temperature rise.

To suppress the hot spot in 3D packaging, use of an interlayer micro-channel cooling embedded 3D stacked chip has been previously studied due to its high cooling performance at very high power densities [1]-[3]. However, implementation of stable liquid flow in the micro channel is difficult in terms of the need for an external power source and a pump device in the physical configuration of a high-end server. As a candidate that realizes thermal

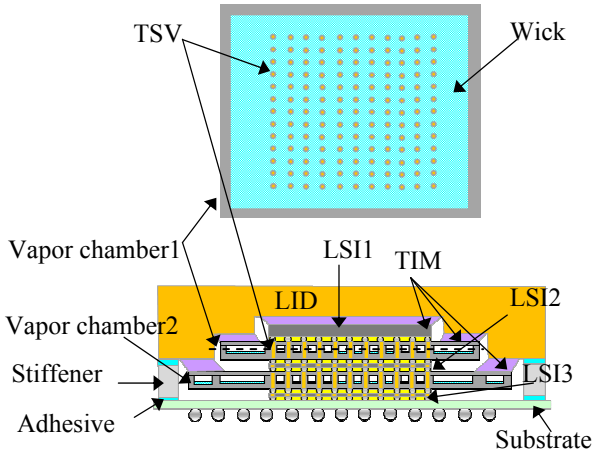


Fig. 1 Structure of a 3D package embedded vapor chamber chip (upper) cross section view of vapor chamber1, (lower) cross section of the package

management in a limited physical configuration, we have developed a Si vapor chamber that performs as a new heat dissipation path for 3D-LSI interlayer cooling, shown in Fig. 1.

Vapor chamber chips that are fabricated by a Si machining process are larger in overall size than a vertically stacked chip on substrate. In the packaging assembly, a stacked chip structure is attached to a lid structure, typically solid copper or Al-SiC via thermal interface material (TIM) and structurally supported by stiffener and adhesive. In constant, not only the top of the stacked chip but also the outer periphery of the vapor chamber chip is attached to the lid structure via TIM. Most of the vapor caused by a hot spot is moved to condensation area at outer periphery of the vapor chamber chip.

The development of only the Si vapor chamber has been investigated, and a high performance was reported [4]. However, to achieve our concept, the vapor chamber must be thinner to reduce the wiring length. In addition, TSVs connect upper and lower chips. Research on the influence of obstacles (e.g. TSV) related to fluid internal flow is scarce.

This paper presents, for the first time, a thin Si vapor chamber composed of a channel about 100-µm high, and investigation regarding flow obstacles. In this paper, the fabrication process, testing of the prototype, and spacing of TSVs are discussed.

Fabrication Process

The process flow including cross sectional schematics is shown in Fig. 2. The fabrication of the vapor chamber chip is performed using a Si micromachining process with deep reactive ion etching (DRIE), and surface activated bonding.

The first wafer process begins following the completion of the semiconductor back end of line (BEOL) process with a 200-µm-thick Si wafer. After 10-µm photoresist is patterned, a 100-µm-deep vapor channel excluding the TSV area is etched by DRIE on the back side.

The second wafer process starts with a 200-µm-thick Si wafer. After 10-µm photoresist is patterned, a 30-µm-deep wick structure is etched. Oxygen plasma cleaning and sulfuric acid and hydrogen peroxide mixture cleaning are performed to remove the photoresist.

The silicon wafers with engraved micro structures are bonded to each other using a low temperature bonding technique. Both wafers are irradiated with Argon fast atom beam sources in a high vacuum bonding chamber (less than 10^{-6} Pa) at room temperature. The load applied when both wafers are bonded is 500 kgf. Hermetical sealing is then performed. TSV fabrication is accomplished with DRIE of the TSV holes. Cu is used to fill vias in the TSV holes after oxide is deposited. The surfaces of the TSV and wiring layers are planarized using chemical-mechanical polishing (CMP). After back grinding, copper pillar is formed by recess etching on the back side. After etching the oxide, benzocyclobutene (BCB) polymer is applied in several batches. On the final application, the vapor chamber is evacuated and charged with the working fluid, thus completing the Si vapor chamber. The 3D-LSI stack that forms the thermal diffusivity layer is soldered to wiring layer after chip to chip bonding using solder bumps.

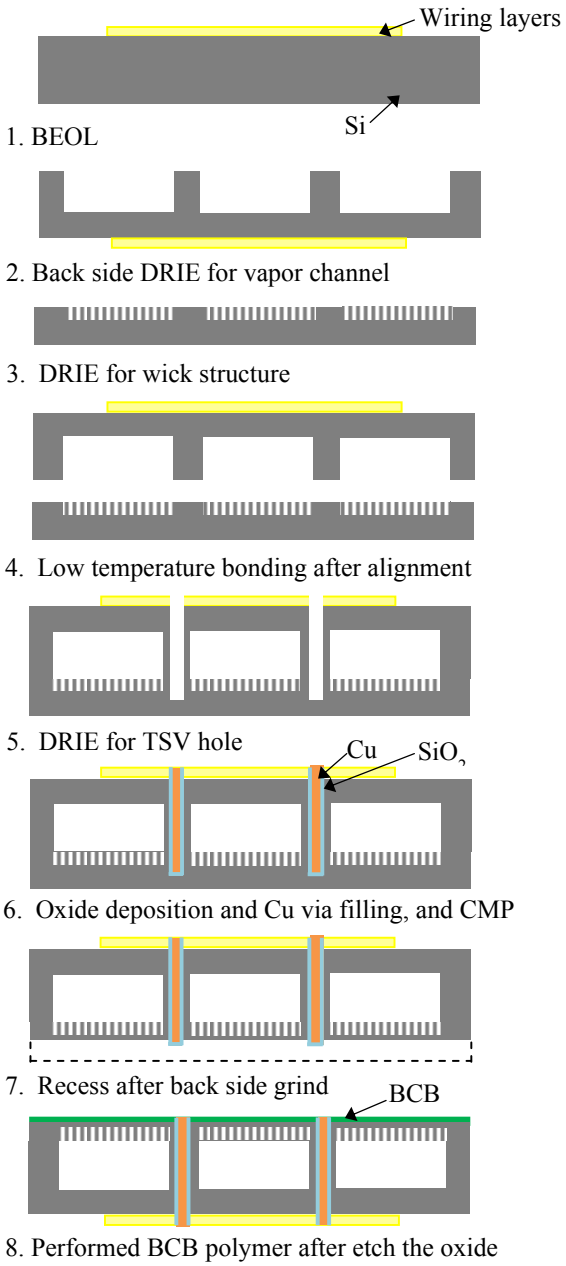


Fig. 2 Fabrication process

Figs. 3 to 5 show SEM photographs of the wick and TSV structures for the Si vapor chamber with different views.

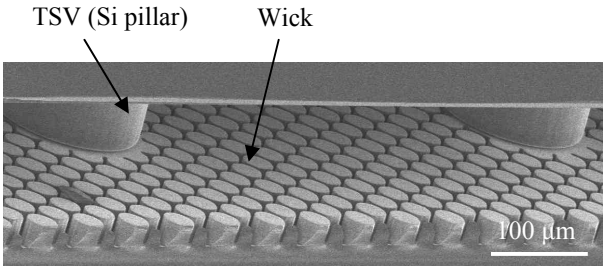


Fig. 3 SEM Si vapor chamber TSV chip (bird's eye view)

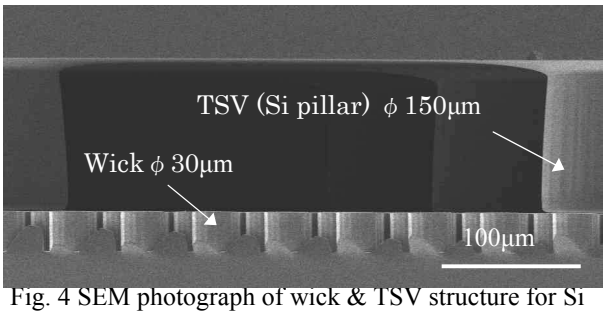


Fig. 4 SEM photograph of wick & TSV structure for Si vapor chamber (cross section)

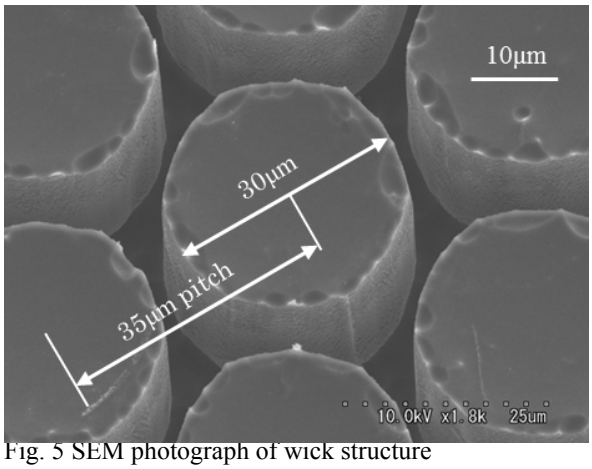


Fig. 5 SEM photograph of wick structure

3. Experimental Setup

The experimental setup is shown in Fig. 6. The outer part was cooled with an air-cooled heat sink as well as our concept for cooling interlayer of 3D-LSI module (Fig. 1). The sample is fixed with the heat sink that opens for observation through the glass. The installation load is 3kgf. The heated area is 5mm × 5mm. The heater block used to simulate a hot spot, is electrically heated at its base with a ceramic heater, and is connected by a layer of thermal paste under the center of the vapor chamber area (Cosmo thermal grease SF401, thermal conductivity 4.5W/m K). The heat sink and the sample top plate are cooled with a fan blowing air in the direction shown. Temperature is measured by five thermocouples (K-type 100-µm wire probe). To measure the heat flux of the heater block, three points are set up. And to measure thermal resistance as the evaluation value of thermal diffusivity, two points are set up at the edges of vapor chamber area bottom. Thermal resistance is determined by the following expression.

$$R = \frac{T_{center} - T_{bottom}}{Q} \quad (1)$$

Two types of vapor chamber chips are evaluated. One has no obstacles in the vapor chamber, and the other has a Si pillar covered by an outer TSV. The no-obstacle sample is referred to as the no-TSV sample. Both samples consist of a wick structure 30-µm high and a vapor channel 100-µm high. The top of the sample is covered by TEMPAX Float glass with a fluid charging hole. Ethanol is used as the working fluid. The amount of fluid is regulated by observations through the glass after the samples are evacuated using a vacuum pump.

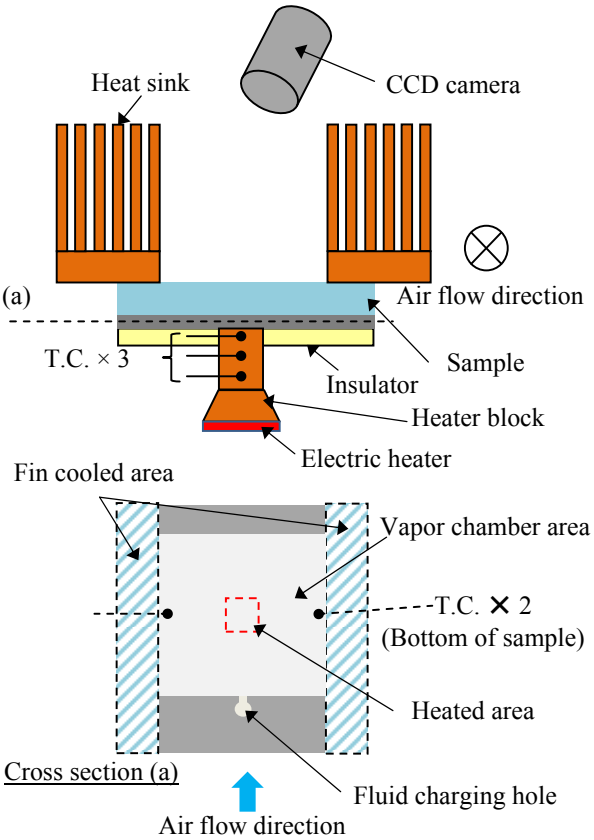
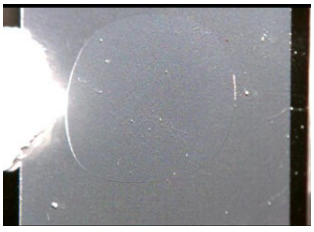


Fig. 6 Schematic of the experimental setup

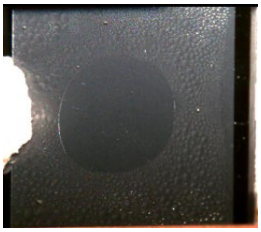
4. Results & Discussion

4-1. No-TSV sample (first prototype)

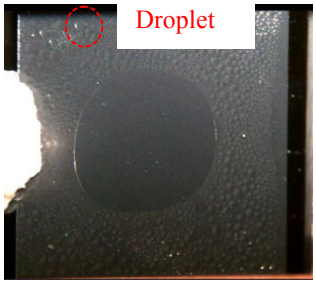
Experimental results of regarding droplet and vapor movement in the no-TSV sample are shown in Fig. 7. In the initial state, the size of the working fluid droplet is about 15mm in radius when attached to the glass side (a). The first appearance of liquid is shown in Fig. 8. The liquid is attached to the glass and wick respectively. The liquid at the center becomes smaller until the inside of the vapor chamber reaches a saturated condition (b). The liquid droplet that attached to the glass side expands during the 400s after the heater power is turned on. The liquid drop that was originally placed on the glass returns to a liquid at the center when it comes into contact with the wicks (c), and (d). The temperature saturated after ~850s. A surrounding liquid drop group repeated similar behavior. The comparison of the thermal resistance obtained from the temperature measurement results is shown in Table 1. Thermal resistance decreased by 7.1% compared with the sample without working fluid. It is thought that a wick attracts the working fluid, and heat is carried by the moving working fluid.



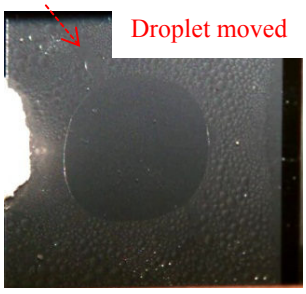
(a) Initial state (0s.)



(b) Center of liquid saturated (400s.)



(c) Steady state1 (874s.)



(d) Steady state2 (875s.)

Fig. 7 Liquid behavior in the no-TSV sample

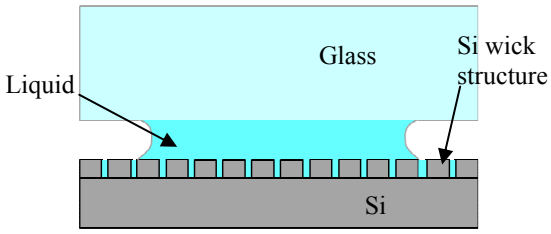


Fig. 8 Appearance of liquid at the center

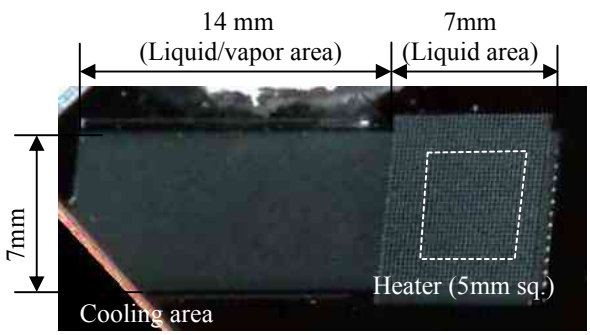
Table 1 Difference of thermal resistance between the no-TSV sample w/ and w/o working fluid

Measurement method	Thermal resistance [K/W]	Improvement rate
With working fluid	4.79	7.1%
Without working fluid	5.16	-

4-2. TSV sample (second prototype)

Experimental results of the TSV sample are shown in Fig.9. In the initial state, the liquid has come into contact with the liquid trap area of the Si pillar with pitch of 200 µm on the glass side (Fig. 9 (a)). After ~400s heater power is turned on, the appearance of the condensed droplet is confirmed (Fig. 9 (b)). Si pillars were not placed in the middle, so the droplet has a reduced velocity, and degenerates before long in front of the liquid trap area (Fig. 9 (c)). In constant, the droplet is trapped by the Si pillar and degenerates as it moves to the middle when using a 1700-µm pitch (Fig. 10 (b)). There is little movement when using a 200-µm pitch, though the droplet is confirmed (Fig. 10 (a)). The comparison of each thermal resistance is shown in Table 2. The different rate that is average of thermal resistance at the 500-µm to 7000-µm pitch was 7.7% compared with 200um pitch (Fig. 11)

Because the droplet in the 1700-µm pitch does not return to the vicinity of the heat source, the droplet is not related to the heat transfer improvement. However, it indicates the wick operation, and the wick operation is more wide-ranging than at the 200-µm pitch. We could not confirm enough parameters to properly investigate about the influence of the Si pillar pitch on heat and mass transfer. However, it is clear that the pitch must be set up to prevent the Si pillar from acting as a plug because of the meniscus action of the droplet and the liquid level. Moreover, it is indispensable that the vapor passage has enough width to allow full passage of vapor in order to obtain the heat transfer performance.



(a) Initial state (0 s.)

(b) Steady state 1 (400 s.)

(c) Steady state 2 (407 s.)

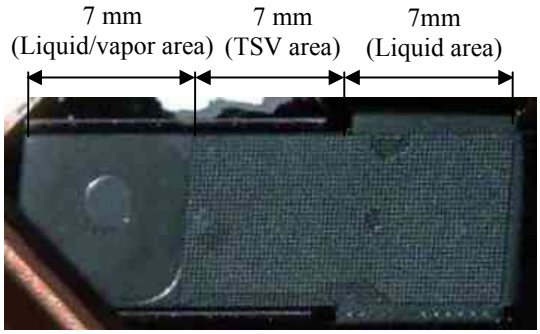
Fig. 9 Liquid behavior in the no-TSV samples

5. Conclusion

In this research, the application of a Si vapor chamber to a 3D-LSI cooling structure was demonstrated for the first time. A 100-µm channel structure was fabricated in the prototype Si vapor chamber chip for trial purposes. The vapor chamber chip is inserted between the stacked LSI chips, and provides a new heat dissipation path that transports heat away from an internal hot spot through liquid/vapor transport. It is a device that has assisted in previous cooling structures.

The visual properties and the thermal performance of the internal fluid of the vapor chamber chip were confirmed, using a glass top plate structure, and it is confirmed that there is an average performance difference of 7.7% in the thin 100-µm vapor passage when using a TSV pitch of 500 to 7000 µm compared with 200um pitch.

It is necessary to prevent the liquid from plugging the vapor passage when TSV pillars are present.



(a) Steady state (pitch 200µm)

(b) Steady state (pitch 1700µm)

Fig. 10 Liquid behaviors in TSV (Si pillar) samples

Table 2 The different rate of thermal resistance (all cases have working fluid)

TSV pitch [µm]	Average Thermal resistance [K/W]	Difference in thermal resistance [%]
200	8.89	-
500	8.22	7.6%
1700	8.27	7.1%
7000 (no-TSV)	8.15	8.4%

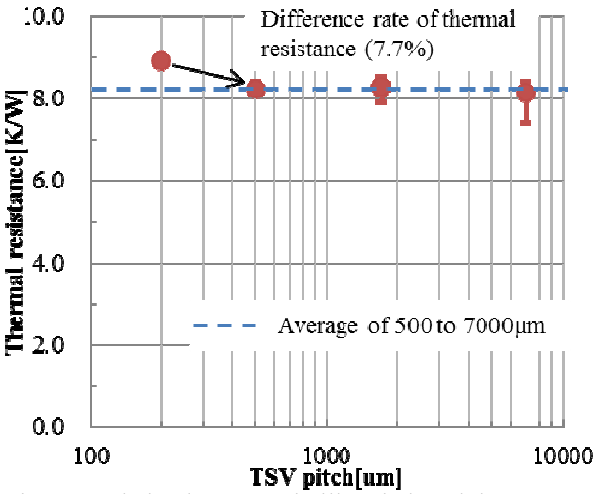


Fig. 11 Relation between Si pillar pitch and the average thermal resistance (all cases have working fluid)

6. REFERENCES

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