Study Photo Imagable dielectric (PID) and non-PID on process, fabrication and reliability by using panel glass substrate for next generation interconnection

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Abstract

In 1965, Gordon E. Moore, the co-founder of Intel stated that numbers of transistors on a chip will double every 18 months and his theory called the Moore's Law. The law had been the guiding principle of chip design over 50 years. The technology dimension is scaling very aggressively in IC foundry. For example, TSMC announced their 5nm Fin Field-Effect Transistor (FinFET) process technology is optimized for both mobile and high performance computing applications. It is scheduled to start risk production in the second half of 2019.[1] To overview the semiconductor supply chain included IC foundry, wafer bumping, IC carrier, PCB (Printed circuit board) and OSAT (oversea assembly and testing)…etc., the IC carrier and PCB technology dimension scaling are far behind than the IC foundry since many reasons for the traditional industry. The industry needs different kinds of breakthrough approaches for the scaling of via and strip line in next generation interconnection. Traditional organic substrates faces many challenges of warpage, surface roughness and material dimension stability issues for manufacturing and high density I/Os with very fine line interconnections. To breakthrough these challenges, the materials of glass carrier, new photo-imagable dielectric (PID) and advanced equipment were evaluated for the fine line and fine via interconnection. In the papers, there are many PID and non-PID materials were surveyed and compared for fine via (< 10μm) interconnection or low loss of high frequency application. The first candidate was chosen for redistribution layers (RDL) fabrication by using 370mm x 470mm glass panels. Semi additive process (SAP) was used for direct metallization on glass panel with different build-up dielectric materials to form daisy chain test vehicles. The process, fabrication integration and electrical measurement results of daisy chain showed good continuity and electric resistance in the glass panel substrate. The reliability of the thermal cycling test (TCT) and highly accelerated stress test (HAST) were evaluated as well in this study.

Key words

Photo Imagable dielectric (PID), Glass substrate, Reliability, High density interconnection, IC carrier, and redistribution layers (RDL)

I. Introduction

Traditional semiconductor components include active chips, passive device, silicon interposer, organic substrate, and printed circuit board. How to package these components as a module is based on the product requirements. In recent decades, lots of assembly technologies and structure solutions for different packaging have been evaluated, such as flip-chip assembly, Fan-out/Fan-in, InFo (Integrated Fan-out), CoWoS (Chip on Wafer on Substrate), SWIFT (Silicon Wafer Integrated Fan-out Technology), SLIM (Silicon-Less Integrated Module), EMIB (embedded multi-die interconnect bridge), 2.1D/2.3D/2.5D/3D IC packaging and so on. All of these package technology solutions were considered to the electrical routing interconnection. The scaling of strip line and via is always the trend for the semiconductor industry supply chain.

To achieve the dimension scaling in IC substrate and PCB industry, glass as the removable carrier [4] or substrate core [2, 3, 5] played a very important role for the next generation interconnection. Benefits to apply glass as the carrier or substrate core such as low profile surface suitable for high density application and good size effect for large form factor compared with Si wafer had attracted many researchers' attentions to develop. Besides, good dimension stability of glass also shows lower warpage in the process and high control level in fine line/space and via formation through

traditional IC carrier and PCB process. However, there are still many challenges need to be conquered in glass carrier or glass core, such as very careful handling of single/double side metallization process due to its brittleness and interfacial adhesion improvement among glass, metal and other materials like dielectrics.

Since the single side semiconductor process with liquid photo resist and liquid dielectric material by using silicon or glass material are very common in foundry and display industry. The fine strip line and fine via are mutual and achieved easily by using liquid spin and slit coating process. However, for the double side IC carrier and PCB process with organic substrate, there are still rare to have a suitable dry film photo resist or dielectric materials for dimension miniaturization.

In this paper, 370mmx470mm glass panel was selected to integrate the fine strip line and via interconnection. The dry film PID (photo-imagable dielectric) and non-PID dielectric materials are surveyed and evaluated with single side glass carrier or double-side glass core by adapting SAP (semi additive process) to form redistribution layers (RDLs). Daisy chain test vehicles were also fabricated for reliability including thermal cycling test (TCT) and highly accelerated stress test (HAST) test.

II. Dielectric selection

A. Photo-imagable dielectric (PID)

PID material had many benefits by using image transfer procedure to form finer interconnection via and better throughput compared with laser technology. Spin or slit coating process are well known processes to form thin PID material on single side silicon wafer in IC foundry. However, for applying the dielectric material on double side structure, dry film type PID shows higher feasibility in double side process in IC carrier or PCB factory compared with liquid type PID. In addition to process flexibility, PID intrinsic properties are also important. Firstly, aqueous developer system such as TMAH (Tetramethylammonium Hydroxide) has better handling than organic solvent such as PGMEA in IC carrier or PCB factory. Secondly, higher curing temperature and glass transition temperature (Tg) means higher thermal stability. Thirdly, lower coefficient of thermal expansion (CTE) results in better warpage control in process. Based on the above considerations, PID-A in Table 1 was chosen as the target material.

Chemical resistance is very important for PID before process evaluation because many kinds of light sensitive chemical agents are added into PID material to form via patterns easily through exposure and development process. Electric-less Nickel electric-less Palladium immersion Gold (ENEPIG) is one of typical surface finish wet process with many chemical process and high temperature reacting sink in IC carrier and PCB plant. If the compositions in PID are more sensitive and easier attacked by the wet chemicals, it will be hard to integrate the PID interconnection. After preliminary test, PID-A showed enough chemical resistance against ENEPIG process.

Table 1. Film type PID material candidates

Property	A	B	C	D
Developer	TMAH	TMAH	PGMEA	PGMEA
Curing Temp (C)	220	200	200	200
Tg(C)	>250	220	200	230
Moisture (%)	0.74	0.1	1.5	<1%
Df	0.0176 (40GHz)	0.013 (30GHz)	N/A	0.015 (1GHz)
CTE (ppm/K)	54	120	45	46

Adhesion strength is another important factor for PID integration. Cross-cut testing is a common method to evaluate the compatibility between PID and glass. Five classifications are illustrated in ASTM D3359 standard as shown in Fig. 1. Usually, level 5 result indicates good adhesion for PID on glass.

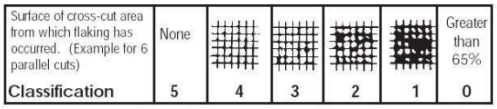


Fig. 1 cross-cut Classification (ASTM D3359)

Fig. 2 showed the cross-cut test of PID on Cu. No PID was removed by 3M adhesive tape and showed cross-cut result in level 5, which indicated that the PID-A has enough adhesion property to Cu layer on glass or organic substrate.

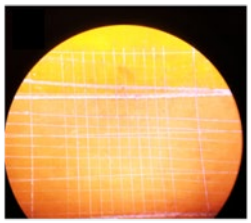


Fig. 2 The OM image of cross-cut test on PID/Cu.

B. Non-photo-imagable dielectric (non-PID)

In current IC carrier and PCB factory, non-PID is used widely and its high filler content resulted in lower CTE and higher Young's module than other polymers, such as polyimide. For high density application, electrical properties and the adhesion to glass substrate are considered as selected criteria. Table 2 shows three candidates of non-PID and material B was chosen due to its lower signal loss properties and better adhesion performance to glass substrate by

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following ASTM D3359 standard as shown in Fig 3.

Table 2. Non-PID material candidates

Property		A	B	C
Type		film	film	film
Curing Temp(C)		190	200	190
Tg (C)		176	165	180
Dk	@5.8GHz	3.3	3.3	3.3
Df	@5.8GHz	0.0074	0.0036	0.0037
CTE (ppm/K)		20	20	27

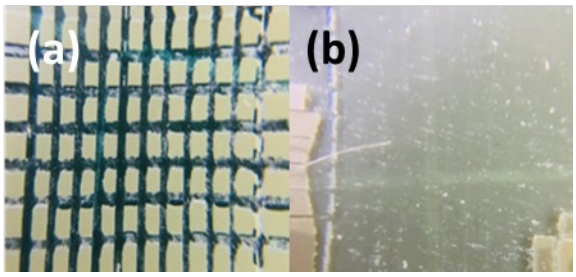


Fig. 3 The initial verification of cross-cut results (a) material B is in level 5 before reliability (b) material C is failed in level 0 before reliability.

III. RDL process integration

A. Integration structure and interface evaluation

The dry film photo resist and dielectric materials can be applied with the RDL (Re-distribution Layers) substrate and the TGV (through glass via) substrate. Fig. 4 shows the RDL process integration structure in this study. In this structure, four interfaces, such as (1) the dielectric material to glass surface; (2) the dielectric material to the inner metal trace; (3) the second metal trace on the dielectric material; and (4) the dielectric material to itself or to the top solder resist layer were considered. Table 3 showed the evaluation summary of each interface:

- At PID/glass interface, PID-A passed cross cut test on glass substrate and TCT 1000 cycles.
- At PID/metal interface, no blister and delamination be observed between the interface and it passed TCT 1000 cycles.
- At metal/PID interface, the peeling strength is larger than 0.35kgf/cm.
- At PID/PID interface, no blister and delamination issue occurred in PID after TCT 1000x.It indicates this PID has good potential for multiple RDL structure.

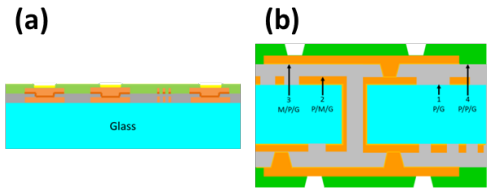


Fig. 4 The structure scheme of glass substrate. 4(a)RDL (Re-distribution Layers) on glass carrier; 4(b) RDL on TGV (through glass via) substrate.

Table 3. PID reliability test result summary

No	Interface	Pass items
1	P/G	-Cross-cut 5B -TCT 1000x pass
2	P/M/G	-Cross-cut 5B -TCT 1000x pass
3	M/P/G	-Cross-cut 5B -Peeling strength> 0.35kgf/cm
4	P/P/G	-Cross-cut 5B -TCT 1000x pass

Cu peeling strength (P/S) was also measured by following ASTM D903 standard with 25μm Cu layer as shown in Fig. 5. Higher peeling strength indicates higher adhesion between Cu and PID. Fig. 6 showed the peeling strength of 10μm and 6μm thickness PID which are 0.54 and 0.41kgf/cm, respectively.

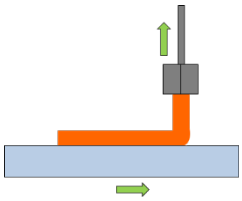


Fig. 5 Schematic diagram peeling strength test

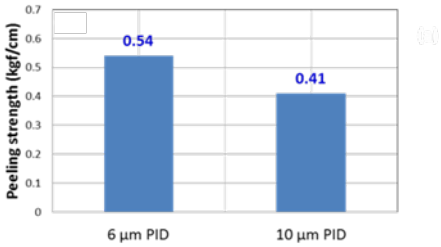


Fig. 6 The Cu peeling strength results on 6μm and 10μm thickness PID.

On the other hand, non-PID after laser drill process would have some residual so-called smear at the bottom of via in general and a process is necessary to remove the smear from via bottom, such as traditional wet desmear process or dry plasma treatment. These processes could also roughen the surface of non-PID and influence the interface condition

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between upper Cu layer and non-PID. In this study, dry plasma process was used for via desmear because traditional wet desmear process always results in larger roughness of non-PID and less compatibility to high trace density application. Fig. 7 SEM image showed initial non-PID surface reveals smooth morphology before plasma treatment. All fillers were also under the resin of non-PID.

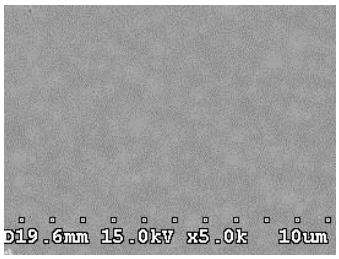


Fig. 7 SEM image of non-PID before plasma

Table 4 showed the SEM images of non-PID surface after plasma treatment with several parameters. The filler particles were gradually appeared because the resin of non-PID has been removed during plasma process. The particles came out along with the plasma treatment power and time. As expected, the surface roughness was also increased as the plasma power increased. Under high plasma power and 5 min plasma treatment time, the roughness of non-PID is 0.34µm.

Table 4. The SEM image of non-PID roughness correspond to plasma condition

Power / Time	Low	Medium	High
1min	Ra:0.15µm	Ra:0.22µm	Ra:0.24µm
3min	Ra:0.24µm	Ra:0.26µm	Ra:0.30µm
5min	Ra:0.25µm	Ra:0.32µm	Ra:0.34µm

Cu peeling strength (P/S) was also measured by following ASTM D903 standard as shown in Fig. 6. Higher peeling strength indicates higher adhesion between Cu and non-PID. Fig. 8 showed the Cu P/S corresponding to the plasma treatment conditions. All plasma conditions performed P/S larger than the target value 0.5kgf/cm. The highest P/S was produced by the highest power with the longest process time.

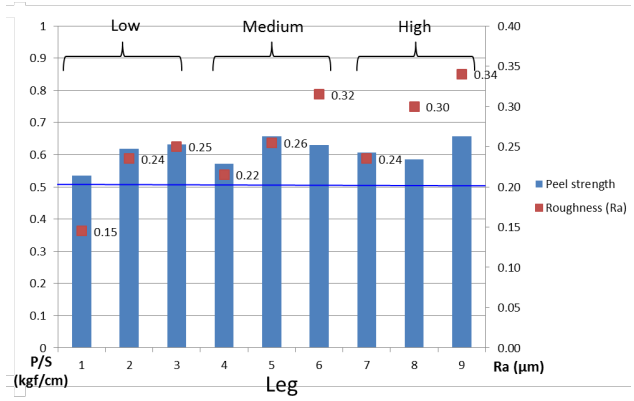


Fig. 8 The plasma condition correspond to peel strength

The compatibility of laser drill and plasma process was evaluated by the quick via pull (QVP) test and the schematic diagram was showed in the Fig. 9. If non-PID scum remained in the bottom of via, upper Cu plating layer will be separated from the lower Cu layer without any mechanical damage, as shown in Fig. 10 (a1) and (a2). The QVP results revealed that the smear of non-PID could be removed by plasma and the lower Cu layer of all samples were pulled out from the bottom of via, as shown in Fig. 10 (b1) and (b2).

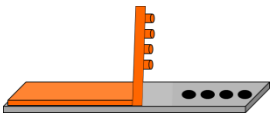


Fig. 9 The schematic diagram of the QVP test.

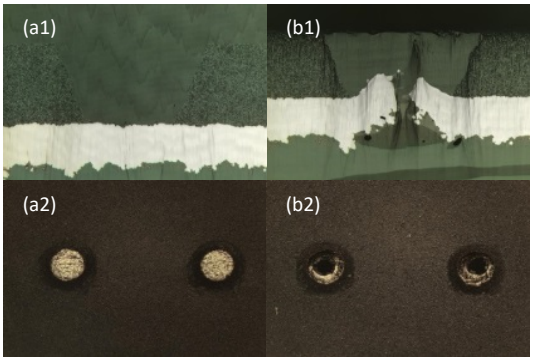


Fig. 10 (a1, a2) Cress-section and top view of NG sample after QVP test (b1, b2) Cress-section and top view of OK sample after QVP test

B. Fine Line formation

In order to meet the demand for increasing process capability in recent years, the wiring in IC chips become more and more miniature. It is necessary to significantly reduce the width of conventional circuits. The use of liquid type photoresist to pattern fine circuits has become mainstream [4]. The liquid type photoresist can be leveraged the experience from display industry. Fig. 11 shows the top view of 2/2µm, 3/3µm and 5/5µm fine Cu trace by liquid

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type photoresist. However, liquid type photoresist have several issues in whole process. For example, liquid type photoresists usually require expensive organic materials as developer and stripper but these chemicals have never actually been used in conventional BGA (Ball grid array packing) manufacturers and liquid type photoresist has poor compatibility to glass substrate with TGV due to its fluidity property.

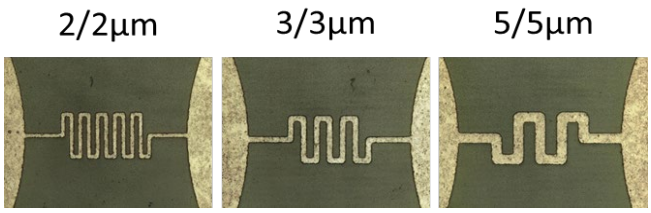


Fig. 11 top view images of Cu trace with line/space 2/2µm, 3/3µm and 5/5µm.

Fig. 12(a) showed SEM top view of fine Cu trace by dry film type photoresist on glass substrate. Tilted SEM in Fig. 12(b) also reveals good sidewall topography of fine Cu trace, which has potential in high speed or high frequency application. From Fig. 12(c), the Cu width and thickness was estimated to 3.23 µm and 3.85 µm respectively. Finally, L/S=4 µm/6 µm of Cu trace was obtained and we believe it is available for future IC carrier and BGA application.

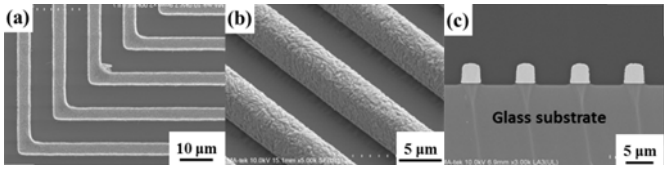


Fig. 12 SEM images of Cu trace on glass substrate, including (a) top view, (b) tilt 45°, (c) cross-section.

C. Fine via formation

To compare with non-PID materials, dry film type PID has the advantage of fine via lithography property instead of laser process. Due to the requirements of fine via formation, film type PID could be provided the possible way to approach the fine via < 10µm on glass and organic substrates.

In 6µm thickness of PID-A, process window check results of exposure and develop process were shown in Fig. 13(a) and (b). Expected 5µm via could be formed under 160mJ/cm^2 exposure dose and 30 sec developing time. Fig. 13(c) showed the 45°-tilted SEM image of 5µm via. The vertical side wall could be seen with barrier/seed layer on PID-A in Fig. 13(d). Besides, no PID residual was observed in the bottom of 5µm via. All 5µm via were fulfilled by plating Cu as shown in Fig. 13(e), which reveals that good process feasibility of metallization process for these fine via with nearly vertical side wall.

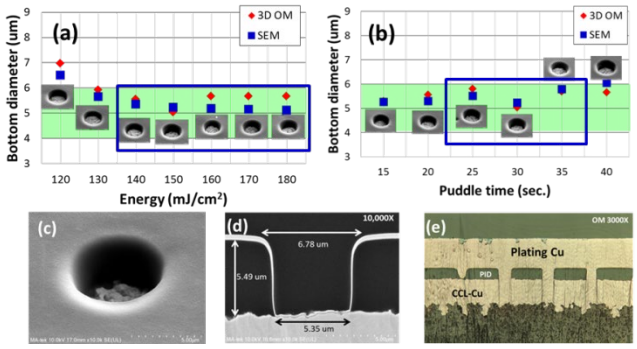


Fig. 13 (a) and (b) are the process window of 5µm via. (c) Tilted SEM image of 5µm via. (d) The cross-sectional SEM of 5µm via. (e) The cross-section image of 5µm via after Cu plating.

In 10µm thickness of PID-A also evaluated and the cross-section photo was shown in Fig. 14 (a). Nearly verticle side wall and clear via bottom without PID scum were observed as 10µm PID-A. The cross-sectional OM of 10µm via after Cu plating as shown in Fig. 14 (b). Cu was fulfilled into via and no void was seen which indicated the seed layer is continuous along the surface of 10µm PID. It is worth to mention that film type PID could be laminated easily by vacuum laminator and keep good thickness uniformity even on organic substrate with obvious warpage issue. This indicated film type PID is a potential candidate for fine via formation on glass and organic substrate.

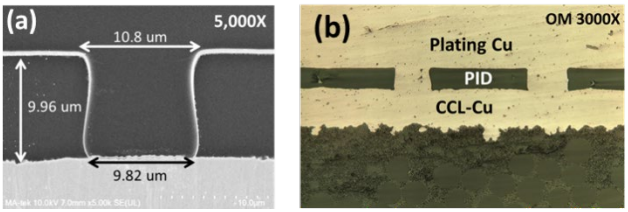


Fig. 14 (a) The cross-sectional SEM of 10µm via. (b) The cross-sectional OM image of 10µm via after Cu plating.

IV. Test Vehicle Fabrication and Reliability

Fig. 15 (a) showed cross-section image of reliability test vehicle with 12µm Cu trace direct on glass and on PID which were formed by dry film photoresist. PID via opening is also shown in Fig. 15 (b) after the delopment process, the via diameter was 29µm on top and 21µm on bottom with 13µm in thickness.

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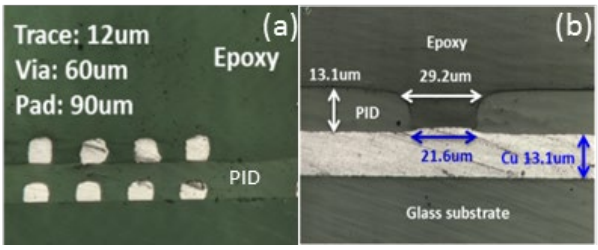


Fig. 15 (a) cross-section 3D laser microscopy image of core layer and build-up layer trace stack structure on glass (b) via formate by lithography process of PID on glass substrate

The resistance of the daisy chain on PID test vehicle was measured before and after thermal cycling test. From the initial, the daisy chain with 2500 blind via has 12~15Ω in resistance, which is close to the theoretical calculation. The resistance also has linear relationship to the counts of blind via as shown in Fig.16. After treated by pre-condition L3a process, which included 24hours pre-baking under 125 ℃,60% humidity thermal humidity baking (THB) for 40 hours, and 3 times of mass reflow in N_2 atmosphere, the shift of daisy chain resistance is less than 7%. The resistance still showed linear relationship to the via counts after TCT 500 cycles and 1000 cycles.

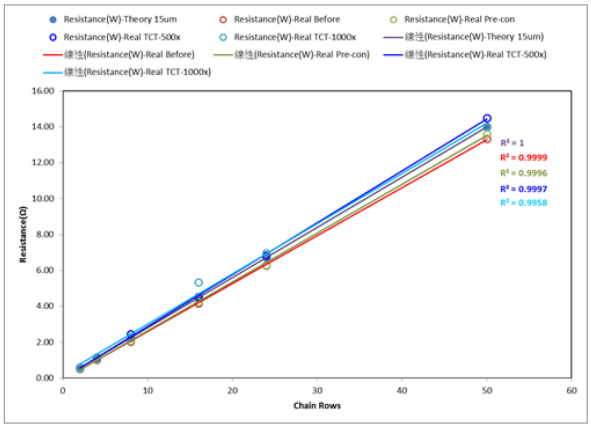


Fig. 16 The electrical measurement of the daisy chain after pre-condition L3a and TCT for 500x, 1000x and 1500x testing.

Fig. 17 showed the cross-section SEM of reliability test vehicle by using non-PID material on glass substrate with TGV (through glass via). The trace was formed by using dry film photo resist. The interconnection via was drilled by UV laser and the tilted SEM photo was shown in Fig. 17 (b) withoht smear in the via. Fig. 17 (c) showed the cross-section of 80μm TGV with funnel shape and conformal electric-plating Cu trace with 15μm in thickness by SAP process on 370mmx470mm glass panel with 410 μm in thickness.

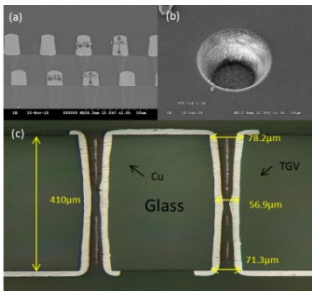


Fig. 17 (a)cross-section SEM of core layer and build-up layer trace stack structure on glass. (b)non-PID laser drilling via. (c)cross-section of TGV with conformal Cu plating on the TGV sidewalls and double side of the glass to form a glass structure.

The resistance of the daisy chain on non-PID test vehicle was measured to check the continuity of the daisy chain in nine test vehicle samples. The chain rows were measured from 2 to 50, and each chain row has 50 TGVs in it. The samples were subjected to the thermal cycle testing (TCT) for 1500 cycles, which consisted from -40℃ to 125℃. As shown in Table 5, the result showed all the samples and arrays passed the TCT test without delamination or crack, which means the 2-RDL test structure, is good enough for the TCT condition. In order to investigate the compatibility and reliability of Cu interconnections, this glass substrate was also subjected to highly accelerated stress testing (HAST). The condition of the HAST is 168hrs at 130℃ /100%RH. The test results showed the R shift of three samples that is lower than 1% (Fig. 18)

Table 5 The TCT test pass ratio of non-PID test vehicle.

Category	TCT 500x	TCT 1000x	TCT 1500x
1	0/9	0/9	0/9
2	0/9	0/9	0/9
3	0/9	0/9	0/9
4	0/9	0/9	0/9
5	0/9	0/9	0/9
6	0/9	0/9	0/9
7	0/9	0/9	0/9
8	0/9	0/9	0/9
9	0/9	0/9	0/9

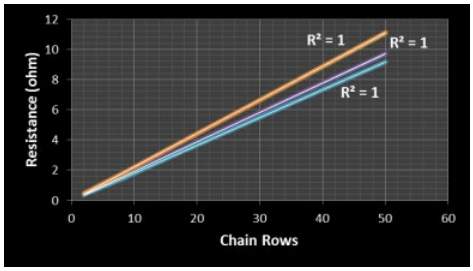


Fig. 18 The electrical measurement of the daisy chain after HAST testing.

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V. Conclusion

Glass material as RDL (Re-distribution layer) substrate or TGV (Through glass via) substrate by using dry film PID and non-PID material for multiple RDL layers integration were evaluated step by step in this work, such as

- The interface of cross-cutting testing, peeling strength testing and reliability
- Line/space 2/2μm~5/5μm evaluation by liquid photoresist, line/space 4/6μm evaluation by dry film photoresist
- Fine blind via 5~10μm evaluation by dry film PID
- Test vehicle integration and reliability

In this paper, the fine line, fine via for next general interconnection already tried to breakthrough these challenges by adapting materials of glass carrier (or glass core), new dry film photo-imagable dielectric (PID), photoresist and advanced equipment were also evaluated. The next steps will try to survey and evaluations are shown as below:

-The dry film photoresist for line/space 2/2μm~5/5μm
-The low loss PID material with Dk<3, Df<0.003 at 30GHz
-The fine line and fine via test vehicle interconnection integration with potential business

VI. Acknowledgment

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VII. Reference

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