

An overview of molded underfill in flip chip packaging applications

Fernando Roa
Amkor Technology, Inc.
1900 South Price Road
Chandler, AZ 85225 USA
Ph: 480 786 7586; Fax: 480 821 1713
Email: Fernando.roa@amkor.com

Abstract

Flip chip packaging is a wide-spread process used in high frequency, high IO count IC devices. It consists of joining the IC chip with the substrate using solder alloys or Cu pillars to form a continuous interconnection for the electronic signals to travel through. However, because during operation these devices dissipate heat, the temperature at the bumps interface rise and drop in cycles which cause thermal stress to build up due to the different thermal expansion of the materials. If left unchecked, these stresses will weaken and eventually cause fatigue failures. Therefore, stress absorbers are dispensed or underfilled to fill the gap between the substrate and the die. Underfills, as these materials are commonly known, are typically dispense as liquids using a variety of techniques like spraying, jetting, injection dispense, etc.

In this paper we'll discuss the benefits and challenges of a new type of process that integrates the overall encapsulation of the package with the underfill process in one single process step, called molded underfilling. We'll discuss this application for simple devices consisting of one IC chip and then extend the discussion towards more complex package configurations consisting of IC chips and passive components to demonstrate the flexibility and robustness of this new process solution.

Key words

Epoxy mold compound, molded underfill, System in a package, modules, encapsulation

I. Introduction

Flip chip interconnection has been around for many years as a reliable, high volume process for the fabrication of high performance ICs. This process consists in mounting Silicon-based Integrated circuits (or IC die) onto the mating pads of organic composite laminates (or substrates). However, to achieve this connection reliably, the use of an encapsulant material that can absorb the thermo mechanical stresses created by the large difference in coefficients of thermal expansion between the die and the substrate is required.¹

Briefly, standard flip chip CSP packaging consist of mounting the IC die on the substrate, such that the die bumps are resting on the corresponding substrate mating pads. After this, the units are taken into an oven which creates the solid interconnection; after cooling, the resulting package needs to be underfilled. This is typically achieved by dispensing an epoxy-based material near the edge of the die and allowing it to flow in between the die and the

substrate driven by capillary forces originating in the microscopic distances separating the surfaces of the die, the bumps and the substrate. This process is commonly referred as capillary under filling (CUF). A picture showing this process is shown in Figure 1.²

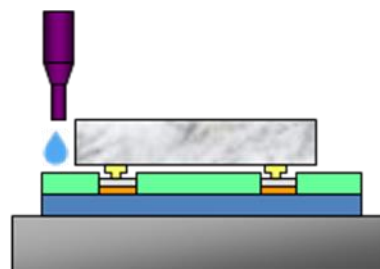


Figure 1. Capillary underfilling (CUF) process description

Although being quite a robust and mature process there are some aspects of this process that drive the search for potential alternatives: CUF is typically a slow process even with the best available equipment solutions, as the material

has to be dispensed unit by unit. Also, since the process is driven by a natural process (capillary force), the design and application of CUF can lead to voids and other yield concerns. Finally, underfill can't flow and protect the other IC surfaces; thus there is the need to perform a 2nd encapsulation process to fully isolate and protect the IC.

This 2nd process is normally done by molding of a 2nd epoxy-based material over the IC and the exposed area of the substrate. This 2nd process is usually referred to as overmolding. Figure 2 shows a typical construction for a finished IC package including the overmold material.

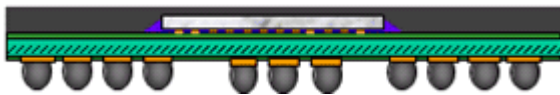


Figure 2. Finished IC package: underfill shown in blue, overmold in black

Thus, there is significant potential for process simplification and cost reduction by combining these two encapsulation processes (CUF + overmolding) into just one operation and by using just one epoxy mold compound (EMC), with the added benefit of simplifying the supply chain for the materials used in the package.

II. MUF: a new way to assemble flip chip packages

Driven by the potential to combine the two encapsulation processes (CUF + overmold), Amkor has invested significant efforts in developing a unified encapsulation process to realize the expected cost and process simplification benefits. This new process is called Molded Under Filling or MUF.

In this process, an epoxy mold compound pellet is melted at about 175°C and forced to flow, under pressure applied by a plunger, and fill a sealed cavity or chase where the bare packages reside. Thus, this type of MUF processing is denominated transfer mold process. Figure 3 graphically shows this process.

Because of the nature of this process, there exists a higher degree of control in the way the melted epoxy compound flows, a shorter cycle time in achieving full underfilling coverage, and if combined with the benefits of CSP packaging, then an overall assembly cycle reduction time since there is no additional encapsulation process needed.

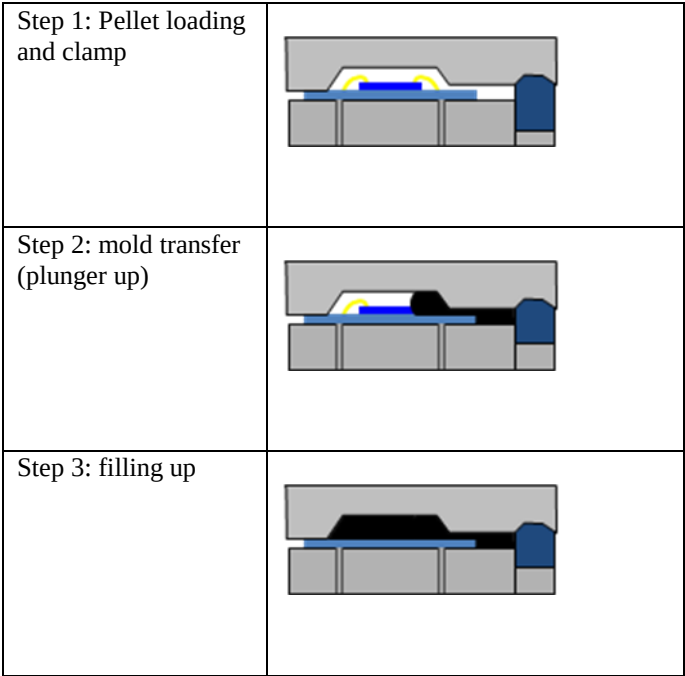


Figure 3. Transfer molding process steps

An alternate process, known as compression molding, uses powdered mold compound which is melted and compressed in situ, as shown in Figure 4.

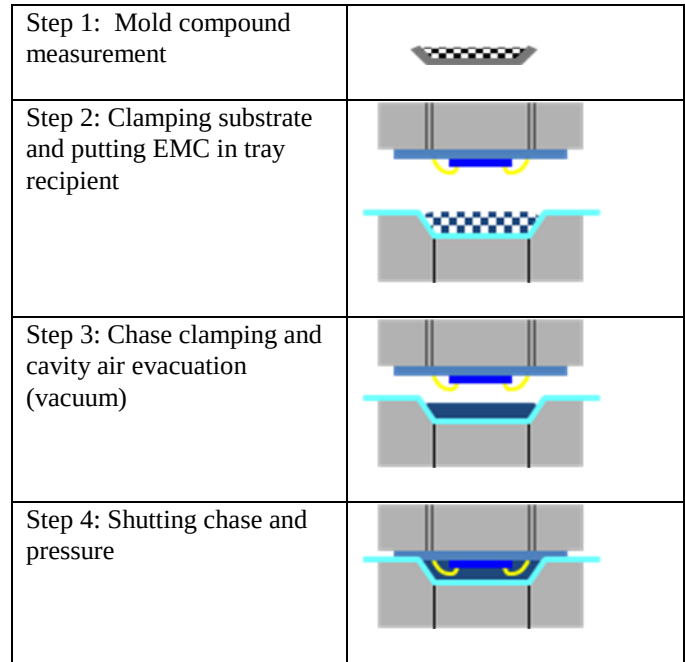


Figure 4. Compression molding process steps

It should be evident that the mold compound flows over and under the die, filling all cavities and spaces between silicon die, laminate and flip chip bumps. The finished packages look very much exactly like CUF-filled packages since the

mold compounds used for both processes are similar in color and finish. Thus, from a purely visual perspective, the change is not evident. From a yield and reliability point of view there are a number of differences of course.

In terms of processing, for example, the differences are quite significant, with MUF necessitating somewhat longer development timelines and more involved characterization at the initial stages to account for differences in material properties, package attributes and package configuration. Table 1 shows a relative comparison between the properties of a typical underfill vs a mold underfill epoxy compound.

Table 1. Comparison of properties of typical materials used for MUF and CUF processes.

Property	Units	MUF	CUF
Filler Wt Content	%	85	65
Nom. Filler Size	um	6.1	0.6
Max Filler Size	um	25	3
Viscosity	Pa-S	9.5	50
Tg	C	153	117
CTE Alpha 1	ppm/c	12	31
CTE Alpha 2	ppm/c	45.25	90
Flex Modulus (< Tg)	Gpa	18.875	11
Flex Modulus (> Tg)	Gpa	0.4	0.15

As seen in Table 1, typical mold compounds have higher more filler loading, with larger filler size distributions, which in turn cause an increase in viscosity and overall difficulty for filling all spaces. It must be remembered that capillary underfill materials are liquid at room temperature while mold compounds come in solid prefabricated pellets or tablets. MUF formulations however come with a variety of additives and modifiers to improve flow, fillability, mold chase release, cure time, warpage, appearance, etc. It is common to test multiple MUF mold compound candidates when starting a new project and a variety of selection criteria are used to downselect to the optimum materials for production.

But materials alone are not the only difference with regular encapsulation technology. Specialized molding tools should be used for the processing of molded underfill; this is because the presses used for regular encapsulation can't drive these higher viscosity materials and push them to fill inside the small cavities under ICs and other mounted components. Thus, a MUF tool is equipped with powerful vacuum pumps to help drive the EMC material. But so high a vacuum also increases the requirements for air-tightness and mating planarity for the mold chases as well as increases the complexity of the venting mechanisms to insure they are not blocked by the finer filler particles used

in the MUF materials. Finally, these tools are also regularly rated with higher tonnage than the regular encapsulation presses.

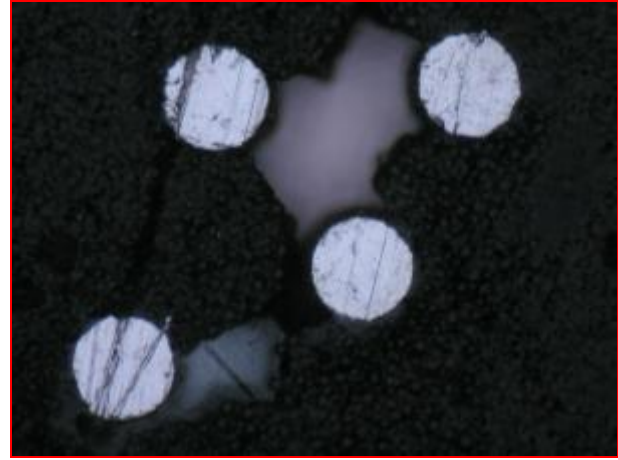


Figure 5. MUF voids. Circles are solder bumps, the black granular section is the EMC area and the irregular whitish areas are the voids.

Most common yield concerns with MUF include mold voids, mold flash during processing, excessive warpage after mold cure and solder extrusion caused by voids. All of these must be addressed to insure a successful ramp is achieved with yields that match those of legacy technologies.

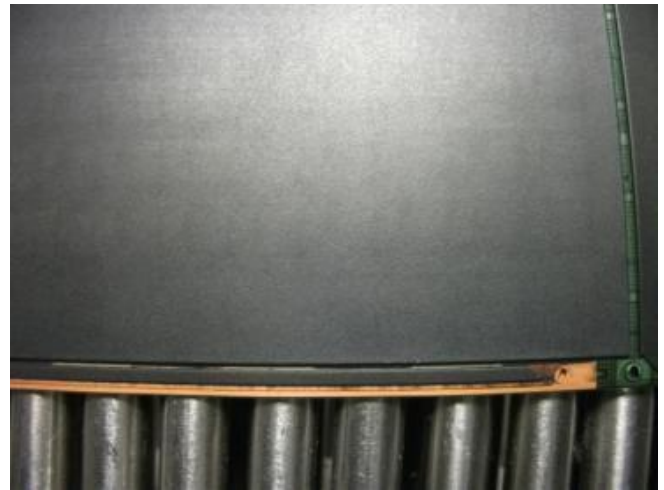


Figure 6. Mold flash during MUF processing.

In particular, MUF voids are caused by many factors: contamination, incomplete melting of the pellet, different mold flow fronts encircling pockets of air before the vacuum systems have a chance of evacuating them, filler particles blocking mold flow, areas surrounded by bumps or features at very tight pitches, residues left over from a

defective cleaning of flux used for flip chip bonding, etc. For systemic problems, i.e., not caused by excursions, screening evaluations and blind controls are needed to establish the nature and root cause of the voids; then process optimization, material selection or product design or configuration changes are required to address the problem.

Mold flash is commonly caused by fine filler particles in the mold compound that escape the mold cavity through the venting systems or through areas where the mold chase is not perfectly seated on the substrate, as shown in Figure 6. Tight control of the filler distribution of the mold compound is key to eliminate this problem as well as insuring the flatness of the substrate area where the mold chase is going to land.

Finally, the tendency of the epoxy polymeric chains to shrink as they crosslink with each other, during the mold cure step, creates another challenge in the form of warpage. Warpage of the unit (as absolute warpage or its proxy, coplanarity) is a serious enough concern for surface mounting. Yet, it is also a significant concern for downstream operations from mold, for the assembly house since the processing unit there is a CSP strip, composed of many units. So, typically, the warpage seen at the CSP level is many orders of magnitude that of the single unit.

To solve this problem, different approaches have been devised. Proactively speaking, balancing of the thickness, size and thermal and mechanical properties of the different module components has to be achieved; this usually is done by performing a finite element model of the silicon, substrate, mold and bumps and determining the resulting warpage to be expected. If the modeled warpage exceeds the processing go criteria, changes to die or substrate thickness, different mold compound formulations, and other changes must be implemented. Alternatively, to counteract the natural tendency of the mold to shrink, snap cures or the use of weights during curing are often also used.

III. Molded underfill for system in a package modules.

In general, the same considerations discussed above for the case of single die and substrate apply when passives are mounted along with the flip chip die on the substrate. There is significant production where devices including SMTs are overmolded. A point of concern with flip chip modules is that there are competing priorities for the proper selection of a process and bill of materials: on one side the need to completely fill the gap under the die, which generally has tighter interconnect pitches than the passives; on the other

side, the passives tend to collapse more after SMT reflow; thus the space available for the mold compound to flow and fill the cavities under the passives is less. This issue notwithstanding, the real concern is solder extrusion which can easily occur in these cavities not sealed by the MUF compound.

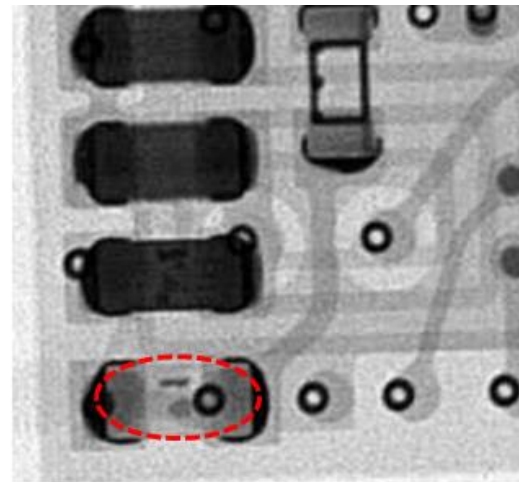


Figure 7. Solder extrusion occurring under a 0201 component after SMT reflow.

In order to address these concerns, some ingenious design rules have been used for SMT packages tailored for MUF processing.

IV. Conclusion

In this paper, we discussed the promise for process simplification and cost reduction provided by molded underfill over traditional capillary underfill assembly solutions. We provided an overview of the development challenges and successes of converting regular capillary underfill products to a single molded underfill process with emphasis in the needs for improved package design, material formulation and equipment selection and tuning. MUF is a highly reliable, repeatable process, with great promises for cost reduction through process and material consolidation. Some trade-offs remain in terms of design for manufacturability and tailored development ramps.

Acknowledgment

The author acknowledges the help provided by the Amkor factory teams in Korea, Philippines and China.

References

- 1 Tummala, Rao in *Fundamentals of Microsystems Packaging*. McGraw-Hill, 2001. Pg 271- 280

- 2 Ying, M; Tengh, A.;Yew, CC; Mohtar, A.; Pak WW. *Process Development of Void Free Underfilling for Flip-chip-on-board* in Electronics Packaging Technology Conference, 2007, pg 805-810.
- 3 Islam, N.; Darveaux, R.; Jimarez, Miguel in *Molded Flip Chip – FCmBGA* – White paper at IMAPS International Conference and Exhibition on Device Packaging, March 17-20, 2008