

Glass Based Inductors, Capacitors and System-In-Package for RF Applications

Jeb H, Flemming, Roger Cook, & Kyle McWethy
 3D Glass Solutions, Inc.
 5201 Venice Ave, NE
 Albuquerque, NM, 87113, USA
 Ph: 866-559-8982; Fax: 866-561-0975
 Email: info@3DGlassSolutions.com

Abstract

Glassy materials offer a number of advantages over traditional packaging materials, such as laminates and ceramics including: (1) Better material properties, (2) decreased surface roughness to mitigate current crowding, (3) the ability to create small precise features with greater densities, and (4) the opportunity to integrate passive devices such as power inductors and High-Q inductors into an interposer substrate along with other active and passive devices. This paper will cover an overview of our efforts to create APEX[®] Glass based devices that form the building blocks for a variety of RF applications including power inductors, High-Q inductors, capacitors, filters and interposers. We also demonstrate the power of integrating these individual building blocks into more complex devices that offer compelling solutions for the increasingly complex RF market. Performance data is presented for power inductors and the in-glass inductors.

Key words

Glass, High-Q, Inductor, Packaging, Through Glass Vias

I. Introduction

Glassy materials offer a number of advantages over traditional packaging materials [1], such as laminates and ceramics, including: (1) better material properties, (2) decreased surface roughness to mitigate current crowding, (3) the ability to create small precise features with greater densities [2], and (4) the opportunity to integrate passive devices such as power inductors into an interposer substrate itself along with other active and passive devices [3, 4].

Several glass manufacturing techniques are available on the market today for the formation of through glass vias (TGVs) for I/Os and interconnects, including laser ablation, electrostatic discharge, ultrasonic milling, and wet chemical etching. While each of these approaches have unique advantages, wet chemical etching offers a number of benefits. These include: (1) process simplicity, (2) low processing tool capital cost, (3) batch manufacturing for lower production costs, and (4) the decreased formation of micro-fractures between structures, commonly seen in processes that input high levels of thermal and mechanical stress to the glass.

The presented work describes a high performance glass

ceramic material that enables the production of highly anisotropic 3D structures in glass using photolithographic patterning, baking, and wet chemical etching. With this material, features of any pattern may be etched into the glass. Features such as circular Through Glass Vias (TGVs), trenches, and coils may simultaneously be microfabricated using a precise, rapid, and cost effective batch manufacturing process.

A. Glass for RF Passive Devices

RF passive devices are produced using a variety of material sets, including glass reinforced epoxy laminates (such as FR-4), silicon liquid crystal polymer, and ceramics. For a number of reasons, including surface roughness, material constants (such as dielectric constant, loss tangent, Young's modulus, etc.), manufacturability, and cost, the RF community is continuously looking for new materials for device packages as new applications and product geometries continue to push current material property limits.

The presented photosensitive glass ceramic material is a dielectric material very similar to other types of glass, such as BK7 (Schott) and is able to be processed using standard

IC processing techniques. Table 1 below shows some relevant material properties specific to RF electronics.

Table 1: APEX® Glass Ceramic Material Properties

Young's Modulus	81 GPa
Electrical Resistivity	$10^{12} \Omega$
Coefficient of Thermal Expansion	10 ppm/K
Loss Tangent (3.3 GHz)	0.0086
Loss Tangent (10.2 GHz)	0.0106
Dielectric Constant (3.3 GHz)	6.58
Dielectric Constant (10.2 GHz)	6.575

The presented photosensitive glass ceramic is processed using a simple three-step process (Fig. 1). First, a standard lithography mask is placed directly onto the glass wafer and the wafer is exposed to ultraviolet light (Fig. 1A). During this step, photo-activators in the glass become chemically modified. In the second step of the production process, the wafer is baked (Fig. 1B). During this step of the baking process, any previously exposed regions are converted into a ceramic state, where increased levels of exposure lead to more complete ceramic formation.

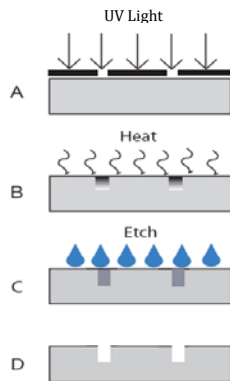


Fig. 1. Processing steps of presented glass ceramic.

In the final processing step (Fig. 1C), the wafer is etched in a dilute hydrofluoric acid solution, etching the ceramic state 60 times more preferentially than the glass state. In this manner a wide variety of features, such as posts, wells, TGVs, microfluidic channels, blind vias, or other desired features are gently wet etched (Fig. 2). The desired structure depth can be controlled by etch concentration, processing duration, bath temperature, and etching direction.

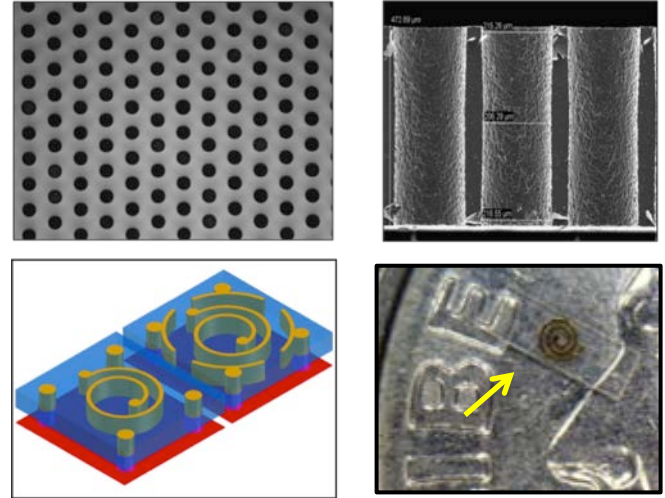


Fig. 2. Top Left: An array of 60 μ m diameter, 120 μ m pitch, through holes in glass. Top Right: A cross section of the described through holes showing the anisotropic etch profile. Bottom Left: A rendering of the described RF power inductors. Bottom Right: A produced power inductor resting on a US Dime.

B. Wet etch vs. laser ablation for non-circular structures

Several companies and academic organizations are focused on the production of features in glass using high power lasers. While this process has shown good success in the creation of round TGVs there are several inherent concerns associated with laser ablated TGVs. These include: (1) laser ablation tools are very costly, easily exceeding \$2M; (2) by design ablation manufacturing approaches are serial, able to produce only small arrays of circular TGVs on a single wafer at one time; (3) ablation process commonly sputter a large amount of debris around the holes that may interfere with further processing steps; (4) the sidewall of laser ablated TGVs typically range from 60-80°; and (5) they may inject a large amount of heat shock into the glass substrate creating micro-fractures that lead to decreased material strength of interposer packages, decreasing product reliability.

In contrast, the processing of photosensitive glass ceramics is accomplished by leveraging the physical and chemical difference between the glass state and the manufactured ceramic state. Therefore, features in photosensitive glass ceramics are produced using a wet chemical etching process.

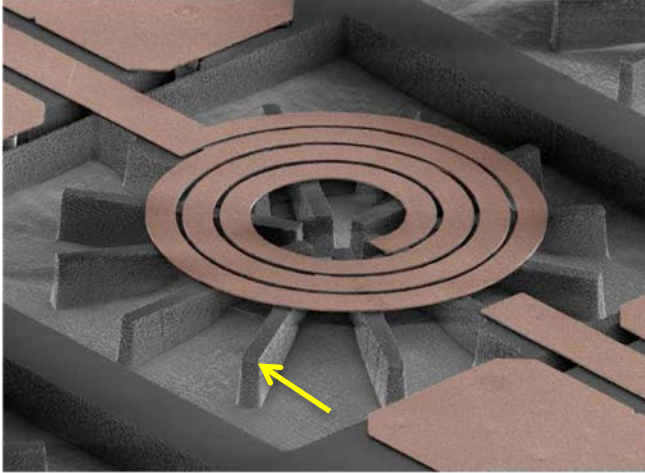


Fig. 3. Example of non-circular features produced in glass ceramics. Colored portions of the images are copper. In this image a 50-micron wide copper trace is resting on 20-micron wide glass rails (Yellow Arrow).

Using photosensitive glass ceramics it is possible to produce an unlimited variety of structures in addition to TGVs. In the production of power inductors, the manufacturing process allows for a coil shape to be etched into the glass with micron-scaled precision. Next, the etched regions are filled with copper. This process allows for the production of copper coils with placement and line width precisions of less than 5 microns, producing devices with extremely repeatable performance.

II. Results

A. Power Inductors and Experimental Results

Power inductors are utilized in a number of product areas including power amplifiers, voltage controlled oscillators and matching networks for antennas and filters. Historically, surface mount high-power inductors have been limited to copper wire wound around a ceramic core for power handling. These surface-mount devices typically can only handle up to 1.5 amps and are more than 1mm in height. This large height oftentimes prevents them from being used in many applications that possess limited package headspace. In contrast, power inductors manufactured in photosensitive glass ceramics may be as thin as 0.2mm and are capable of withstanding up to 2.8 amps of power with less than 40C rise above ambient temperatures. Furthermore, at 1GHz these inductors are capable of producing Quality Factors of more than 40 at 6.5nH.

Testing of the produced parts was accomplished using a 2-port shunt measurement approach. This measurement approach incorporates a T-Network, which allows for the

de-embedding of measurement parasitics using ABCD matrixing. Within this model the inductance and Quality Factor may be calculated.

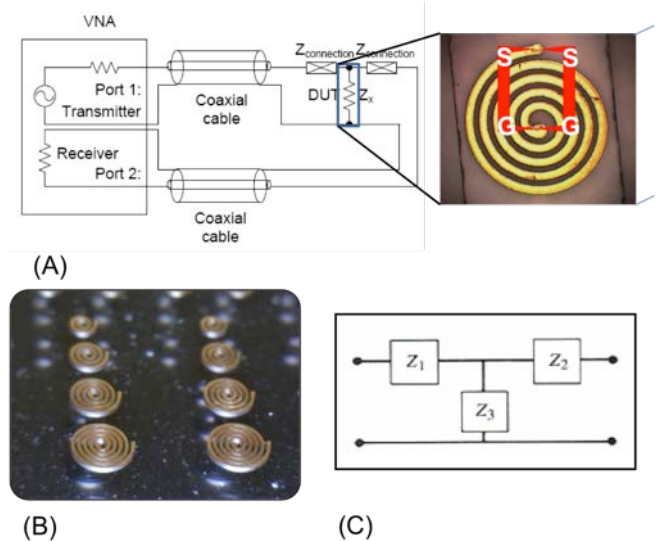


Fig. 4: (A) A schematic layout of the 2-port shunt measurement approach. (B) Production devices of the power inductors with varying number of turns. (C) The above discussed T-Network Illustration where $Z_3 = Z = R + j\omega L$, where Quality Factor (Q) $Q = R/\omega L$.

All power inductor designs were modeled using EM Pro software from Keysight Technologies using standard 2 port simulation methods. Inductors of 3.5 turns were simulated to have an inductance of 4.8nH at 1GHz. The Inductance and Quality Factor results from these measurements are shown below in Figure 5.

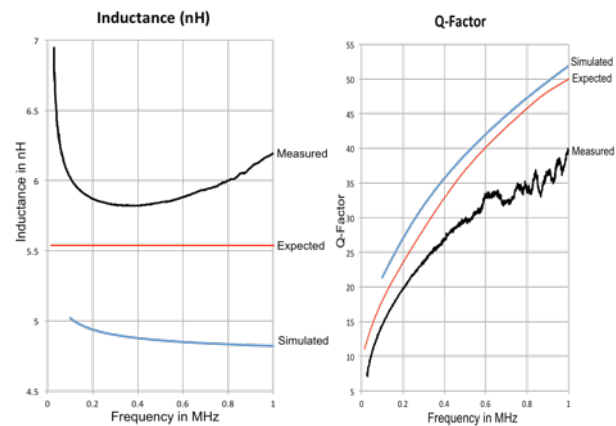


Fig. 5: Measured vs. Simulated results for inductance (Left) and Quality Factor (Right).

Slight differences exist between the simulated and measured values. This is attributed to several differences. The tested parts were thicker than modeled. The modeled power inductors had a thickness of 200 microns. The tested parts had a thickness of 280 microns. Also, there was

additional parasitic capacitance due to the thickness differences and potentially from the test set-up during analysis that were not in the model.

1.75 and 3.5 turn inductors were tested for their current handling ability using Würth Elektronik testing methods [5], where maximum current handling is defined to increase device temperature 40°C above ambient temperature.

Table 2 below shows the results of this testing, where various current loads were applied to the devices and the temperature rise of the inductor was measured. In this testing, the 1.75 turn power inductor was able to carry 2.8 amps and the 3.5 turn power inductor was able to carry 2.2 amps.

TABLE 2: Summary of 1.75 & 3.5 Turn Inductor Power Current Handling

1.75 Turn Sample					
Current Amps	Voltage mV	Ambient Temp °C	Inductor Temp °C	DC Resistance Ω	Temperature Rise °C
0.50	41.3	22.0	23.4	0.082	1.4
1.00	82.5	22.1	25.5	0.082	3.4
1.50	123.9	22.4	30.1	0.082	7.7
2.00	165.7	22.6	35.9	0.082	13.3
2.25	142.6	23.0	45.2	0.063	22.2
2.50	168.3	23.1	51.3	0.067	28.2
2.75	197.8	23.4	59.5	0.071	36.1
2.80	204.8	23.5	61.4	0.073	37.9

3.5 Turn Sample					
Current Amps	Voltage mV	Ambient Temp °C	Inductor Temp °C	DC Resistance Ω	Temperature Rise °C
0.50	116.1	23.6	25.4	0.249	1.8
1.00	236.7	23.8	30.6	0.237	6.8
1.25	300.3	24.2	34.7	0.240	10.5
1.50	362.2	24.8	40.0	0.241	15.2
1.70	406.7	25.3	45.3	0.239	20.0
2.00	499.1	23.8	57.0	0.249	33.2
2.20	560.1	24.0	65.5	0.254	41.5

B. High-Q Inductors and Experimental Results

In addition to power inductors, a number of inductors have been designed with the goal of creating high-Q inductors in the range of 1.5nH to 10nH. Instead of an in-glass coil, we have created a design that we call a stitched inductor that incorporates a top and bottom metal pattern in addition to copper filled TGVs (Fig 6). This design approach allows a lot of design flexibility including number of turns, distance between turns, glass thickness, etc. These design flexibilities allow for a single inductor design to be adapted to many different footprints and packaging methods without compromising on the inductor layout keeping performance as close as possible between different packaging methods.

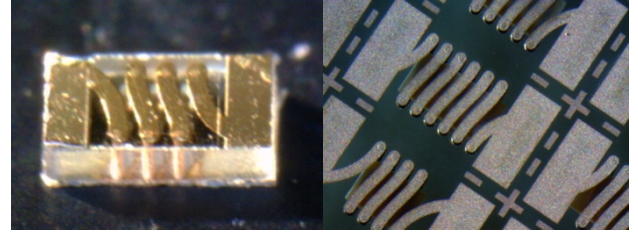


Fig. 6: Image of 3 (left) and 6 turn (right) stitched inductors.

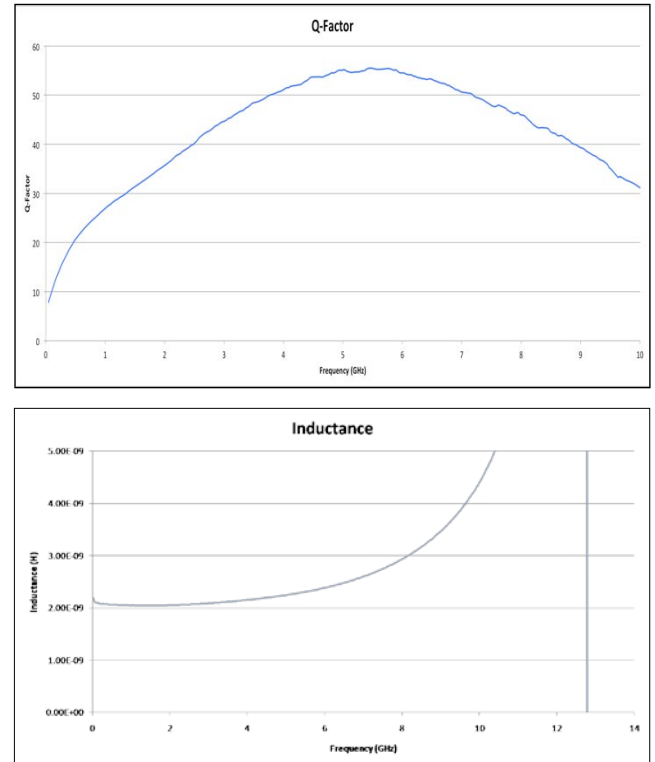


Fig. 7: Top: Measured Vs. Simulated Q-Factor, Bottom: Measured inductance.

The 2nH stitched inductor design was tested by Modolithics (Fig. 7). The inductance measured within 10% of simulation excluding differences related to SRF.

C. In-Glass Capacitors and Experimental Results

Capacitors can be built using the same manufacturing approach as was used for the power inductors. Much like the power inductors, in-glass capacitors rely on a patterned structure filled with copper. This structure, instead of being a coil, consists of parallel lines with each line being connected to an alternating side of the capacitor (Fig. 9). This method utilizes the inherent dielectric constant of the glass and full height of the substrate, thus improving coupling density when compared to standard comb capacitors and edge coupled traces. Furthermore, using the native glass dielectric properties enables the production of a capacitor with a breakdown voltage greater than 1,000

volts. The process is much cheaper than higher capacitance density processes that rely on a deposited thin film dielectric while still providing a capacitance range that is good for RF filter applications. Capacitance values of 0.1 – 10pF are being targeted and initial data on actual devices correlates to within 10% of modeling. These in-glass capacitors can provide a similar capacitance to that of deposited thin film processes with the benefit of having a much higher breakdown voltage.

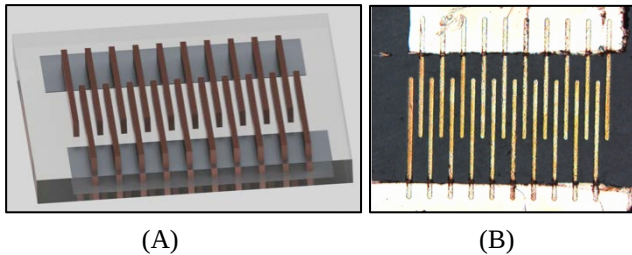


Fig. 8: (A) Modeled and (B) actual in-glass capacitors

D. RF Filters and Experimental Results

Due to the in-glass capacitors and high-Q inductors sharing the same process flow, incorporating inductors and capacitors onto a single compact part is not only simplified but also cost effective. The process used also allows unique grounding, isolation and filter component designs that could reduce common nuisance effects such as loop inductance (Fig. 9). This should offer tremendous advantage compared to having to source and package individual devices for each filter.

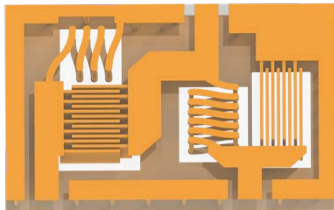


Fig. 9: A simple diplexer design that combines inductors and capacitors.

All of the building blocks are in place for creating RF filters utilizing our glass processing methods described in this paper. 3D Glass Solutions is in the early stages of building complete RF filters with the goal of understanding which product applications will have a good match to our specific technology capabilities.

E. Interposers and Complex Integrated Designs

The same photosensitive glass ceramic process used to build capacitors and inductors can also be used to create a number of other custom products such as interposers,

antennas, microfluidic channels, sensors and optical wave guides (Fig.10). All of these products can be built using the same base process and the small form factors are compelling for today's mobile electronics market. Interposers are one market that has received wide spread interest in the electronics community in recent years, with glass based interposers considered an economical option. This technology has been used to build proprietary interposer designs for a number of customers with good success. Although interposers alone are compelling from a market perspective, interposers with integrated passive devices would be even more compelling. We expect to see these types of integrated products in the market over the next 1 – 2 years.

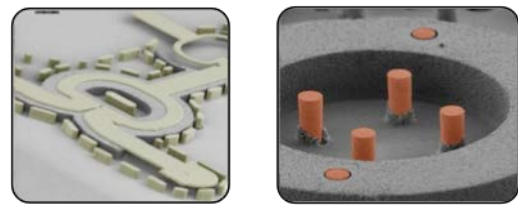


Fig. 10: Left: Electronic device with parameter shielding. Right: Micro-cavity with copper pillars (colored) which go to the backside of the package for metal redistribution

Conclusions

Glass based power inductors, high-Q inductors and capacitors have been demonstrated utilizing photosensitive glass ceramic material and the inherent processing advantages of this material. More complex systems such as glass-based interposers have also been demonstrated. The presented glass ceramic is an ideal substrate for the production of complex 3D structures in glass including passive inductive devices, RF filters and System-in-Package devices. Wafer processing is accomplished through standard batch IC processes enabling a low-cost alternative to ceramic, laminate, and polymer based substrates.

References

- [1] Töpfer, M., et al., *3D Thin Film Interposer based on TGV (Through Glass Vias): An Alternative to Si-Interposer*, 2010, ECTC Proceedings, pgs. 66-73
- [2] Sukumaran, V., et al., *Design, Fabrication and Characterization of Low-Cost Glass Interposers with Fine-Pitch Through Package Vias*, 2011, ECTC Proceedings, pgs. 583-588
- [3] Lai, W.C., et al., *300mm Size Ultra-Thin Glass Interposer Technology and High-Q embedded Helical Inductor (EHI) for Mobile Application*, 2013, IEEE International Electron Devices Meeting.
- [4] Sridharan, V., et al., *Design and Fabrication of Bandpass Filters in Glass Interposer with Through Package Vias (TPV)*, 2010, ECTC Proceedings, pgs. 530-535

- [5] Klein, Stefan, Application Note: The Sham of High Rated Current, August 2013, retrieved from URL:mouser.com/pdfdocs/The_sham_of_the_high_rated_current.PDF