Glass Wafers as Support Carriers for Wafer Thinning Processes

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1. **Introduction**

As the industry strives to get more logic packed with the same power demand on the same footprint, the thickness of silicon device wafers needs to decrease, meanwhile its diameter increases. In the thinning process, the silicon wafer will be bonded face down to a carrier and then ground down to the desired thickness. After this process step, device wafer and carrier wafer will be separated again. Silicon wafers are often used for carrier wafers, but some engineered glasses have a number of attributes that make them well suited for use as carrier wafers. All carrier materials need to meet specific requirements including: strength to withstand handling; low particle and metal contamination; and a coefficient of thermal expansion (CTE) matching the application requirements. Non-uniformities in the carrier directly impact the accuracy of the silicon wafer total thickness variation (TTV). Other important requirements include excellent flatness, high thickness uniformity, and low warp. Easy inspection of the bond layer and the use of advanced low temperature de-bonding techniques are also desirable for the large diameter silicon wafer precision thinning processes. We will demonstrate that glass can be engineered to be a good candidate for use as a carrier substrate and show how the strength of engineered glass wafers compares with silicon wafers using standard mechanical strength test methods. Even though the mechanics of failure differ greatly between crystalline materials (Si) and amorphous materials (glass), the data shows that the strength of a glass wafer compares favorably to that of a silicon wafer. In addition, we will present data on CTE, flatness, warp, and TTV for glass wafers. The data will support the conclusion that engineered glass wafers represent an ideal candidate for carrier substrate in the large size precision silicon wafer thinning process.

2. Thinning Process For IC Stacks

A thinned silicon IC wafer is very difficult to handle. Therefore it generally requires the use of a carrier substrate attached with a temporary bonding method as an aid to handling. During this process, the device wafer is temporarily bonded to the carrier wafer with an adhesive, the back of the silicon device wafer is ground to the desired thickness, and the device and carrier wafers are separated for further processing (see Figure 1 on page 5).

3. Glass Wafers

TTV and Warp

When using the temporary bond/de-bond process for thinning operations, it is important that the carrier/adhesive/wafer stack have a TTV that is minimized and less than a few microns. This means that the carrier wafer must start out with very low TTV.

The history of Corning glass for LCD displays was recently published highlighting the fusion process for making glass [2, 3]. In this process the glass flows over the edges on both sides of a trough rejoining underneath the trough. The fusion process is shown in Figure 2. The pristine outer edges of the glass do not touch any of the forming surfaces and are contact free. As a result, the surface of the glass is extremely smooth and defect free.

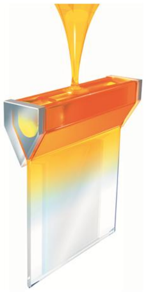

Figure 2. Corning Fusion Process

A critical feature of the fusion process for LCDs is to minimize thermal stress effects in the glass. With very little thermal stress in the glass, the warp can be very low. Enhancements to the fusion draw process can also be leveraged to produce wafers with exceptionally low TTV. Production of 300 mm diameter wafers with TTV < 2 µm and warp <30 µm is readily available today. Because no polishing is required it allows for easier volume scaling and positively impacts substrate reliability (see Figure 3).

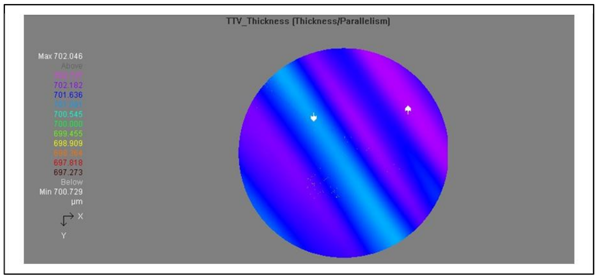

Figure 3. Glass wafer with TTV less than 2 µm

Additional advantages of using the fusion process for generating carrier substrates are due to flexibility with respect to size and thickness. Since the fusion process provides sheets with dimensions of more than three meters, it is straightforward to provide wafers of almost any size. Wafers up to 450 mm in size are readily manufactured today.

Warp as defined by ASTM Test Method F657 is the difference between the high and low points of the median surface of an unclamped wafer. Gravitational force can cause substantial flexing of large diameter wafers, whether they are supported at the edge or near the middle, and unless compensated, can cause an error in warp measurements. ASTM F1390 provides two approaches which aims to correct the gravitational effect [5].

A new interferometric measurement technique has been developed to overcome the limitations described above. The FlatMaster® MSP-300 (Multi-Surface Profiler) System (see Figure 4) is based on a new frequency scanning technology. This system has a field of view of >305 mm and measures absolute height, flatness and parallelism of multiple surfaces. It is well-suited to quickly (~ 1 minute total measurement time) characterize wafer flatness (warp, bow) of silicon and glass wafers with vertical accuracy of < 1 µm. The system utilizes a 2k x 2k camera, which gives sub-millimeter lateral resolution in wafer characterization. Each pixel of the camera represents a point of direct measurement on the wafer – means that on a 300 mm diameter wafers there is on the order of 3 million actual direct measured data points. Contrast this to current methods which are frequently hundreds or maybe a few thousand points, with extensive interpolation, which means much of the wafer remains uncharacterized. For glass wafers (transparent at operating wavelength) the FlatMaster® MSP-300 enables simultaneous measurement of flatness, thickness, and TTV. The system provides the ability to characterize up to 1 mm of bow with micron level accuracy. Thickness and TTV accuracy are < 1 µm and < 0.1 µm respectively. [7] Figure 5 shows a Corning glass carrier product with very low warp (26 µm) and total thickness variation (0.8 µm). The detail given by the high data density is evident in this figure.

Figure 4. FlatMaster® MSP-300 Interferometer

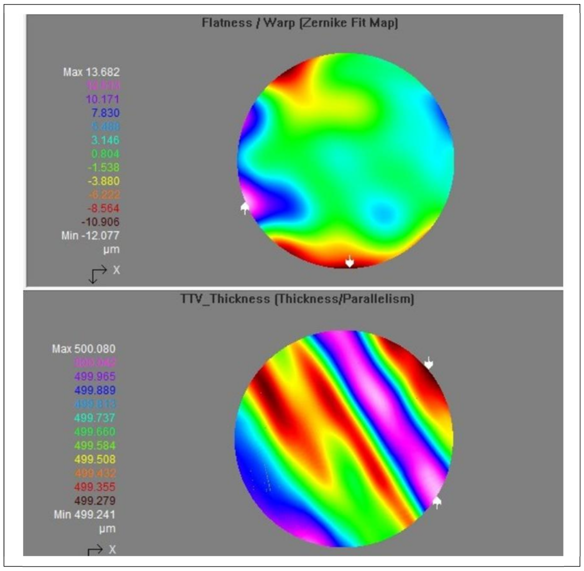

Figure 5. Champion 300×0.7mm wafer - 26µ warp & 0.8µ TTV show 1 µm TTV sample

Strength

Wafer breakage is a major concern in semiconductor manufacturing lines since it results in significant costs and disruptions. Silicon wafers typically break by cleaving along crystallographic planes. Glass breaks by brittle fracture. However, both substrates are considered highly brittle materials. This means for both materials their strength depends on the presence of flaws (micro-cracks, etch pits, etc.) rather than the intrinsic material properties. When more flaws exist, there is a higher statistical probability of failure when loads/stresses are applied to the wafer during manufacturing processes. This increases the importance of methods used in wafer preparation, making management of grinding and polishing processes extremely important [6]. In the next sections, we discuss some baseline data on the practical strength of glass and silicon.

Even though the fracture modes are different it is useful to compare the fracture strength of a silicon wafer surface to a glass wafer surface by using standardized test methods. A ring-on-ring test is appropriate for surfaces. The ring-on-ring technique consists of two concentric rings. The larger ring is positioned on the bottom, the smaller ring on top and the wafer under test placed between the two rings. The force is applied to the top ring creating a region of uniform tensile strain in the lower surface of a wafer material. The applied force is increased until failure occurs by fracture from a flaw.

To evaluate the statistical nature of the failures it is useful to put the fracture data onto a Weibull plot. Figure 6 shows a Weibull distribution of 300 mm diameter silicon wafers and glass wafers. The median strength values are almost identical for both materials. The relatively steep slope given by the glass wafers in Figure 6 results in a more repeatable, predictable performance and avoids the very low strength specimens seen in the silicon population.

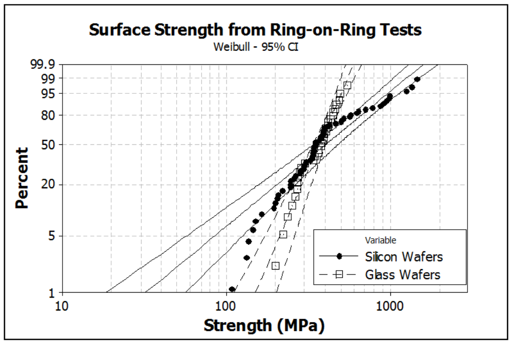

Figure 6. Ring-on-ring results for glass and silicon wafers.

Edge Strength

Edge strength and proper notch design is another key factor of the reliability of glass as a carrier substrate in the precision thinning process. Edge design depends on the manufacturing process and should not impact edge strength. Figure 7, shows the edge strength of standard silicon wafers, and glass wafers finished with four different processes. Clearly the edge strength is more a function of the process used rather than material, which is due to the properties of brittle materials.

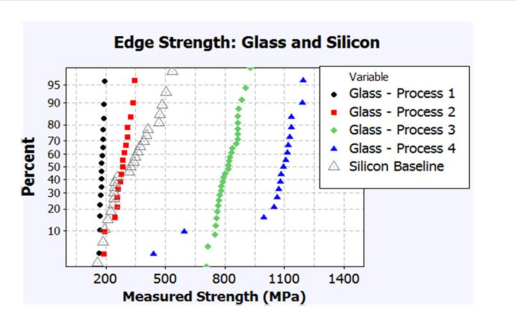

Figure 7. Edge strength of glass carrier wafer

Stack TTV

In order to have good uniformity in thinned wafers, it is important for the TTV of the bonded stack to be low. Several wafer stacks were bonded using the 3M™ wafer support system using glass carriers with two different TTV populations: 1) ~ 2 µm, 2) ~6 µm. These glass carriers were bonded to silicon wafers and the stack TTV was measured. The trend shown in Figure 8 is clear; total stack TTV is lower if the glass carrier TTV is low. Another aspect of this is that the TTV must be characterized in a reliable manner. Figure 9 shows the TTV of the same 10 (polished, not fusion formed) glass carriers measured using three different techniques. Two of the methods utilized << 100 data points and reported a TTV on the order of 1 µm. When these same carriers were measured on the FlatMaster® MSP-300, the high data density showed that the actual TTV was often times > 5 µm! As you can see from Figure 8, this would have tremendous impact on the TTV of the bonded stack and ultimately the thickness of the thinned Si wafer. While the fusion process provides significant advantages in providing carrier wafers with low TTV in a reliable manner, having the correct metrology, such as the FlatMaster® MSP-300, is important to make sure that the wafers are properly characterized prior to downstream operations.

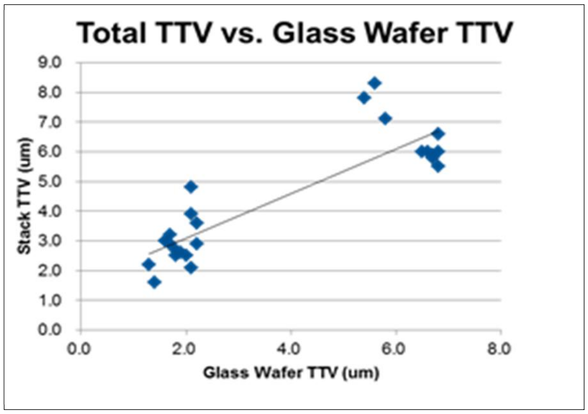

Figure 8. Bonded Stack TTV vs. Glass Carrier TTV

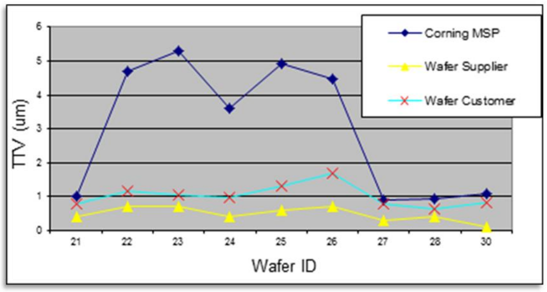

Figure 9. Measured TTV is strongly dependent on the method used. The high data density from the FlatMaster® MSP-300 provides important information whereas limited data sets can under-report total wafer TTV.

Conclusion

Any carrier material for large diameter silicon wafer precision thinning processes needs to meet requirements such as strength to withstand handling, low particle and metal surface contamination, and a CTE, which closely matches silicon. The Corning fusion process allows substrates with excellent flatness, high thickness uniformity, and low warp. Easy inspection of the bond layer and the use of advanced low temperature de-bonding techniques are available due to the glass' inherent transparency.

As we illustrated, glass can be engineered to be a good candidate for being a carrier substrate. The strength of Corning glass wafers compares with silicon wafers using standard mechanical strength test methods. Even though the mechanics of failure differ greatly between crystalline (Si) and amorphous materials (glass), the data show that the strength of a Corning glass wafer compares favorably to that of a silicon wafer. In addition, data on flatness, warp, and TTV demonstrate that Corning glass wafers represent an ideal candidate for carrier substrate in the precision silicon wafer thinning process.

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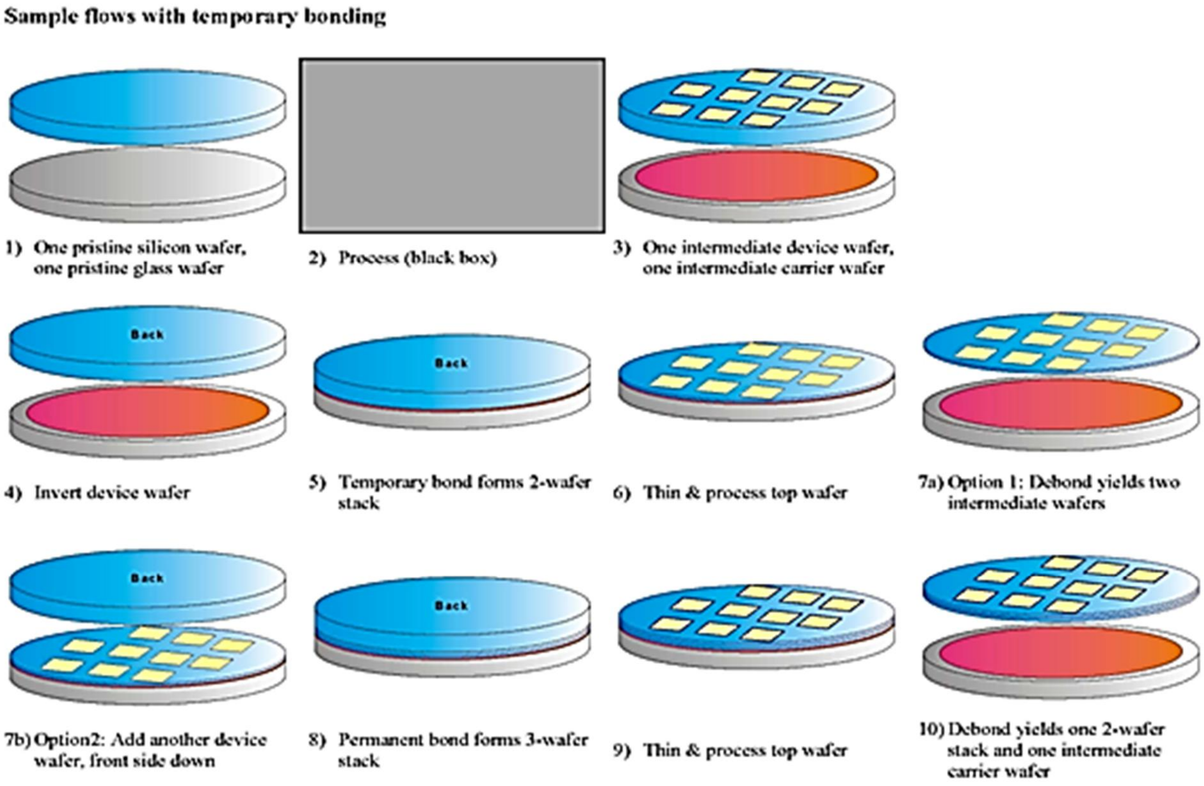

Figure 1. Temporary bonding example flow for a process by which two wafers, only one of which as circuitry and TSVs, are bonded together, the processed wafer thinned, and the pair de-bonded [1].