Optimization of laser release layer, glass carrier, and organic build-up layer to enable RDL-first fan-out wafer-level packaging

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Abstract

With increasing demand for mobile devices to be lighter and thinner and consume less power while operating at high speed and high bandwidth, many equipment suppliers and assembly participants have invested great efforts to achieve fine-line fan-out wafer-level packaging (FOWLP). However, the inherent warp of reconstituted wafers, which can contribute to poor die placement accuracy and/or delamination at the interface of the build-up layer and carrier, remains a major challenge. In this study, the interactions among laser release layer, glass carrier, and build-up layer were evaluated for optimization of redistribution layer (RDL)–first FOWLP as a foundation to move toward fine-line FOWLP.

In this study, a series of experiments incorporating glass carrier, laser release layer, and build-up layers were carried out to determine the optimal setup for RDL-first FOWLP. First, glass carriers (300 mm x 300 mm x 0.7 mm) with coefficients of thermal expansion of 3 and 8 ppm/°C were treated with 150-nm laser release layers. After deposition of 0.1 µm of sacrificial material on the glass carrier, 8-µm build-up layers were coated and patterned by lithography to electroplate Cu interconnections with a density of approximately 10% of the surface area. Subsequent to die attachment, molding compound was applied on top to form a 200-µm protective overcoat. The reconstituted wafer was then separated from the glass carrier through a laser ablation process using a 308-nm laser to complete the design of experiments (DOE).

An experiment to study the correlation of glass carrier, laser release layer, build-up layers, and molding compound in RDL-first FOWLP processes is discussed to address full process integration on 300-mm glass substrates. The combination of glass carrier, laser release layer, build-up layer, and molding compound will pave the way for realizing cost-effective RDL-first FOWLP on panel-size substrates.

Key words

RDL First, Fan Out, Laser Debonding, and Wafer-Level Packaging

I. Introduction

Forecasts and technology roadmaps from all prestigious conferences have indicated that future electronic appliances will be dominated by mobile, medical, wearable devices and the IoT[1], all of which have several requirements in common: high-speed communication, low power consumption, and multi-function operation. Thus, high I/O density and chip stacking become necessary. To accommodate increasing demand on I/O and chip stacking, 3-D IC stacking supported by through-silicon via (TSV) was first introduced [2], which was mostly adopted by hybrid bandwidth memory (HBM) but was rarely applied to other applications due to its high cost of ownership, risk to IC performance, and complexity of design. Subsequently, a 2.5-D IC packaging scheme was then proposed as the next version, with cost and performance closer to what industry needs [3], in which silicon or glass interposers with through-substrate vias were applied. However, the cost of ownership still could not meet industry's demand.

Hence, several new terms coined by industry leaders to address unresolved issues from 2.5-D/3-D IC packaging were introduced recently, such as embedded wafer-level BGA (eWLB) from Infineon [4], redistributed chip package (RCP) by Freescale [5], integrated fan-out wafer-level packaging by TSMC [6], silicon wafer integrated fan out by Amkor, and fan-out chip-last packaging by ASE [7]. Despite the various advantages claimed for each technology at conferences or in papers, two fundamental fabrication process flows are inherent: chip-first and RDL-first. More importantly, it becomes obvious that debonding material and technology are the key enablers to facilitate integration for both process flows.

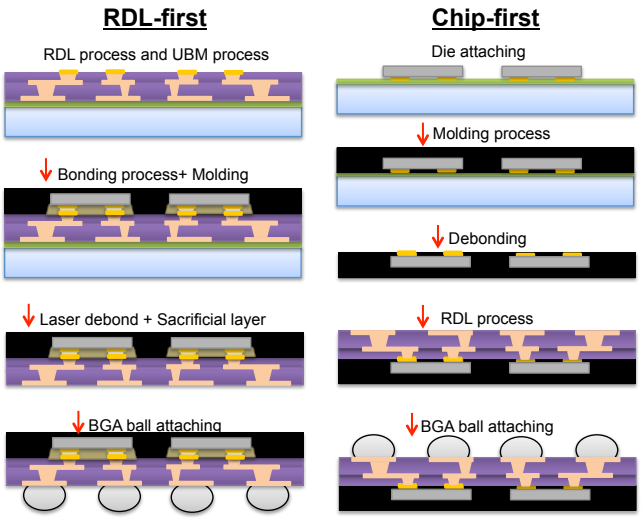


Figure 1. Chip-first and RDL-first flows

Chip-first starts with die assembly on an intermediate carrier followed by overmolding and debonding of the molded wafer from the carrier. The redistribution layers and bumps are subsequently applied on the molded wafer. As for the RDL-first approach, the redistribution layers are applied first on an intermediate. Following underfilling material and molding, the carrier is then separated from molded wafer before bump formation.

Because the chip-first approach was reported vigorously in the past few years, this study focuses on the RDL-first approach, which has the advantage of process simplicity, along with selection of laser release layer and dielectric material. In addition, an RDL-first approach, which allows dies to be placed on redistribution layers to improve yield loss, is an ideal flow for panel-level packaging.

By using the optimal laser release layer, build-up layers, and RDL-first process flow, cost-effective panel-level packaging can be realized in the future.

II. Experiment

A. *Material Properties*

The laser release layer is typically designed to easily decompose under laser radiation while still providing high thermal stability for backside processes. In this study, four laser release layers were evaluated to identify material properties that are reliable and applicable for RDL-first FOWLP processes. Generally speaking, the fan-out process includes multiple thermal cycles such as dielectric material curing, metal deposition, and molding compound curing. Thus, the laser release material must have a thermal decomposition (Td) temperature higher than 200ºC with the highest possible UV absorption.

Release layer	Td (°C)	Type	Transmittance at 308nm
A	545	Thermosetting	50%
B	539	Thermosetting	45%
C	<250	Thermosetting	80%
D	<250	Thermosetting	20%

Table 1. Characteristics of laser release layers

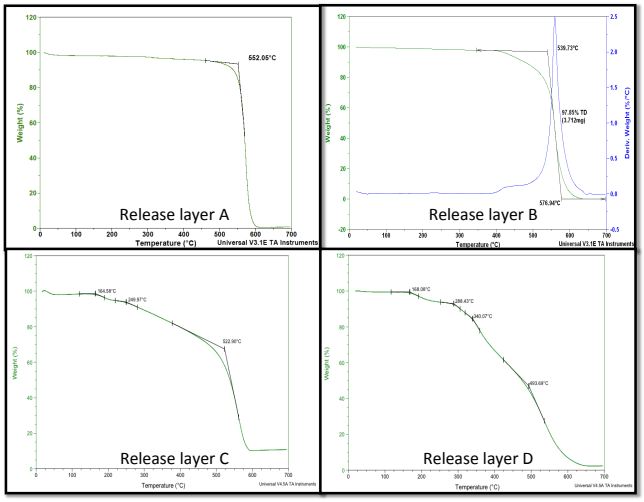


Figure 2. Thermo-gravimetric analysis of four release layers

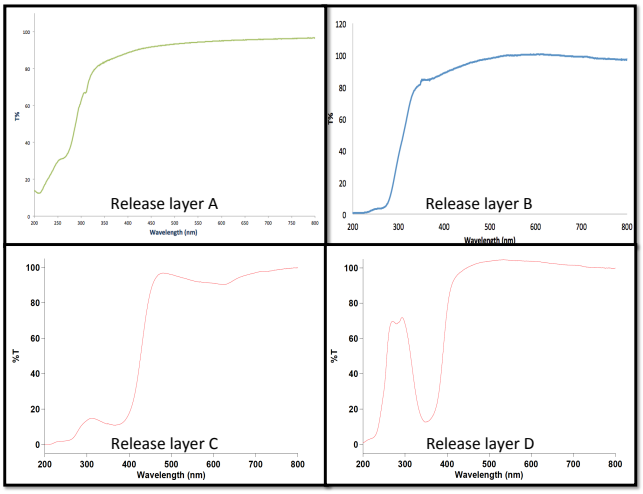


Figure 3. Transmittance of release layers

One important criterion for a reliable laser release layer is the ability to adhere well to the glass carrier and sacrificial layer applied on top for redistribution layer formation. Figure 4 shows an illustration of adhesion of a laser release layer to the sacrificial layer and glass carrier. Weak adhesion of the release layer is the root cause of delamination in subsequent backside processes when stress accumulates [8]. To obtain desirable adhesion, performance of the sacrificial layer used along with each of four release layers was evaluated by pull-off adhesion testing, as illustrated in Figure 5.

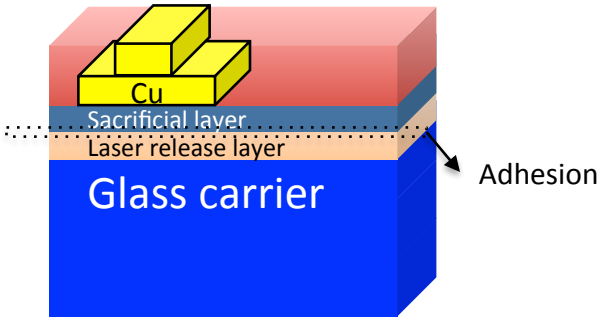


Figure 4. Illustration of adhesion interface

First, a glass carrier was treated with a laser release layer. After thermal curing, a sacrificial layer was then deposited for the subsequent pull-off adhesion test. This process was repeated to collect adhesion data for all four release layers.

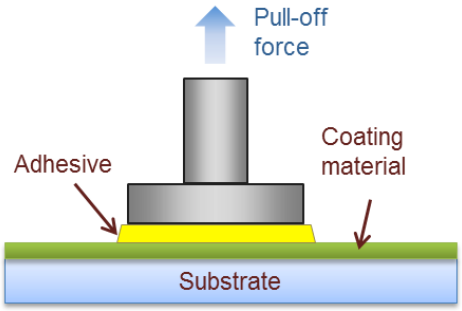


Figure 5. Illustration of pull-off test

The UV laser debonding process in this study is illustrated in Figure 6, showing the interface between the glass carrier and the sacrificial layer. A scanned laser beam travels through the glass carrier to reach the laser release layer, usually around 100 to 200 nm thick, to enable rapid decomposition. Whenever the release layer decomposes at the interface, adhesion at the area is minimized to allow the glass carrier to be easily lifted off the surface of the sacrificial layer.

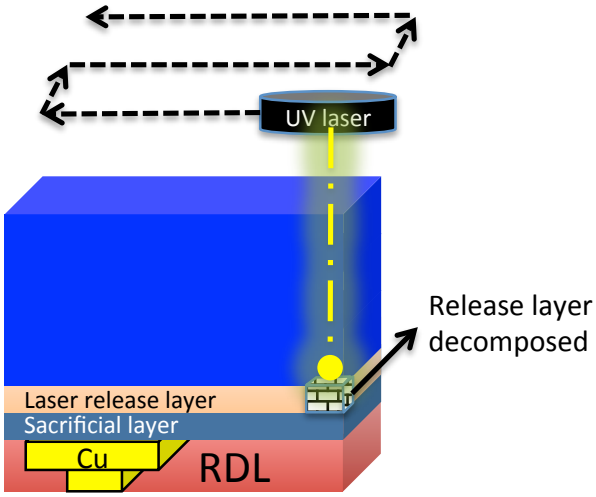


Figure 6. Mechanism of laser debonding by UV laser scanning

B. Test Vehicle and Experiment Design

To develop an RDL-first WLP process, a test vehicle design was divided into two portions, including a test chip and bottom glass carrier wafer. As shown in Figure 7, the test chip size was 9 mm x 9 mm with a thinned thickness of 150 µm. The electroplated copper pillar bumps on the chip were designed as a nearly full-array type, and 3000 I/O pads were within one chip. Copper pillar bumps had a bump size of 2 µm and were composed of 5 µm of Cu, 4 µm of Ni, and 5 µm of Sn. Bumps were distributed with a bump pitch of 100 µm.

A 300-mm glass wafer that was 700 µm thick was used as the carrier. An optimum laser release material was

chosen from the evaluated results of pull-off test. After coating the chosen laser release layer and sacrificial layer, the corresponding RDL pattern was fabricated onto the bottom glass carrier. As the test chips were stacked on the wafer, test patterns, including daisy chain and Kelvin structure, could be used to evaluate the electrical connectivity. Finally, the full wafer was molded with sheet mold material. Warp issues were also monitored. The experiments were executed to apply different glass wafers with coefficients of thermal expansion (CTEs) of 3 ppm/°C and 8 ppm/°C. The warp was measured after fabricating two layers of RDLs and and two layers of passivation and completion of the molding process.

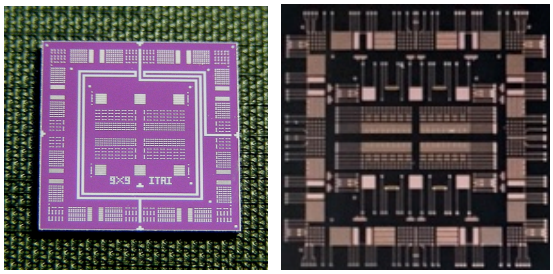
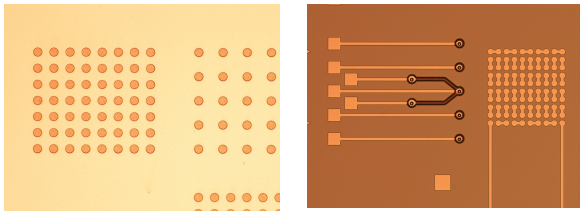


Figure 7. Test chip and corresponding RDL pattern on wafer

C. *Integration Process*

The process flow for manufacturing RDL-first fan out is similar to Figure 1. The structure was fabricated on a glass carrier. First, glass carriers (300 mm x 300 mm x 0.7 mm) with CTEs of 3 ppm/°C and 8 ppm/°C were treated with the laser release layers at a spin speed of 2,500 rpm, to achieve a 150-nm film. The release layer was fully cured to survive at high temperature up to 500°C after baking on a bake plate at 300°C for 5 minutes.

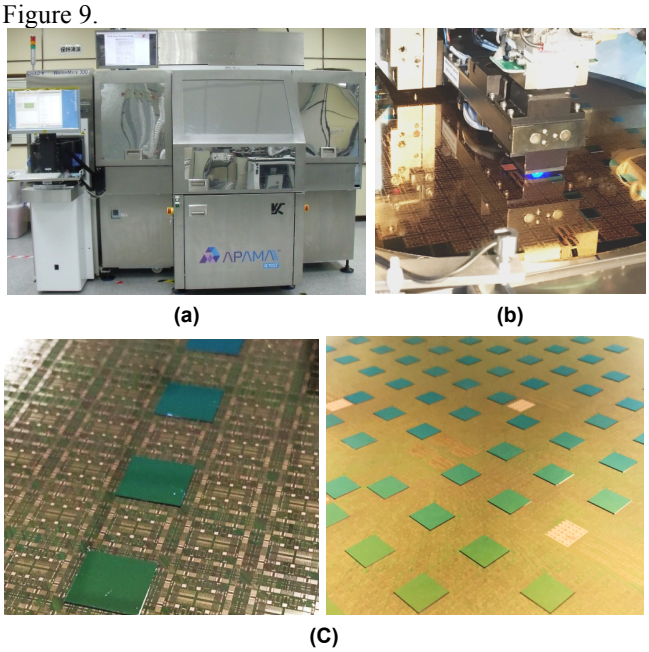
After subsequent sacrificial layer deposition, two layers of 3 µm RDL and 4 µm passivation were fabricated on the glass carrier to accomplish electrical interconnection. The two layers of RDL and passivation are shown in Figure 8.



(a) (b)

Figure 8. Optical images of RDL-first FOWLP fabrication: (a) the first RDL and passivation on glass carrier, and (b) the second RDL and passivation on glass carrier

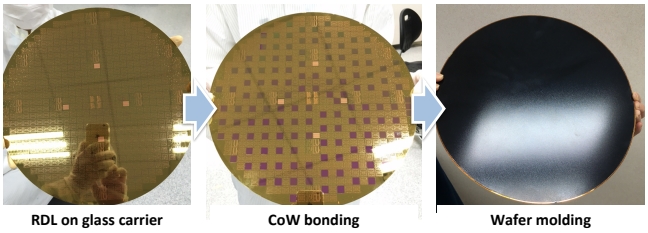
After wafer-level processing, the test chip was flip-chip bonded onto a wafer with adhesive using a K&S APAMA C2W bonder. Photos of the bonder and bonding process are shown in Figure 8. Sheet-type molding compound was applied in this WLP study. A sheet mold with thickness of 200 µm was laminated on the wafer surface at 130°C for 60 seconds by a Meiki laminator. After lamination, all the wafers were put in a high-temperature oven and post-mold curing was performed at 150°C for 8 hours. After curing, all the process evaluation was finished. Three photos of key steps, including wafer-level process, C2W assembly, and molding process, are shown in Figure 9.



(a) (b)

(C)

Figure 9. Images of chip-on-wafer (CoW) bonding: (a) CoW flip-chip bonder, (b) wafer on bonder stage, (c) chips on wafer



RDL on glass carrier CoW bonding Wafer molding

Figure 10. Images of three key steps of integration process

III. Results and Discussion

A. *Adhesion analysis*

The results of pull-off adhesion testing for the four release layers were normalized and are summarized in Table 2. All four release layers adhere sufficiently to the sacrificial layer needed to protect the passivation and RDL layers. Thus, thermal stability was used as criterion to

determine release for following laser debonding evaluation. Both release layers A and B, with T_d up to 500°C, were chosen to proceed for further evaluation.

Release layer	A	B	C	D
Pull-off adhesion	0.93	0.98	0.94	0.90

Table 2. Summary table of pull-off adhesion testing for the four release layers with the sacrificial layer

B. Laser debonding evaluation

The laser debonding testing was conducted by using a UV laser with a wavelength of 308 nm. During the laser irradiation, the high-energy laser pulses break bonds in the laser-sensitive release layer. Afterward, the laser-sensitive release layer−coated glass carrier is easily lifted off and removed from substrates with zero force. In this case, glass carriers coated with Material A and Material B release-layers were debonded with 200 mJ/cm^2 of laser energy and removed successfully from the substrate with zero force.

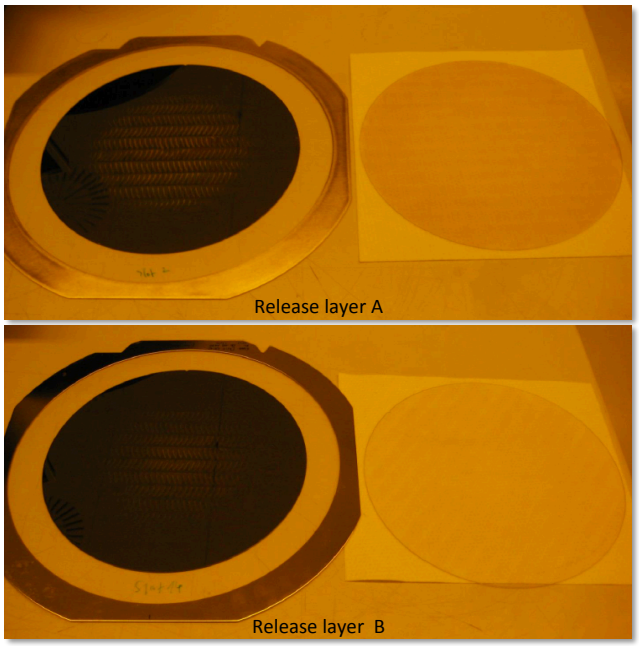


Figure 11. Images of laser debonding results

C. Process Integration (ITRI)

Three warpage situations were measured after two RDL and passivation layers were fabricated, and the molding compound process was performed. Table 1 summarized three warpage values as each step finished. Two types of glass carriers with different CTEs were compared. These results showed that the warpage of the 3-ppm/°C-CTE carrier is comparable with that of the 8-ppm/°C-CTE carrier after second RDL and passivation fabrication. However, the warpage of the 3-ppm/°C-CTE carrier increased rapidly after the molding process and post-mold curing. Figure 12 and Figure 13 show warp measurements of the carriers of both CTE types, 3 ppm/°C and 8 ppm/°C, were 4.5 mm and 0.75 mm, respectively. For this reason, the glass wafer with a CTE of 8 ppm/°C is suitable for further process development. We also checked the interface between the laser release layer and RDL passivation and did not find any delamination or physical warp forming. The laser release layer could hold a stable adhesive strength under warp form.

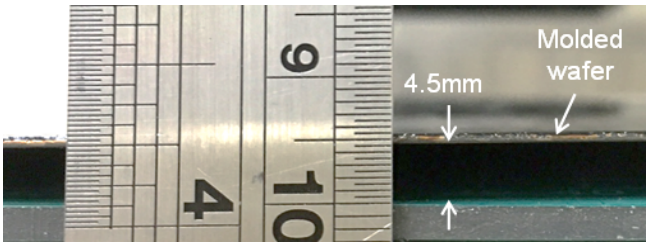


Figure 12. Warpage of molded wafer on glass carrier with CTE of 3 ppm/°C

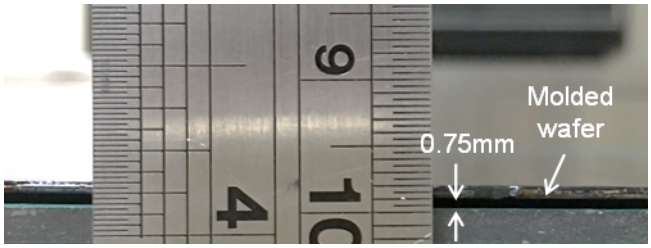


Figure 13: Warpage of molded wafer on glass carrier with CTE of 8 ppm/°C

Finished processes	CTE 3 ppm/°C	CTE 8 ppm/°C
1st RDL and passivation	350 µm	385 µm
2nd RDL and passivation	485 µm	507 µm
Molding/curing process	4500 µm	750 µm

Table 3. Warpage measurement results for each process

IV. Conclusion

A 300-mm glass carrier with CTE of 8 ppm/°C was found suitable for RDL-first FOWLP development in terms of better warp performance after the molding process and post-mold curing. As warp could be as large as 4500 µm, although there was no delamination found on release layer B, adhesion from layers underneath to chips in relation to reliability has become an important subject to study in the future.

Acknowledgments

The authors greatly appreciate the support of the ITRI 3-D IC team, SUSS MicroTec, and Corning Incorporated.

References

[1] Robin Taylor, David Baron and Daniel Schmidt, "The World in 2025-Predictions for the Next Ten Years," Electronics, "Progress in digital integrated electronics," *International Conference on Electronics Materials and Packaging (iMPACT 2015)*, pp.358-361. (2015)

[2] J. Keech, et al., "Fabrication of 3D-IC Interposers," *Proceedings of IEEE Electronic Components and Technology Conferenc*e (ECTC), Las Vegas, NV, May 28–31, 2013, pp. 1829–1833.

[3] M. Brunnbauer, E. Furgut, G. Beer and T. Meyer "Embedded wafer level ball grid array (eWLB)," *IEEE ECTC*, 2006, pp.1-5. (2006)

[4] Keser, et. al., "The Redistributed Chip Package: A Breakthrough for Advanced Packaging," *IEEE ECTC*, 2007, pp.286-291. (2005)

[5] Liu, C.C et. al "High-performance integrated fan-out wafer level packaging (InFO-WLP): Technology and system integration," *Electron Devices Meeting (IEDM), 2012 IEEE International* (2012)

[6] Scott C. et. al., "A Comparative study of a Fan-Out Packaging Product: Chip First and Chip Last," *Proceedings of IEEE Electronic Components and Technology Conference (ECTC*), Las Vegas, NV, May 31-Jun 3, 2016

[7] D. C. Hu, et al., "An Innovative Structure that Combines Interposer and Carrier," *Proceedings of IEEE Electronic Components and Technology Conferenc*e (ECTC), Las Vegas, NV, May 28–31, 2013, pp. 1332–1335

[8] Markus Woehrmann1, et. al "Characterization of Thin Polymer Films with the Focus on Lateral Stress and Mechanical Properties and their Relevance to Microelectronics," *Proceedings of IEEE Electronic Components and Technology Conference (ECTC)*, Orlando, FL, May 27-30, 2014