Challenges in 3D Inspection of Micro Bumps Used in 3D Packaging

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Abstract

2.5D/3D devices are the next major packaging technologies, driven by the need for more functionality, lower power consumption and smaller footprint. Many device manufacturers are devoting capital to develop their own processes and some are already shipping devices such as FPGA (Field Programmable Gate Array) on interposers. 3D packages often require hundreds of thousands of I/O per die. Micro Pillar bumps and C4 bumps are the main bump geometries used in 3D packages as their small pitch and size allow the required number of I/Os. Inspecting these bumps throughout the process is critical because failure after chip to chip or chip to wafer bonding is very costly. This paper describes the use of a camera and laser triangulation to provide complete 2D and 3D measurement and inspection capability.

Key words: 3D inspection, micro bumps, copper pillar bumps, laser triangulation

Introduction

Successful micro bump inspection and metrology must meet a number of challenging requirements. With micro bump diameters are already at 20µm and heights at 5µm (and both are headed for smaller) measurements require submicron precision to avoid excessively large guard bands resulting in unncessary yield losses. The sensor must also be able to handle finely pitched bump arrays where the space between bumps is typically about equal to the bump diameter. The inspection tool must accommodate a variety of bump materials, including copper, nickel, and various solder compositions. With manufacturers' road maps indicating more than 60 million bumps per wafer and more than hundreds of thousand bumps per die, the measurement system must be able to process and store large amounts of data quickly and effectively. Finally, the system must provide both two dimensional and three dimensional inspection capabilities while striking an acceptable balance between precision and throughput.

Solder bumps (C4) have been in use for some time in flip chip processes. More recently, many manufacturers are developing copper pillar bumps, which may or may not be surmounted by a solder cap. The use of pillar bumps is growing rapidly. They offer small pitch flexibility, higher I/O counts, better standoff, improved heat dissipation and compliance to lead free process. Pillar bumps with 40 micron pitch and 5 µm heights are currently in use, with 20 and 10µm pitch in development.

Microbump metrology requires measurements of height, coplanarity, position, diameter and volume (Figure 1). In addition, inspection capabilities must include the ability to detect bump defects, including missing bumps, bridged bumps, and misshapen bumps.

Bump Metrology

1. Bump height
2. Coplanarity
3. Diameter
4. True position

Bump Defect

- Missing Bump
- Bridge between bumps
- Bump shape (Nodule, crater, etc.)

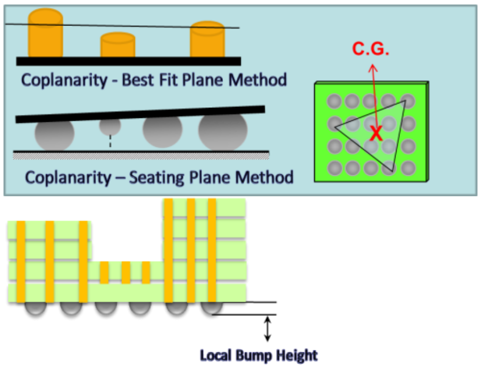

Figure 1 – Typical bump metrology requirements.

Laser Triangulation

The inspection system used in this study (Wafer Scanner™ 3880, Rudolph Technologies) uses laser triangulation for 3D measurements of bump height and coplanarity (figure 2). A laser, incident on the wafer surface at an angle of 45 degrees and focused to a spot size of 5 micron, scans a line over 1mm in length at a rate of 8 MHz on the wafer surface while the wafer is transported in a direction perpendicular to the scanned line. A lens collects the reflected/scattered laser light and focuses it on a position sensitive detector. Changes in the location of the collected light on the detector provide height dimensions with a resolution of less than 60nm. A range of resolution settings permits the user to select the optimal balance of throughput and resolution. The combination of high scanning rate and wide scan path permit 100% 3D scanning of bumps on a 300mm wafer in minutes, allowing 100% bump height inspection when needed.

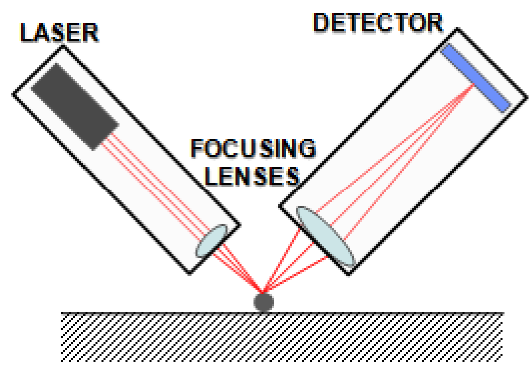

Figure 2 - Laser triangulation uses a finely focused laser and a position sensitive detector to measure bump height.

Because of the 45 degree incidence angle of the laser, the bump may shadow a portion of the wafer surface adjacent to the bump on the side opposite the laser, and the next bump may prevent reflected laser light from reaching the detector. The degree of shadowing depends on the shape and height of the bumps, but may well be enough to prevent the acquisition of any data points between tall, closely spaced bumps (Figure 3). However, relevant wafer surface data remain available for all bumps from areas to the side of the bumps (perpendicular to the direction of the laser) providing a valid basis for bump height calculations.

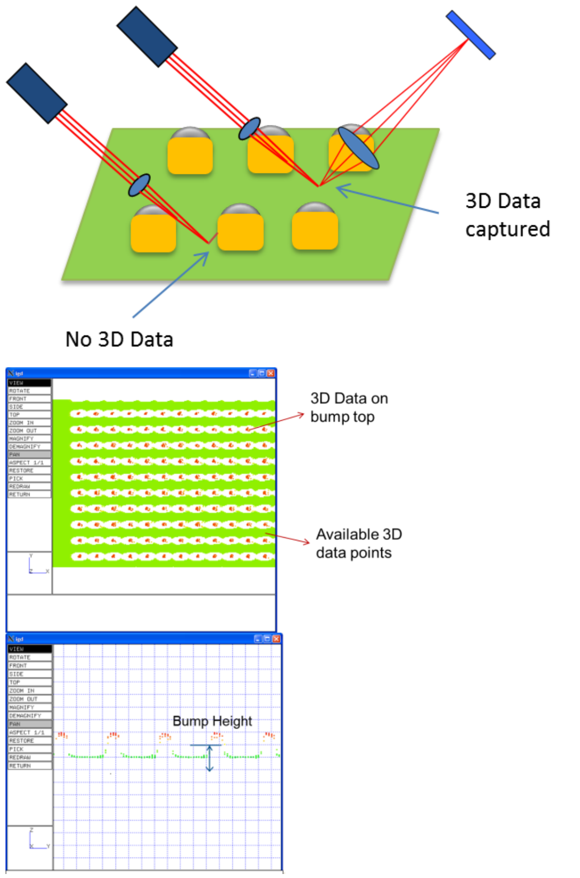

Figure 3 - Laser is able to collect 3D data points on the wafer surface even when pitch is very tight.

During operation the system scans the entire wafer surface in swath widths of over 1mm, simultaneously acquiring 3D data points from top of the bumps and the surrounding wafer surface. These 3D data points can then be used to provide local bump height measurement over the entire wafer allowing user to measure their variation across the wafer. Figure 4 is a color contour plot showing an example of the bump height variation across the wafer. The spacing of the data points can be varied to optimize efficiency on bumps of various sizes. The system can display 3D data points collected on individual bumps as well as calculating various bump, die and wafer level results. Using data from the top of the bump and the immediately adjacent wafer surface to calculate bump height improves the accuracy and repeatability of the measurements by eliminating the effect of wafer warpage. In addition, data from the tops of the bumps are used to calculate coplanarity with a variety of fitting models. Finally, data from the wafer surface provides information about wafer characteristics such as warpage (Figure 5).

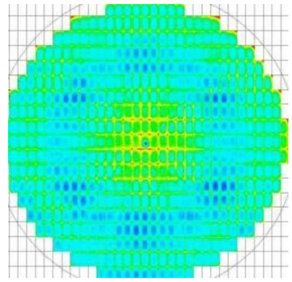

Figure 4 - Bump height variation across the wafer (dark blue indicates lowest bump height and yellow/red indicate higher bump height).

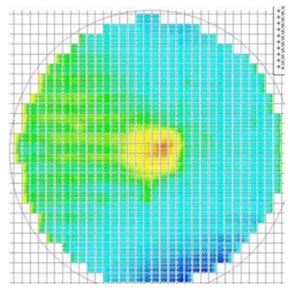

Figure 5 – Wafer warpage across the wafer using 3D data points from the wafer surface.

A unique staggered scan technique, shown in figure 6 further enhances the repeatability of bump height measurements. Staggering the scan increases the pitch in the direction of the line scan and reduces the pitch in the direction of the wafer movement, effectively spreading the data points more evenly over the wafer surface with no penalty in throughput. Staggered scanning can improve bump height repeatability significantly.

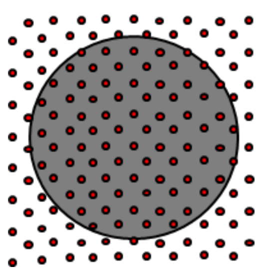

Figure 6 – Staggered 3D data points allow for maximum coverage improving measurement accuracy.

In the average bump height wafer map shown in figure 7, bump heights are averaged over each die. This map shows a definite trend of decreasing bump heights from the center toward the edge of the wafer, indicating a need for corrective action and, possibly, an opportunity for yield improvement. In addition to full wafer results, the system can display profiles of individual bumps (figure 8). Notice the multiplicity of data points from bump and the adjacent wafer surface, essential to ensure accurate, repeatable measurements.

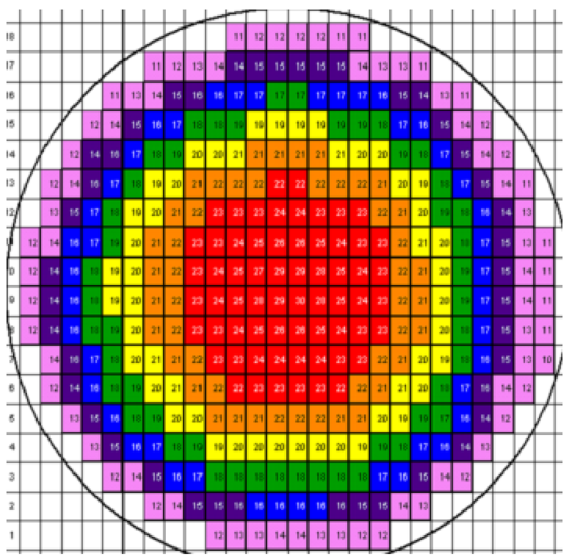

Figure 7 - A full wafer map of bump height averaged for each die shows a definite trend of decreasing bump height outward from the center of the wafer.

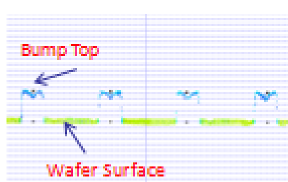

Figure 8 - Numerous data points acquired from the top of the bump and the surrounding wafer surface permit fast, precise measurements as well as reconstruction of 3D images of individual bumps.

The inspection system also includes a line scan camera for image-based 2D inspection and measurement. The 4K pixel camera provides fast clear images of defects. An automatic lens turret mounts multiple objectives with magnifications ranging from 1.25X to 20X. Both bright field and dark field illumination are available. 2D inspection can detect defects, such as the presence or absence of bumps, bridging between bumps, and misshapen bumps. 2D metrology can measure bump diameter and location.

Figure 9 shows bump diameter across the full wafer. In this color coded map, the yellow regions near the wafer edge indicate an increase in bump diameter. A damaged area of larger bumps is also apparent. Figure 10 shows defective bumps detected by the 2D inspection. Figure 11 demonstrates the system's ability to directly correlate individual defects to measurement data. In this example, the bump identified as defective in the 2D inspection also displayed excessive height in the 3D measurement. The user can zoom directly from the defect location indicated on the wafer map to a high resolution image of the defect.

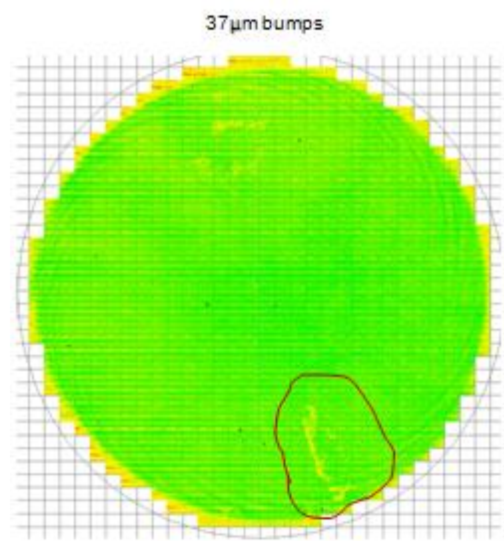

Figure 9 - 2D measurements, such as this one displaying average bump diameter for each die cross the full wafer, are performed in a separate scan using a line scan camera. This color coded map shows larger bumps near the wafer edge (yellow) and a damaged area of larger bumps (outlined in black).

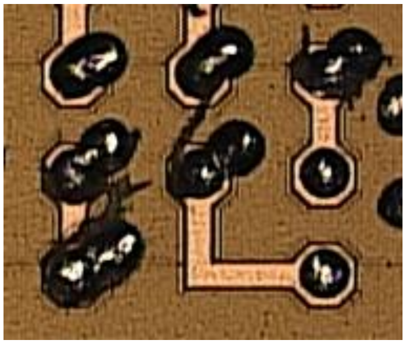

Figure 10 - Image-based inspection detects defects such as contamination, corrosion, and missing bumps, as well as ensuring that two dimensional characteristics, such as diameter and position, fall within specifications.

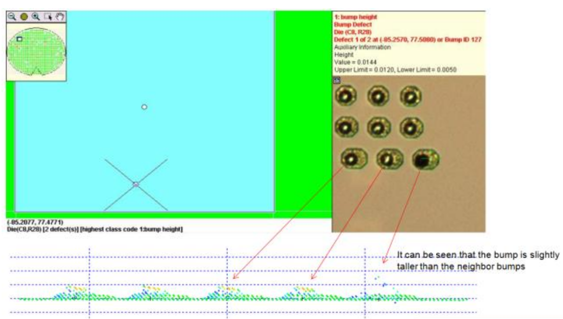

Figure 11 - From the wafer map the user can zoom in to examine individual defects and correlate the defect image directly with 2D and 3D measurements.

Application Studies

Micro Solder Bumps (C4)

This study used a 300mm wafer with bumps that were nominally 10 µm in diameter and 5 µm in height. There were more than 3.5 million bumps on the wafer. The wafer was evaluated for bump height and coplanarity, bump diameter, and bump and surface defects. Figure 12 shows wafer maps for bump height, bump diameter, die coplanarity, and wafer surface flatness. Figure 13 shows images of representative bump defects.

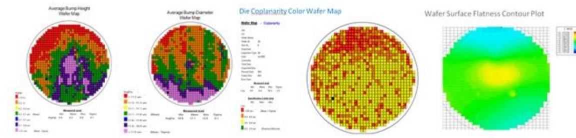

Figure 12 - Measured bump heights (left) ranged from 4.8µm to 5.8 µm and a trend to larger heights from center to edge is apparent Bump diameters .(center left)ranged from 10.6µm to 12.5 µm with a striping pattern left to right and a trend from higher to lower values from top to bottom. Die coplanarity (center right) ranged from 3.9µm to 18.3µm and also showed a trend to higher values at the top of the wafer. The substrate (right) was highest in the middle and lowest a top and bottom of the wafer.

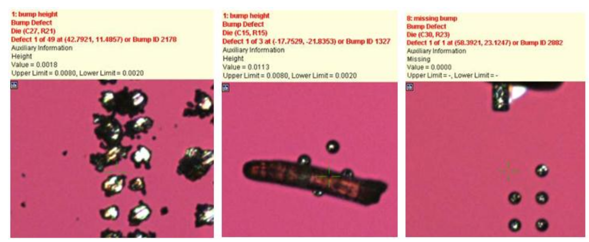

Figure 13 - Detected defects included (left) fragmented, misshapen, poorly formed bumps; (center) contaminating debris; and (right) missing bumps.

The precision of the bump height measurement was evaluated on 5 die with approximately 3000 bumps each, for a total of 15,000 bumps. Each bump was measured 10 times. The results demonstrated a repeatability of 0.3µm at 3σ. The 3D scan of the full wafer took 18.4 minutes, yielding a throughput, including handling, of just over 3 wafers per hour.

Micro Pillar Bumps

The second study also used a 300mm wafer. The bumps were copper pillar bumps with reflowed solder caps. They were nominally 20µm in diameter and height, with a pitch of 40 µm. There were approximately 65,000 bumps pre die. As figure 14 shows, bump heights were similar across the wafer but there was a distinct pattern within each die showing smaller bump heights near the center and greater heights near the ends.

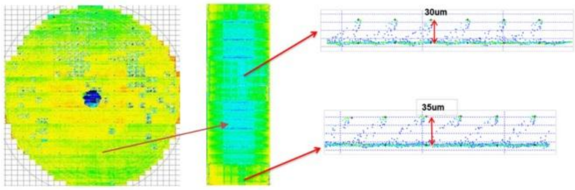

Figure 14 - Pillar bumps on this 300mm wafer appear to be similar across the wafer but show a consistent pattern within each die, taller at the ends than in the middle.

The precision of both 2D diameter measurements and 3D height measurements was evaluated on 5 die with 10,000 bumps each. Each bump was measured 10 times for a total of 500,000 measurements. Repeatability at 3σ was 0.91µm for the diameter measurements and 0.4µm for the height measurements.

Conclusion

Laser triangulation provides production-worthy 2D and 3D metrology and inspection capability for micro bump processes used in advanced 3D packaging applications. It delivers the submicron precision required for bumps with dimensions 20 µm and lower. Camera based 2D inspection is capable of detecting bump defects, and the high resolution images it generates facilitate fast, effective corrective action. The system used in these studies handled the large number of bumps and completed full wafer 3D scans in under twenty minutes.