A High Performance Full SiC Power Module Based On a Novel Stacked DBCs Hybrid Packaging Structure

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Abstract
This paper proposed a novel stacked DBCs hybrid package structure and designed a low inductive 1200V/120A SiC half-bridge power module based on the package structure. Using the multi-layer structure of DBC+DBC, the main loop parasitic inductance of the power module has been reduced to 1.8nH by optimizing the three-dimensional commutation loop and using the mutual inductance cancellation concept. The module was designed and fabricated, the low inductance characteristics of the module was verified by dual pulse testing and power testing. Dynamic test results show that the module can switch safely with a low overvoltage under zero ohm external drive resistance, and the switching loss is reduced by 57% compared to commercial modules.

Key words
SiC devices, stacked DBCs, parasitic inductance, hybrid packaging.

I. Introduction
One merit of Silicon Carbide (SiC) devices is the high switching speed, which allow SiC devices operating at high switching frequency with less switching loss. This feature makes SiC devices popular in high power density power electric applications [1]. Nevertheless, SiC devices' fast switching results in high slew rate in switching voltage (dv/dt) and current (di/dt), the higher di/dt will generate high voltage overshoot and ringing across the device, and the high dv/dt will generate cross-talk and EMI noise [2-3]. These issues will limit the benefits of SiC devices. Therefore, in order to take advantage of the high switching speed of SiC devices, the parasitic parameters should be careful treated in SiC power module design.

In order to reduce the parasitic inductance, some new 3D power loop packaging structures have been proposed, such as planar packaging structures [4], direct multilayer Direct Bonding Copper (DBC) structure [5] and hybrid packaging structures [6]-[7].

Planar package structures can reduce parasitic parameters and easily achieve better heat dissipation with double-sided cooling. However, these packaging structures have complex manufacture processes, lower reliability and the mutual inductance cancellation which are not easy to realize. Satoshi Tanimoto [5] presented a direct multilayer DBC structure, which uses a novel three-conductor double-ceramic layered substrate. The direct multilayer DBC structure makes current in two conductor layers with different direction and achieves mutual inductance cancellation. Finally, only 4.5 nH stray inductance (without power terminal inductance) is achieved. Since the structure adds another ceramic layer and another conductor layer, the thermal resistance will increase and the reliability of multilayer DBC will also be a problem.

Hybrid packaging structure can achieve a multi-layer 3D power loop structure with wire-bonding and stacked multi-substrates [6]-[7]. Due to the low cost of the PCB, the current hybrid package structures are mostly based on the DBC+PCB structure. However, due to the current limitation of PCB, making the DBC+PCB packaging structure unsuitable for high current power modules. Therefore, some high current power modules based on stacked DBCs packaging structure have been developed [8-9], which have high current capability and better thermal performance. But the parasitic inductance is still large.

Therefore, an improved stacked DBCs packaging structure with low thermal resistance and low power loop inductance will be proposed in this paper. The 3-D power loop of one HB-cell is optimized based on the stacked DBCs. In addition, a parallel multi-chip power module with symmetric current distribution is introduced. The power loop inductance of a 1200V/120A SiC HB power module has been reduced to 1.8nH by 3-D power loop design and the
mutual inductance cancellation design. The low power loop inductance of the module was verified by dynamic testing.

II. Design of the low inductive SiC power module

A. Design of the low inductive stacked DBCs packaging structure

The proposed stacked DBCs packaging structure concept is depicted as Fig. 1. This packaging structure consists of two DBC substrates, SiC devices, bonding wires, power terminals, and gate driver connectors. Two DBCs are stacked together by soldering to form a multi-layer structure. The SiC chips are embedded on the top of the bottom DBC through the windows of the top DBC. This chip placement structure can reduce the thermal resistance compared to top DBC placement, and the SiC chips are wire bonded to the top DBC. Moreover, the power terminals of the DC input is placed in the middle of the DBC to form the laminated structure.

As the dotted line of the current communication loop (CCL) shown in Fig. 1, this structure design has small power loop length with mutual inductance cancellation, which could achieve ultra-low parasitic inductance. The current flows from DC+ terminal through the vias1 of the top DBC to the bottom, and then the current flows to the drain pad of Q1. Afterward, the current flows through the MOSFET to the top source pad and back to the top copper layer of the top DBC through the bonding wires. After that, the current flows from vias2 to the bottom, and then the current flows to the cathode pad of D2. Finally, the current flows back to the DC- through the bonding wires on the anode pad of D2. It can be seen that the power loop current directions on top layer and bottom layer are parallel and opposite, which can produce a mutual inductance cancellation effect. Moreover, the bonding wires are oriented to power terminals which can shorten the loop length. The smallest communication loop area and the mutual inductance cancellation design can significantly reduce the parasitic inductance.

B. Design of the power module

Based on the proposed stacked DBCs packaging structure, a 1200V/120A full SiC half-bridge (HB) power module is designed as shown in Fig. 2. The HB module has six paralleled Cree’s CPM2-1200-0080B (1200V/24A@100°C) SiC MOSFET bare die and three paralleled Cree’s CPW4-1200-S020B (1200V/20A) SiC Schottky diode bare die for both high side and low side switch. The power module is divided into three identical sub-modules. This method can effectively reduce the warpage of DBC, thus increase thermal reliability. Besides, it also increase the fabrication yield.

One of the sub-modules is depicted as shown in Fig. 3(a) and (b). Two paralleled 1kV/20nF MLCC decoupling capacitors are integrated into the sub-module. Furthermore, the drive connection of SiC MOSFETs are Kelvin connection, and the power loop and drive loop are vertical to each other. Therefore, nearly zero common source inductance can be realized [10]. The MOSFETs are symmetrically distributed on the DBC to obtain the symmetrical current sharing for multi-chip paralleling. DC+ and DC- terminals are soldered in the middle of the DBC and are designed in the laminated structure to minimize the parasitic inductance. The power loop is designed into opposite current between the two layers, which forms a negative mutual inductance, thus, reduces the commutation loop inductance. Furthermore, the parasitic inductance of the proposed power module in Fig. 2 is extracted in Ansys Q3D, and the power loop parasitic inductance is only 1.8 nH, and the parasitic inductance of the power terminals is only 1.7nH, which is relatively small compared to the state-of-art 15 nH Wolfspeed 62mm 1200V/120A CAS120M12BM2 power module [11] and 15.8 nH modified 1200V/120A power module [12].
Fig. 3. Structure of the sub-module. (a) Top view of the sub-module, (b) side view of the sub-module.

III. POWER MODULE FABRICATION AND INTEGRATION

A. Fabrication of the sub-module

Considering the cost, the traditional Al bonding wires are used to verify the proposed packaging structure. Fig. 4 shows the fabrication processes of one sub-module. Firstly, vias are cut by laser cutting machine. DBCs are etched into designed pattern and electroplated. Then the Sn96.5Ag3Cu0.5 solder is screen printed to the top DBC and the bottom DBC. The top DBC is placed on the bottom DBC. The decoupling capacitors are placed on the top DBC, and the SiC chips are placed in the cavities. Next, the decoupling capacitors, DBCs, and SiC chips are attached together using a vacuum-reflow soldering process with a pre-designed fixture. After that, Al bonding wires are bonded to chips by an ultrasonic bonding machine. Finally, the power terminals and gate drive connectors are soldered to the top DBC during the secondary vacuum-reflow soldering with Sn37Pb63 solder paste.

B. Assembly of the integrated power module

Fig. 5 is the assembly process of the full module. After screen solder pasting on the copper baseplate with Ni plating, three sub-modules are soldered on the baseplate by vacuum-reflow. Then the module is housed with a polyphenylene sulfite (PPS) case and encapsulated with Qgel 310 epoxy resin as shown in Fig. 5(a), (b), and (c). After that, two gate drive boards are mounted on top of the HB module. Finally, the DC-link PCB with 45×2.2μF capacitor is mounted on top of gate drive board and the module. The high power density integrated HB SiC power module can be obtained as shown in Fig. 5(e). The dimensions of the integrated power module are 93.5mm×92.4mm×24.1mm (0.208L).

IV. Experimental Results

A. Static Characteristics

The static characteristics of the processed power module are measured by a Keysight B1505A power device analyzer at the room temperature of 25ºC. Fig. 6 presents the measured results. Fig. 6(a) depicts the output characteristics, the \( I_{DS}-V_{DS} \) curve at the different values of \( V_{GS} \). Fig. 6(b) shows the transfer characteristic curve. As shown in the test results, the static characteristics of the proposed module are similar to the commercial module. The little difference is caused by the chips’ characteristics and the test connector.

B. Dynamic Characteristics

In order to fairly compare the dynamic characterizations of the stacked DBC based hybrid structure SiC power module with the commercial SiC power module (CAS120M12BM2), the same double pulse test boards are designed for them as shown in Fig. 7. In order to exactly measure the \( V_{ds} \) waveform and the switching loss, several groups of decoupling capacitors are added in the DPT setup. The power loops of the test board are designed as same as possible and the gate driver board are identical. The waveforms are measured by Lecroy HDO4054 oscilloscope with 1GHz bandwidth. The drain source current is measured by the shunt resistor SSDN-10 (0.1Ω and 2GHz bandwidth) from T&M research. The gate source and drain source voltage are measured by Lecroy PP011 (500MHz bandwidth).
passive probe with low ground lead inductance probe tip and BNC connector. It should be noted the $V_{ds}$ of the commercial module is measured at the terminals. The measured $V_{ds}$ will be smaller than the actual MOSFET drain source voltage due to about half of the power module inductance in the voltage measuring loop [12]. The $V_{ds}$ of the proposed module is also measured at the terminals, but the terminal inductance is small, so the measured $V_{ds}$ will be close to the actual MOSFET drain source voltage.

![Fig. 7. Double pulse test PCBs for two modules: (a) tester PCB for the proposed module, and (b) tester PCB for CAS120M12BM2 module from CREE.](image)

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Fig. 8 are the experimental comparison circuits of parasitic inductance influence for voltage overshoot of commercial power module and proposed power module. Because the power supply connection wire and the PCB copper trace from $C_{ds}$ to $C_{dec1}$ introduced the parasitic inductance $L_2$ and $L_{ds}+L_{s1}$, there are large $C_{ds}$ and $C_{dec1}$ decoupling capacitors to eliminate the influence of these parasitic inductance.

The layout of the test board is carefully designed, however, about 8nH $L_s$ will be introduced by the current shunt. Because the current shunt must be installed outside the power module outline, there will be long copper trace to connect the power terminal and the current shunt. Compared to the 3.5nH $L_{dec1}+L_{module}$ of the proposed module, the 8nH inductance cannot be neglected. Otherwise, the voltage overshoot will be mainly caused by $L_s$. Therefore, an additional group of decoupling capacitors $C_{dec2}$ (9×2.2μF) are inserted between the current shunt and power module to eliminate the overshoot affected by $L_s$ for $V_{ds}$ measurement, as shown in Fig. 7. Meanwhile, the proposed power module has been tested under both 120nF $C_{dec}$ integrated inside the power module and not integrated.

![Fig. 8. Experimental comparison circuits of parasitic inductance influence for voltage overshoot of commercial power module and proposed power module: (a) adding $C_{dec2}$ for commercial power module, (b) adding a large $C_{dec2}$ for proposed power module without $C_{dec}$, (c) adding $C_{dec2}$ with $C_{dec}$.](image)

Fig. 8. Experimental comparison circuits of parasitic inductance influence for voltage overshoot of commercial power module and proposed power module: (a) adding $C_{dec2}$ for commercial power module, (b) adding a large $C_{dec2}$ for proposed power module without $C_{dec}$, (c) adding $C_{dec2}$ with $C_{dec}$.

Fig. 9 shows the turn-off waveforms of commercial power module and stacked DBC based power module. The load current is measured instead of the shunt current because of the existence of $C_{dec2}$. It should be noted that due to the asymmetrical gate loop, each SiC MOSFET in the commercial module has integrated 10Ω gate resistors. Otherwise, the power module will not operate normally [13]. The commercial power module used 1.1Ω turn-on gate resistance and 0.55Ω turn-off gate resistance respectively. In order to keep the same drive resistance, the external turn-on and turn-off gate resistor of the proposed power module are selected as 1.1 Ω and 0.55 Ω respectively. As shown in Fig. 9(a), the voltage spike of the commercial power module is 499 V at turn-off. As mentioned previously that the $V_{ds}$ of the commercial module is measured at the terminals and about half of the power module inductance influence is in the measuring loop, the actual $V_{ds}$ voltage spike will be 558V as predicted by the simulation results shown in Fig. 10. As the measured waveforms shown in Fig. 9(b) and (c), the stacked DBC based power module is only 435V (actual voltage is 453V) and the voltage spike is reduced to 428V (actual voltage is 442V) with integrated decoupling capacitors $C_{dec}$. The overvoltage reduced by 73% compared with the commercial module. Moreover, the parasitic inductance can be calculated according to oscillation frequency as the following equation:

$$f = \frac{1}{2\pi \sqrt{L \cdot C_{oss}}} \quad (1)$$

Where $f$ is the $V_{ds}$ overvoltage resonant frequency and $C_{oss}$ is the output capacitor of the power module. $C_{oss}$ of the commercial module is 1010pF reading from the C-V curve at 400V of the datasheet. $C_{oss}$ of the stacked DBC module is 859pF, which forms by six MOSFET (6×95pF from bare die datasheet C-V curve) paralleled, three SBD (3×93pF from...
bare die datasheet C-V curve) paralleled and the parasitic capacitance introduced by overlap of Output layer and –DC layer of DBC (10pF from simulation). Although the overvoltage of the commercial module is not actual, the oscillation frequency is the same as actual and can be used to calculate the inductance. The parasitic inductance of the commercial module is estimated as 16.7 nH at 38.8MHz oscillation as shown in Fig. 9(a). \(L_{\text{module}}+L_{\text{dec}}\) of the stacked DBC based module is calculated as 4.9 nH at 77MHz oscillation as shown in Fig. 9(b). Moreover, \(L_{\text{module}}\) of the stacked DBC based module can be obtained as 2.4 nH at 109.6 MHz oscillation as shown in Fig. 15(c). It can be seen that the test circuit induced only around 0.6 nH inductance for the module terminal connections. Additionally, Fig. 10 indicates the proposed power module has lower \(V_{\text{ds}}\) overshoot than the commercial module under different turn-off current.

Fig. 11. Experimental comparison circuits of switching losses for commercial power module and proposed power module: (a) without \(\text{C}_{\text{dec}2}\) for commercial power module, (b) without \(\text{C}_{\text{dec}2}\) and \(\text{C}_{\text{dec}}\) for proposed power module.

Fig. 12. Switching waveforms of commercial module and stacked DBC based module under zero external gate resistor and 400V/120A condition: (a) turn-off waveforms of commercial module, (b) turn-on waveforms of commercial module, (c) turn-off waveforms of proposed module without \(\text{C}_{\text{dec}}\), (d) turn-on waveforms of proposed module without \(\text{C}_{\text{dec}}\), (e) turn-off waveforms of proposed module with \(\text{C}_{\text{dec}}\), (f) turn-on waveforms of proposed module with \(\text{C}_{\text{dec}}\).

Fig. 13. The voltage overshoot and switching energy comparison results under different current: (a) voltage overshoot curve, (b) switching energy curve.

Moreover, the switching loss comparison of the commercial module and the stacked DBC based module are measured with zero external gate resistor at 400V/120A. The test circuit is shown in Fig. 11. In order to accurately measure the drain source current, the decoupling capacitors \(\text{C}_{\text{dec}2}\) and \(\text{C}_{\text{dec}}\) are removed. The current shunt resistor (SSDN-10) from T&M research is used to measure the drain current. Fig. 12 presents the switching waveforms of these two modules at 400V/120A condition. Fig. 13 shows the voltage overshoot and switching energy comparison results under without \(\text{C}_{\text{dec}}\) condition. It can be seen that the switching speed of the proposed power module is 2.1 times faster than commercial module, and the switching loss reduce about 57% as shown in Fig. 13(b). After adding the \(\text{C}_{\text{dec}}\), the voltage spike of \(V_{\text{ds}}\) reduces to 479V as shown in Fig. 12 (c) and (d). The \(dv/dt\) just changes a little for adding the decoupling capacitor.

V. Conclusion

A low inductive and low profile full SiC half bridge power module has been presented using the new hybrid packaging structure based on stacked DBC. The power loop parasitic inductance is 1.8 nH for a 1200V 120A power module by using the principle of mutual inductance cancellation and integrating the decoupling capacitors in the module. The gate driver, decoupling capacitors, heatsink, and DC-link capacitors has been integrated in the power module. Moreover, the power module can be easily fabricated based on the modular design and the wire-bonding technology. The static and dynamic characteristic tests are compared between the commercial and the proposed modules. The experimental results show that the overshoot voltage of the proposed power module with integrated decoupling capacitors has been reduced 73% compared to the commercial module under the same gate resistor. In addition, the proposed power module has 2.1 times higher switching speed and the switching loss can be reduced by about 57% compared to the commercial power module under zero external gate resistor.
References


