Manufacturing Readiness of BVA™ Technology for Fine-Pitch Package-on-Package

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Abstract

Ever increasing performance demands in a rapidly evolving smart phone market have led to a need for higher density interconnections linking memory components with logic devices in a standard package on package (PoP) configuration. While existing solutions present a technological roadblock at 350-400µm PoP pitch, new Bond Via Array (BVA™) technology provides a cost effective and scalable alternative that can achieve 240µm and below pitch values while utilizing conventional wirebond package assembly processes and tools. BVA is a high density, ultra-fine pitch package-on-package (PoP) interconnect solution that enables more than 1000 high aspect ratio connections between memory and processor components in a standard outline PoP. This increase significantly improves PoP capability and correspondingly provides increased bandwidth for the next generation of mobile devices. Here we discuss the 1020 IO BVA demonstration test vehicle, associated manufacturing process details, reliability performance and bi-level socket hardware developed to test these wire bond based novel interconnects. Furthermore the overall high volume manufacturing (HVM) readiness state of this technology for PoP applications will be described. The 1020 IO BVA prototype features 5 rows of vertical interconnects at 0.24mm pitch within an industry standard 14 x14mm package footprint. Although BVA interconnects were primarily developed for PoP packages, they offer many benefits over traditional vertical interconnects and can be implemented in a variety of other applications.

Key words

Bond Via Array, Package on Package, Stacking, Wide IO, High Bandwidth, Mobile

I. Introduction

In mobiles phones and tablets, the physical layout of the memory-processor subsystem has evolved to take on the form of a package-on-package. This configuration facilitates size and power reduction by stacking packaged memory directly on top of the logic component in conventional a surface-mount style operation. Furthermore this method permits continued supply chain flexibility as the memory and the logic packages are manufactured and tested separately. However, due to manufacturing constraints of existing PoP assembly solutions, only around 300 IOs between the base logic and top memory package are possible within a standard 14mm x14mm package footprint. Recent exceptions to this limit are high end smart phones that achieve approximately 450 PoP interconnects, but only through extreme thinning of device and package mold dimensions. These approaches do not address the fundamental issue of providing a cost-effective high-aspect ratio vertical interconnect that enables fine pitch PoP.

With a trend towards System-on-Chip (SoC) mobile processors with multi-core CPU, memory bandwidth requirements are sharply increasing. With 64-bit memory data for a 300 IO package, the bandwidth is limited to 25.6 GB/s at 1600 MHz DDR signal speeds. A wide IO memory industry standard recommends 512 memory data interconnects to quadruple the current bandwidths to >100 GB/s even at lower 800 MHz DDR signal speeds. For memory devices to offer 512 data lines though, a total of about 1000 interconnects are needed to include the accompanying address, control, power and ground signals required for operation. No current PoP technology can offer 1000 interconnects due to limited fine-pitch capability within the standard package outline. Through-Silicon-Via (TSV) technology continues to be developed as an ideal solution however TSV manufacturing is still being

developed to address several challenges relating to process, yield, reliability, thermal performance, and supply chain. These factors affect overall cost of TSV technology and need to be resolved before it is considered for widespread industry adoption.

Bond-Via-Array (BVA™) is a new PoP interconnect technology that provides this high-bandwidth interconnect capability today [1]-[3]. Instead of conventional solder balls or through mold via (TMV) interconnects at the periphery, this technology uses free standing wire bonds to connect base and top packages. This paper details the equipment and process development engineering results related to HVM readiness of BVA technology along with design optimization, critical assembly process steps, reliability performance and testing.

II. Bond Via Array PoP

BVA is developed as a cost effective and scalable advanced PoP solution that is able to provide a very high density of interconnects between the bottom processor and the top memory package. Since these are wire bond based interconnects, very tall interconnections can be achieved at ultra-fine pitch that well exceeds capabilities of existing solder-based PoP interconnect technology. Multiple rows of free-standing vertical wire-bonds at 240µm pitch are formed along the periphery of the processor package. The package is then molded such that the wire tips are exposed above the encapsulation material, which are then attached to the BGA solder balls at the bottom of the memory package. Figure 1 depicts the cross section of a typical BVA PoP package.

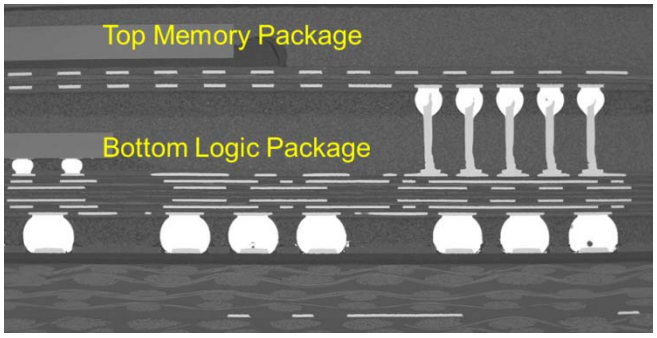

Figure 1. SEM micrograph of BVA PoP

The technology was introduced with a 432 IO BVA prototype build; its details along with the reliability data has already been published [2], [3]. This early stage proof-of-concept prototype build had an array of free standing wire bonds achieved by forming the stitch bond at the logic substrate. In the subsequent 1020 IO test vehicle reported in this work, the modified wire bonding process forms a conventional ball bond at the substrate to achieve a high aspect ratio vertical interconnect.

Unlike with developing technologies such as TSV, BVA enables the manufacturing of these ultra-fine pitch interconnections without the need for new assembly equipment or materials. This advantage is realized by fully leveraging the well-established wire bonding assembly infrastructure. Wire bond pitches below 100µm are easily achievable today on polymer substrates and hence BVA technology provides a solution that would be viable for the next few generations of finer pitch PoP interconnects. This technology can achieve interconnects as short as 200µm and as tall as at least 750µm. Apart from varying heights, experiments to evaluate wires thinner than 50µm diameter are also ongoing.

III. Design Optimization

Package design optimization was performed with comprehensive finite element analysis (FEA) modeling of package structure and construction materials. Stepwise FEA simulations were created to represent each assembly process step for memory and logic builds. This includes flip chip, underfill, molding and solder ball attach for logic package. Accurate material property datasets as a function of temperature were generated (e.g. modulus vs temperature curves) to obtain a more accurate representation of the prototype. The materials and structural design were selected to achieve package warpage within a maximum of 100µm, and minimize the differential warpage between the memory and the logic package. Over-mold compound was identified as one of the most critical materials affecting package warpage and so a wide range of options were analyzed. Although both the processor and memory packages warp in the same direction with increase in temperature, the room temperature warpage increases for thinner mold gap and thinner die; hence managing package warpage for thinner package is extremely challenging [4].

Table 1. Structural iterations within the FEA design of experiment matrix for the 1020IO logic package

Option	Mold Compound	Mold Gap (um)	Die Thickness (um)	Mold Cap (um)	Core Material	Core Thickness (um)	Warpage at 25C	Warpage at 217C
1	A	400	125	575	Sub-A	40	139	-26
2	A	261	125	436	Sub-A	40	114	-23
3	A	160	125	335	Sub-A	40	99	-17
4	G	160	125	335	Sub-A	40	116	-85
5	G	100	125	275	Sub-A	40	98	-84
6	G	50	125	225	Sub-A	40	74	-81
7	G	80	125	225	Sub-A	80	68	-88
8	G	50	125	225	Sub-A	120	62	-94
9	G	80	125	225	LCTE	40	83	-80
10	G	20	125	195	Sub-A	40	73	-76
11	G	50	125	225	LCTE	120	72	28
12	H	100	125	275	Sub-A	80	93	-74
13	I	100	125	275	Sub-A	60	94	N.A.
14	G	100	125	275	Sub-A	80	91	-77
15	G	120	125	295	Sub-A	60	98	-77
16	H	100	100	250	Sub-A	80	107	-77
17	H	150	100	300	Sub-A	60	132	-95
18	H	100	150	250	Sub-A	80	91	-88
19	H	80	150	280	Sub-A	60	89	-85
20	H	100	100	250	LCTE	60	118	-47
21	H	150	100	300	LCTE	60	140	-48
22	H	80	150	280	LCTE	60	98	-55
23	H	100	150	300	LCTE	80	90	-95

For the logic package, 2 different core materials were analyzed including standard Sub-A and LCTE substrate with a Low Coefficient of Thermal Expansion. As shown in Table 1, a total of 23 different combinations of various parameters including die, substrate core and mold gap thicknesses as well as substrate core, underfill and mold compound materials were analyzed. It was found that the overall package warpage decreases for thicker substrate core. Moreover, the warpage at both room and reflow temperatures decreases as the mold gap above the die is reduced.

Option 23 turned out to be the most promising design which provided a warpage below 100µm. This profile meets the original criteria of <1.3mm total stack height and individual warpage ≤100µm at both room and reflow temperatures. The differential warpage between the memory and the logic was then analyzed to expose any potential assembly yield issues. For option 23, the warpage in the memory and logic at room temperature and reflow temperature is shown in Table 2 for comparison.

Table 2: FEA predicted warpage values for the 1020 I/O logic (2 core options) and overlying memory package.

Package	25ºC (µm)	217 ºC (µm)
Memory	90	-37
Logic (Sub-A)	83	-85
Logic (L-CTE)	90	-55

Table 2 shows that memory and logic packages display similar warpage characteristics. The differential warpage between the memory and the logic with a low CTE substrate is 0µm and 18µm at 25ºC and 217ºC, respectively and it is predicted to be 7µm and 48µm at 25ºC and 217ºC, respectively with a standard substrate.

IV. Test Vehicle

An optimized 1020 IO daisy chain test vehicle design was finalized based on the FEA modeling results for a standard 14mm x 14mm package footprint. Table 3 shows the brief dimensional details of this test vehicle.

Table 3. Summary of 1020 IO BVA PoP Package

Package foot print	14mm x 14mm
Package Thickness	1.25mm
Logic Package Thickness	0.74mm
Memory Package Thickness	0.51mm
Logic BGA Pitch	0.4mm x 0.4mm
Number of Logic IOs	916
PoP IO Pitch	0.24mm
Number of PoP IO rows	5
Number of PoP IOs	1020

As indicated in table 3, there are a total of 5 rows of bond via interconnects at 240µm pitch distributed around the periphery of a 200µm thick 7.5mm x 7.5mm logic flip-chip die. These bond-vias provide a total of 1020 connections between the bottom logic and top memory package. The topside of the logic substrate has flip-chip pads at the central region to attach to the logic die and wire-bond pads at the periphery for the vertical bonds. The bottom of the topside memory substrate provides a solder pad arrangement matching the peripheral bond via array of the logic package.

V. BVA Assembly Process

Figure 4 describes the major process steps required to assemble a BVA PoP package.

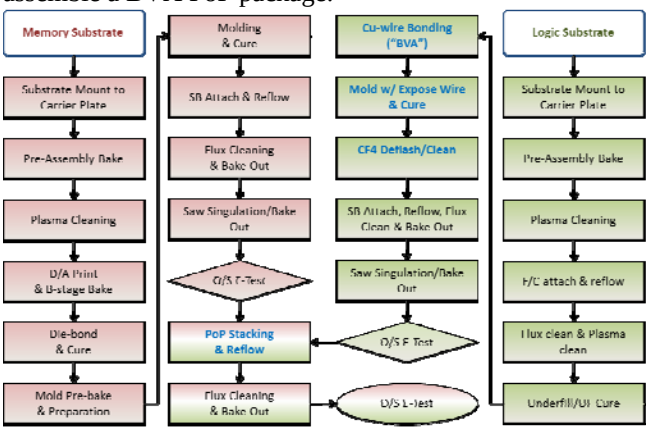

Figure 4. Process flow for BVA PoP

The BVA product does not need any changes to memory package assembly flow and introduces minimal changes to the logic package assembly and stacking process. Some of the key process steps for BVA include:

- Creating an array of free standing vertical wire bonds on the logic substrate
- Encapsulating the logic package while achieving the wire protrusions above the encapsulation mold compound
- Post-mold cleaning of the wire tips to facilitate uniform solder wetting around the wire and
- Package stacking

The logic die is first flip chip bonded to the substrate with a standard assembly process. The array of free standing wire bonds are then formed at the periphery of the substrate surrounding the flip-chip die (per Figure 5).

The vertical wire bond process utilizes 50µm diameter Pd coated Cu wires. Bonding was performed using a modified wirebond sequence developed in cooperation with Kulicke and Soffa (K&S) on the ICONN platform. The tool was used to verify High Volume Manufacturing (HVM) feasibility of this approach to forming high-density vertical connections for PoP. Extensive run trials in quantities over 500K consecutive wire bonds at <40ms cycle-time were successful. The supporting software for BVA wire bonding is also being developed by other wirebond vendors including Shinkawa and ASM.

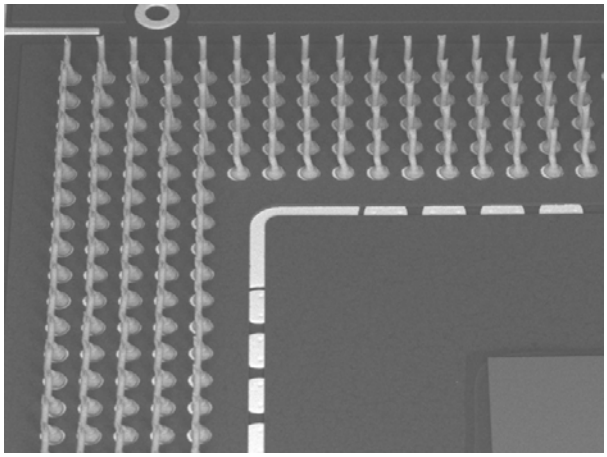

Figure 5. Five rows of vertical wire bonds at the periphery of the bottom processor package.

Alignment and stacking of the top memory package needs a high degree of XYZ positional accuracy of the BVA wire tips. To verify this aspect, wire tip positions were measured using View Micro-Metrology's Benchmark 450 tool, an automated optical monitoring systems. Measurements indicated XY positional accuracy of +/-10µm within pad center-point. Z height variation was less than +/-20µm for these 440µm tall wires.

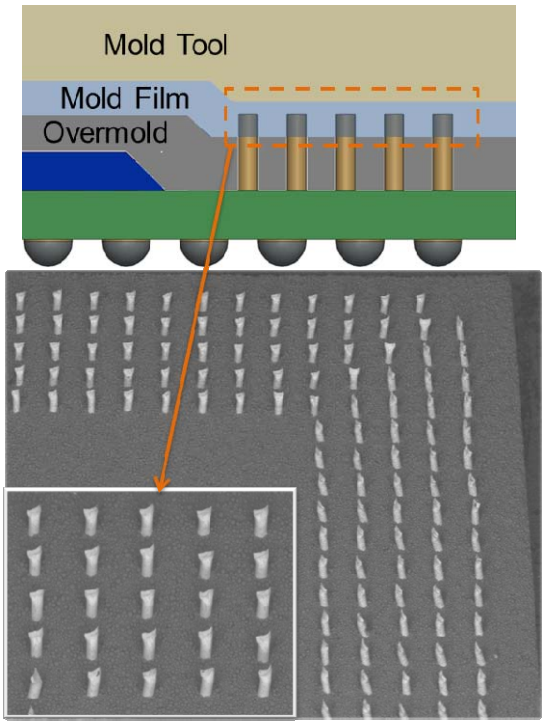

Figure 6. Fim assist molding for wire protrusions above the mold

The processor package is then molded using a standard film assist transfer molding process using APIC YAMADA tool. As the mold tool is clamped over the partially assembled logic package, the tips of the wires penetrate into a portion of the film on the top mold chase. The mold cavity is then filled via transfer mold process and the mold is cured. As the film acts as a barrier to mold flow only for these wire-tip regions, each end of the vertical wires inserted into the film is exposed above the mold as the cavity is released and the film is pulled away from the package. The resulting mold cap with wire protrusions is illustrated in Figure 6. The post-molding tip position was measured again and was within the required tolerance specification for stacking.

Although the film assist mold process enables exposure of wire-tip regions over the mold cap line, some amount of mold bleed occurs along wire-tip surfaces. This may adversely affects the quality of solder joint formed on top of the wire during the memory stacking process. Multiple mechanical and chemical methods were developed for this mold bleed removal including wet blast, chemical wet etch as well as plasma cleaning. CF_4/O_2 and Ar plasma based de-flash process was successfully implemented using Nordson March tool.

The package warpage is then measured by projection Moire interferometry using Insidix TDM tool, which is a compact topography and deformation measurement system. Figure 7 below describes the individually measured warpage data for memory as well as logic package. As indicated by FEA

simulations, both the packages warp in the same direction during the assembly reflow operation.

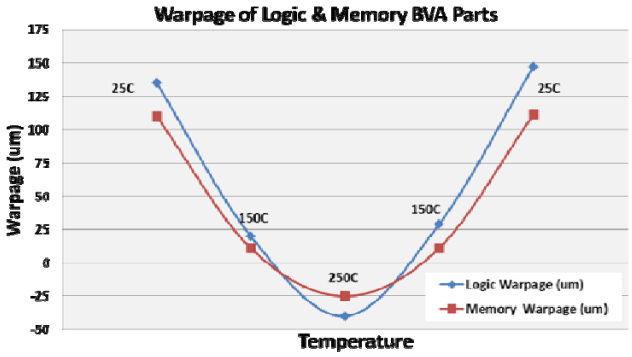

Figure 7. Warpage of memory and logic package using projection Moire interferometry

The memory package is then stacked on top of the bottom logic using a conventional SMT-style PoP assembly process. A high yielding and re-workable soldering process was developed to obtain uniform and consistent joints. Solder paste is first printed on PCB board, followed by pick and place of the logic package. The solder paste dipped memory is then stacked on top of the logic package and the entire assembly reflowed. Package stack SMT of the BVA prototype yielded uniform and consistent joints at fine pitch of 0.24mm as shown in Figure 8. SMT mounting was demonstrated at Universal Instruments Corporation.

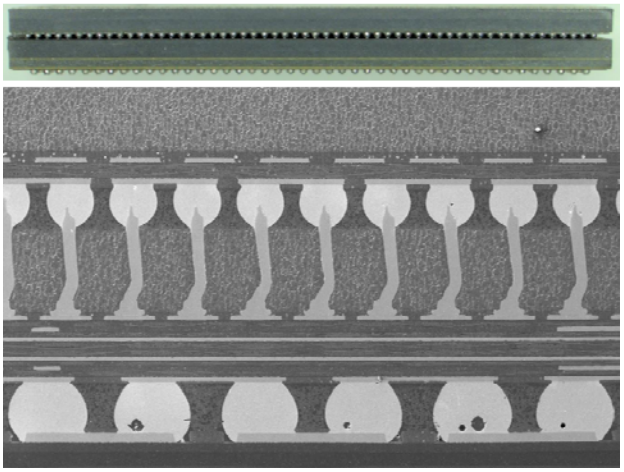

Figure 8. SEM cross-section: stacked BVA PoP package

VI. Bi-Level Test Socket

Testing this ultra-fine pitch logic component as well as the overall PoP stack introduces some challenges as the interconnect pitch exceeds current mainstream PoP design limits. To address this concern, a low-cost test socket hardware solution that accommodates 240µm pitch while remaining fully compatible with existing automated test equipment was developed in co-operation with Leeno and SemiQual. Drawing of the bi-level pin-based test socket demonstrated for BVA PoP testing is shown in in Figure 9.

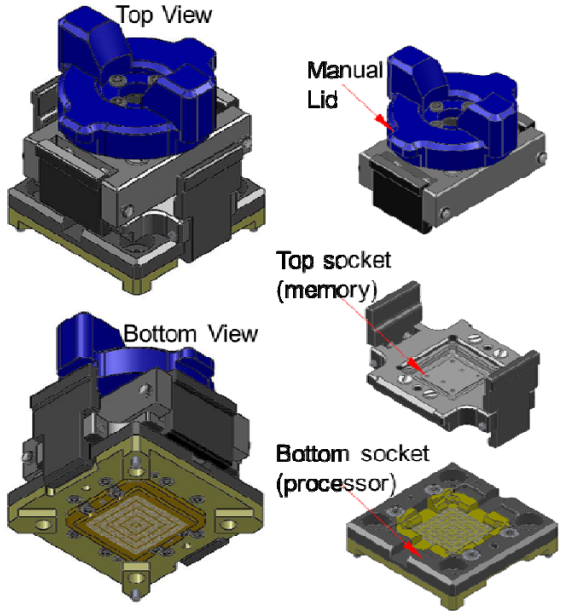

Figure 9. Test socket design

The top socket of this hardware holds the 0.24mm 1020BGA memory package. It connects the BGA of the memory device to the top of the exposed BVA wire tips of the underlying logic device. The bottom (base) socket is mounted to a test board which interfaces with a programmable open/short tester. The shape and size of the wire tips, their orientation, and relative position was measured with respect to the BGA grid reference outline for individual units. The measured positional tolerance fell was specifications and the alignment capability of the socket.

VII. Reliability Testing

The packages were subjected to a complete set of reliability tests including JEDEC level 3 moisture sensitivity, board level temperature cycling, high temperature storage and drop testing. The parts successfully completed all the reliability testing as summarized in Table 4.

Table 4. Reliability test and results of 1020 IO BVA PoP

Test	Standard	Test Condition	Sample Size
Moisture Sensitivity Level 3	IPC/JEDEC J-STD-020C	125°C for 24hrs; 30°C / 60%RH for 192 hrs, 3X Pb-free reflow	22
Temperature Cycling (Board Level)	JESD22-A104D Condition G	-40°C to 125°C, 1000 cycles	45

High Temperature Storage	JESD22-A103D Condition B	150°C, 1000 hrs	22
Drop Testing	JESD22-B111	>30drops, 1500G, 0.5mS of 1/2 sine pulse	20

All the parts passed board level temperature cycling without any issues. As depicted in Figure 10, well after 1000 cycles a small area of fatigue induced micro-cracks were eventually observed near the tip of the Cu wires located at the corner of the packages.

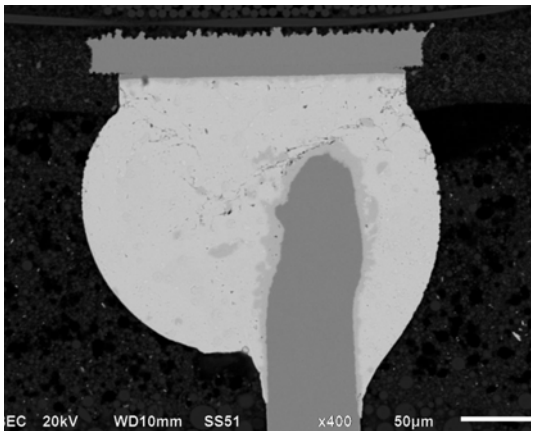

Figure 10. Micro-cracks developed at the wire tip after 2500 temperature cycles

It was reported earlier [1] that bare Cu wire is completely converted into Cu_6Sn_5 intermetallic compound (IMC) during reflow stacking process. Hence Pd coated Cu wires were instead used to achieve robust interconnects. Evaluating the high temperature testing performance for Pd-coated Cu wire was critical, especially near the wire tip area where Pd coating may have been partially removed. Although some degree of IMC is formed around the wire tips within the memory solder ball, Pd nonetheless provides an effective diffusion barrier thus creating a reliable interconnect in this regard.

Per Table 4, the original stack configuration providing underfill on both the BGA and BVA passed drop testing requirements. To further evaluate the drop testing performance of BVA interconnect itself, only the BGA portion of the bottom processor package was underfilled on-board leaving BVA interconnects to the memory without underfill reinforcement. In this case, underfill secures only the logic BGA, effectively moving the the stress to the BVA interconnects. Despite this stress, the package still displayed notably robust reliability performance in extended drop testing. The first failure was reported after 181 drops while multiple units survived 500 drops after which the test was terminated. Mean Time to Failure (MTTF) was calculated to be approximately 354 drops which is significantly improved over existing PoP technologies. All the failures occurred at the corner BVA interconnects of the failed packages. Cross sections indicated crack failures in corner BVA interconnects, while no BGA failures were observed on the underfilled bottom processor package. Figure 11 shows the cross section of the drop test failure after 299 drops.

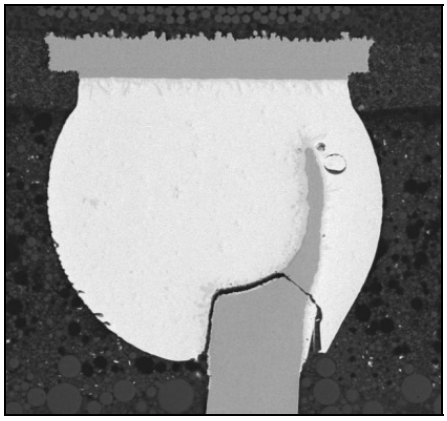

Figure 11. Cross-section of drop test samples after 299 drops

The crack initiated in the corner BVA bumps and propagated vertically along the Cu wire. Failure occurred as the crack moved across the thinner and weaker (IMC dominant) areas of the wire tip. This elongated the crack length required to cause a failure, thereby improving the interconnect reliability.

VIII. Conclusions

BVA PoP has been developed as a wire bond based interconnect technology that enables very high density vertical interconnects at low cost by utilizing existing infrastructure and assembly practices. A 1020 IO BVA PoP was successfully assembled at 0.24mm pitch and passed all standard reliability tests. High volume manufacturing feasibility studies covering various critical process steps were completed and verified with automated assembly and test equipment suppliers. At the time of writing paper, 2 independent contract assembly houses are working on building BVA capabilities and assembly lines. BVA interconnect technology was initially developed for PoP applications. However, this technology's process and structural flexibility along with robust reliability performance and cost advantage make them suitable for multiple other applications. We are working on developing new application areas utilizing BVA interconnects and the relevant updates are to be published soon.

Acknowledgment

The authors would like to acknowledge the contributions from the design, FEA, assembly and failure analysis team at

Invensas that helped develop BVA technology. Special thanks go to Roseann Alatorre, Scott McGrath, Grant Villavicentio, KM Bang, Michael Hyunh, Tami Harchysen and Gabe Guavara.

References

[1] P. Damberg, I. Mohammed, R. Co and E. Chau, "Fine Pitch copper PoP for Mobile Applications", *Proceedings of IEEE Electronic Components and Technology Conference (ECTC)*, San Diego, CA, June 2012, , pp. 1361.

[2] I. Mohammed, R. Zhang and R. Katkar, "3D Packaging for High Computing with WIDE IO Processor-Memory Interface", *Proceedings SMTA International*, Orlando, FL, 2012, pp.163.

[3] Z. Zhao, R. Katkar, R. Zhang, L. Mirkarimi and R. Co, "Bond Via Array – A New Ultra-Fine Pitch Package on Package Solution for High Bandwidth Mobile Applications", *Proceedings of Electronic System Technologies Conference (ESTC)*, Las Vegas, March 2013.

[4] L. Mirkarimi, R. Katkar, R. Zhang, R. Co and Z. Zhao, "A Non-Through Silicon Via 1000+ IO Package On Package Solution for Wide IO Applications", *Proceedings of 46th International Symposium on Microelectronics (IMAPS)*, Orlando, FL, October 2013, pp. 94.

[5] R. Katkar, R. Co and W. Zohni, "Manufacturing Readiness of BVA Technology for Ultra High Bandwidth Package on Package", *Proceedings of IEEE Electronics Components and Technology Conference (ECTC)*, Orlando, FL, 2014, pp. 1389.