A New Package for High Speed and High Density eStorage Using the Frequency Boosting Chip

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Abstract

A die-stacking technology in a multi-chip package can effectively increase the capacity. However, long wire bonding for multi-chip stack, inter-symbol interference caused by large capacitive loading and I/O speed degradations due to simultaneous switching noise (SSN) and power consumption have become obstacles to optimize the internal NAND flash interface. In this paper, to overcome the inevitable challenge between larger storage capacity and higher I/O speed, we propose a new package structure with a frequency boosting interface chip (FBI-chip) for high speed and high density eStorage.

Key words

High speed, eStorage, FBI (Frequency-Boosting-Interface), package structure

I. Introduction

In recent years, data rates to support high speed and multi-function mobile devices have significantly increased and mobile storage density per chip has increased as well with ever growing usage of high speed mobile systems. For these requirements, various eStorage products (eMMC[1], and UFS[2], etc) have been developed and the density of these products has been increased more and more. Thus, in order to implement a level of high density products required by recent mobile device markets, many memory chips as possible should be stacked within a package. Recently, as serial interfaces up to 600MB/s throughput has hindered the accelerating performance growth of mobile storages due to the host bandwidth limit. Therefore, the performance bottleneck of the eStorage product has moved from the host interface to the internal NAND flash interface.

A die-stacking technology in a multi-chip package can effectively increase the capacity. However, long wire bonding for multi-chip stack, inter-symbol interference caused by large capacitive loading and I/O speed degradations due to simultaneous switching noise (SSN) and power consumption have become obstacles to optimize the internal NAND flash interface. In this paper, to overcome the inevitable challenge between larger storage capacity and higher I/O speed, we propose a new package structure with a frequency boosting interface chip (FBI-chip) for high speed and high density eStorage.

II. Improve NAND Speed performance using FBI

A. Explanation of the UFS

The UFS device is a universal data storage and communication media. It is designed to replace previous eMMC devices and cover a wide area of applications as smart phones, tablets, etc. Figure 1 shows the concept of the UFS device, using M-PHY serial interface (3~6Gbps) which consists of differential Tx[3] and Rx[4] pairs. Using this serial interface, the UFS device can overcome the performance bottleneck of the host interface. As the data rate between the AP(Application Processor) and the eStorage device increases, it is possible to significantly increase the internal interface speed between NAND flash memories to the controller. This means that the performance bottleneck of the eStorage product has moved from the host interface to the internal NAND flash interface. Moreover, as the customer's demands for high density and high performance storage devices are increased, we should consider solutions to overcome the

[1] [eMMC] : Embedded Multi Media Card
[2] [UFS] :Universal Flash Storage
[3] [Tx] : Transmission terminal
[4] [Rx] : Receiving terminal

challenge between large capacitive loading caused by the multi-stacking dies and high internal I/O speed. For these reasons, we develop a new package with a FBI-chip to improve the performance of the high density UFS.

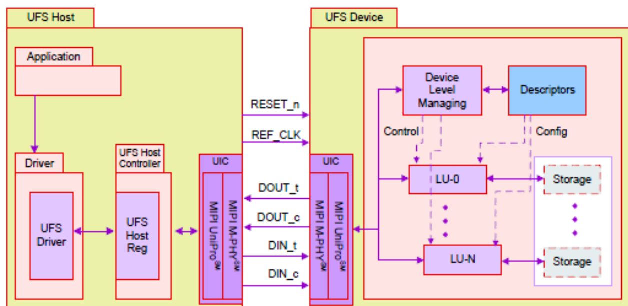

Figure 1. Conceptual drawing of UFS memory device

B. Basic concept of the FBI

In this section, we describe the basic concept of the frequency boosting interface chip (FBI-chip) to increase the internal NAND interface of the high density UFS device. As shown in Fig. 2, the FBI-chip places on internal I/O buses between the memory controller and the NAND flash memories. It mainly consists of the status decision logics and the retiming circuits. The status decision logics control the read or write operation of internal NAND interfaces. The retiming circuits support a retiming mode to reduce skews between the internally generated clock (DQS) and the data (DQs) and to extend the data valid window.

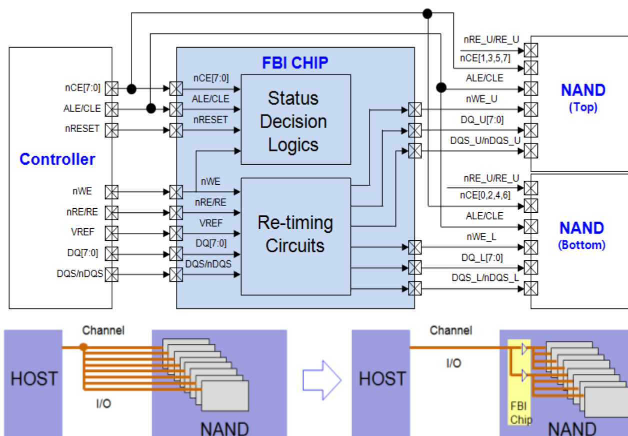

Figure 2. The FBI-Chip architecture

The key advantage of the FBI-chip is the improvement of timing margins caused by the larger capacitive loading in multi-die stacked environment. In Fig 3, The FBI-chip can reduce by half the capacitive loadings on the controller-to-NAND interfaces by implementing and evenly distributing two internal I/O buses between the FBI-chip and NAND chips. The reduction of the capacitive loadings leads to increase the slew rate of the DQ data signals and the DQS data strobe signal. Therefore, we can guarantee the improvement of the eye height and the timing margins for multi-stacked memory interfaces and can increase the internal interface speed.

In general, to increase the internal interface speed, we can use a 2 channel I/O memory controller which leads to increase the controller size and the cost. Additionally, large controller decreases the flexibility of controller chip position and pad location in the limited package size. However, since the FBI-chip is very simple circuits, as shown in Fig. 3, the chip size is very small and the I/O pad location can be placed freely, which means that the flexibility of the chip position can be increased and the routing spaces can be reduced in the limited package size. It leads to optimize the internal I/O speed and to reduce the UFS device cost (package manufacturing cost and controller net die, etc).

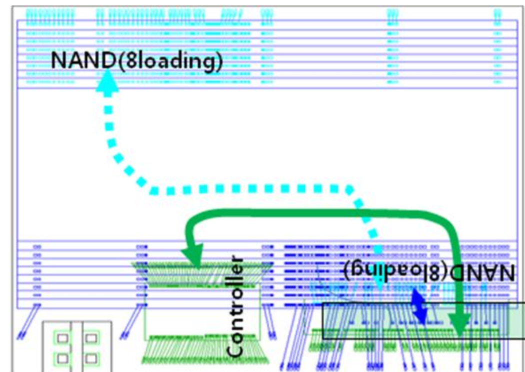

Figure 3. An Example of a Package Structure using the FBI-chip

III. Real application and results

A. *New package structure using the FBI*

Initial applied on the FBI chip is the eStorage product consisting UFS controller (named 'shark') and 16 stacked 64Gb MLC NAND. The FBI has also been produced in accordance with the pad order of the NAND. In the case of general 16 NAND stack, 2 channel 8-8 design or 2 channel 4-4-4-4 combination structure is much applied than 1 Channel 16 stack in order to lessen the burden of the loading according to the multi-chip stack.

The divided design of NAND group causes many problems, by listing them in the order as follow. In the view of assembly process, TAT (Turn Around Time) increase due to process where it is added and increase total assembly cost for the same reason. In the view of signal integration, due to the different lengths between the each NAND groups it is generated a difference in skew. Also routing becomes

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complicated by many channel path, and etc. In order to overcome the problems as in the above, the FBI was applied to difficult 16 stack products and then NAND structure composed of 8-8 stack. And 2-layer PCB structure became possible due to a same pad order of the NAND and the FBI through the routing path reduction. The signal degrade due to large-scale loading of 8 stack NAND are boosting in the FBI and it could control the skew due to the routing path of 8-8 the different length by the re-timing circuit of the FBI. In this final structure express in concept illustration in Figure 4 below. The 8 stack NAND of the upside, direct bonded in the NAND side pad of the FBI which the overhang structure of PACKAGE is underneath placed. The data related pad among this bonding is again connected to the controller which placed at directly through the re-timing circuit of the FBI. Another 8 stack NAND of the lower side, bonding by PCB and it is connected to the FBI through PCB routing and it is again connected to controller through the re-timing circuit of after the FBI.

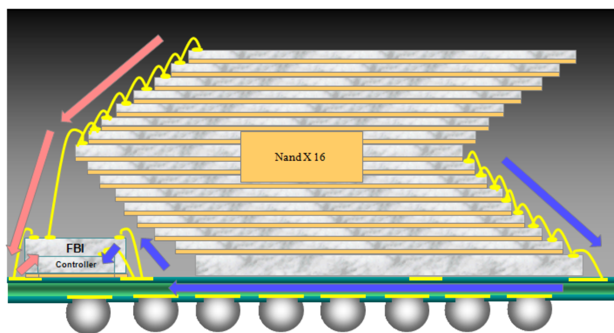

Figure 4. eStorage package structure using the FBI chip

Figure 5 shows the approximate PCB routing and actual structure of the product. Because of realign the pad order of the NAND to the FBI as been previously mentioned, it can see PCB pattern connected from NAND to the FBI as direct without being twisted. In order to prevent the growth of unwanted package size, controller and the FBI placed at the bottom of NAND overhang structure.

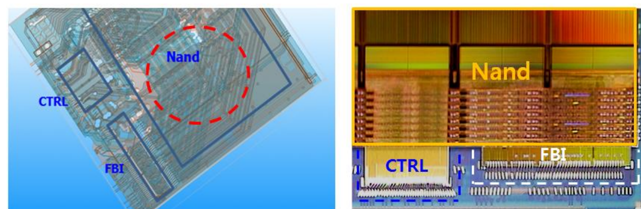

Figure 5. PCB routing & package top view

B. *The experimental method and environment*

In order to confirm the exact signal characteristic change by the FBI in this paper, the experiment proceeded in the wire of the pad through the direct probing. For this probing method, it is necessary to remove some of the top NAND that covers of the FBI and the controller chip. So remove some of the top NAND using vertical section and make probing area of the FBI and controller pad by restricted area laser de-capsulation.

C. *Reducing loading effect*

Loading reduction effect be majored advantage of the FBI can be found through the signal measured before and after passing through the FBI. Figure 6 and 7 below shows the improved signal through the FBI at the read operation 2 kind of signal. First signal is DQs (data strobe signal) which role as the clock and second signal is DQx signal which role as the data. Left signal show a huge rising time due to the large capacitive loading of the multi-chip stack before passing through the FBI. Such a large-scale rising time makes to delay the time reaching to the enough voltage level for data strobe. In addition enough time arriving in the full swing voltage level which device requests is not secured and it gets to have the relatively low voltage peak to peak value. Therefore the effective valid window recognizing data under this strobe signal environment gets to decrease drastically. It becomes the bottle neck of the speed improvement of the device. If this signal is passed the FBI, it can be improved as in right side signal in figure 6. Signal on the right side have an enhanced rising time and have wider valid window than before the FBI. Improved signal characteristics parameter can be found through the subsequent Table 1 & 2. In the table shows rise/fall time which is the greatest effect of valid window can be seen 500ps (60%) more decreased and VCCQ voltage level in which applied 1.8V can be seen decreasing level reduce -1.2V to -0.8V (50% improvement).

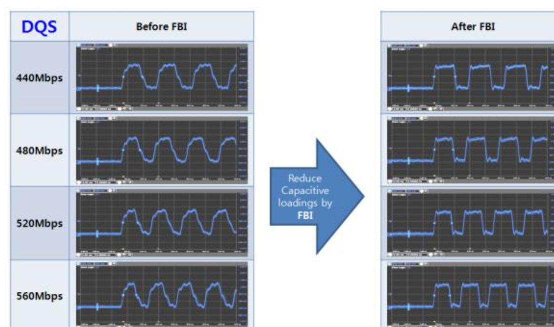

Figure 6. Reduce capacitive loading effect (DQS signal)

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	Before FBI	After FBI
Frequency	282.3Mbps	282.3Mbps
Voltage (P-to-P)	1.68V	1.72V
Rise Time	797ps	262ps
Fall Time	941ps	262ps

Table 1. DQS data strobe signal parameter between the FBI

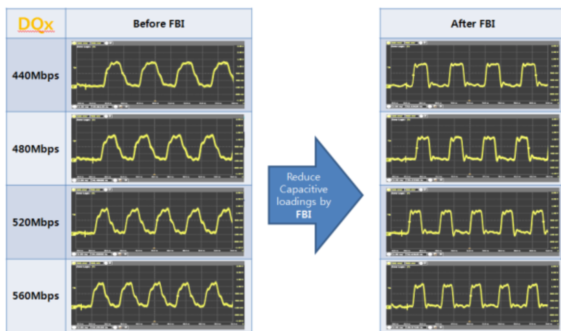


Figure 7. Reduce capacitive loading effect (DQx signal)

	Before FBI	After FBI
Frequency	276.0Mbps	262.3Mbps
Voltage (P-to-P)	1.69V	1.72V
Rise Time	816ps	253ps
Fall Time	959ps	217ps

Table 2. DQx strobe signal parameter between the FBI

D. *Improve internal I/F speed margin*

As to the loading reduction effect that the upper part mentions, can also improvement of eye open scale which role decision of internal speed margin. Figure 8 is show the result of estimate eye opening simulation of the FBI either before or after signal for each speed which in the worst operating condition of the NAND (cold temp -25° / 1.65 low voltage Level). In the simulation result, it can anticipated eye open value improve 5% to pass the FBI.

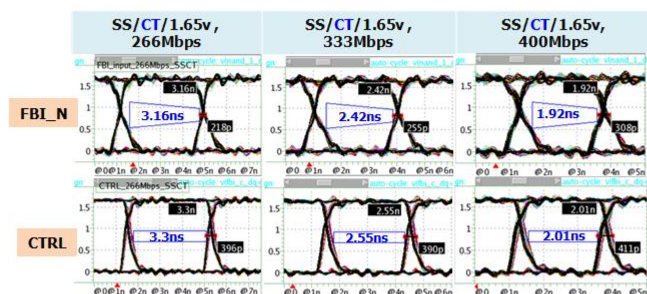


Figure 8. Eye simulation of the FBI

The eye opening size measurement for the verifying above simulation are summarized in Figure 9. Eye diagram illustrates of upper side is the DQx signal delivered NAND to the FBI. Because of package structure, signal analysis dealt with bottom side NAND. This is the result of read signal measurement in the FBI pad of the just before to enter the re-timing circuit of the FBI through the PCB routing which comes out from the bottom side NAND. The rising time of the signal is with a run increased due to ISI (Inter Symbol Interference) channel effect of PCB and the capacitive loading of 8 stack NAND. As a result, the margin of 50% UI (Unit Interval) is barely secured in relatively slow operating speed in 440Mbps. According to the increasing speed rate, eye margin shows that it decreases more and 34% is secured in 560Mbps. Eye diagram of bottom side is showed at controller side pad of the FBI with delivered to controller from passes the re-timing circuit of the FBI. It show improved signal quality by reduced capacitive loading and secured maximum eye margin through the re-timing process. The improved result of over 15% eye margin by the FBI are summarized in table 3.

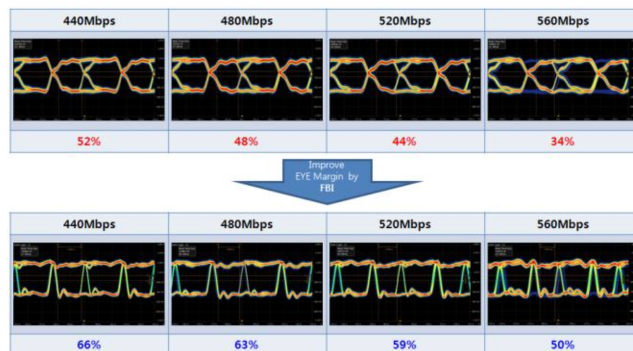
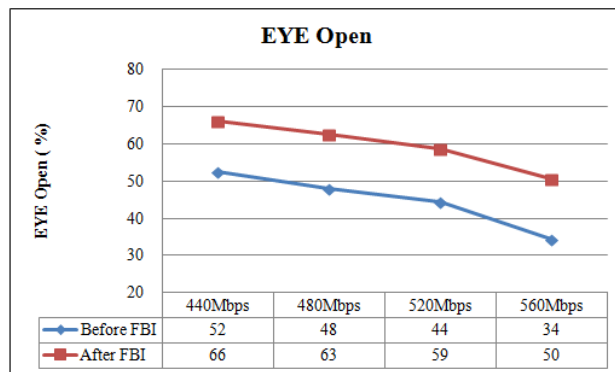


Figure 9. Compare eye open of the FBI effect



	440Mbps	480Mbps	520Mbps	560Mbps
Before FBI	52	48	44	34
After FBI	66	63	59	50

Table 3. Compare eye open of the FBI effect

In this way, the effect of sharply increase in eye opening ratio through the FBI is able to support more than 560Mbps internal speed which it is unable to do the support in the

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general 16 stack NAND device. Also a performance of the total device speed can be improve by the performance enhancement of the internal speed, due to the characteristic of UFS device which have enough external speed support.

IV. Conclusion

In conclusion, the FBI (Frequency Boosting Interface Chip) can be used in all large-scale loading effect device is a concern, through this, it is possible to obtain a large effect accompanying the improvement in the Signal quality. Summarizing the effects obtained through the application of FBI as follows.

1) Reduce loading effect
2) Higher bandwidth for internal interface with no signal distortion by reducing the capacitive loading
3) Routing space reduction on package substrate layers (substrate build-up cost reduction) by the flexibility of the small FBI-chip position

References

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