Packaging Tradeoff for SIP Integration Targeting High Speed PAM-4 Applications

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Abstract

High speed transmission systems using optical fiber are now focusing on 4-level PAM (Pulse Amplitude Modulation) format. This is requesting ultra-wideband electronic system in package, with a high phase linearity behavior in order to drive the electro-optical modulators. Moreover, new power DAC (Digital to Analog Converter) dies, are now available to generate up to 56 GBd, 4-level PAM signals, and providing $4V_{pp}$ of differential output amplitude swing. High frequency studies have been pursued to provide system integration in a BGA (Ball Grid Array) package. The BGA package transitions optimization and the configuration of multi-lines carriers, becomes a key step in the design flow. In this paper, some steps of the design, manufacturing process of the SIP (System In Package) and its demonstration board are proposed. The choices of the package, the thermal management, the clock management function are studied according to the final environmental constraint of the SIP. The data lines phase skew are analyzed with the support of EM (Electro Magnetic) simulations to better understand the potential impact on the output eye. Finally, the BGA package transition, simulated and measured results are compared, from DC up to 40 GHz and the measured SIP output, 4 levels, 56GBps eye diagram is presented.

Key words

BGA, Package, SIP, PAM-4, Optical Transmitter

I. Introduction

Today, Internet transmission is looking for secure link. High bit rate transmission system needs to meet performances, be cost effective and ensure up to 100 Gb/s on a single carrier. Multi-level format are getting more and more interesting and the main reason is that it helps to conserve a compact electrical signal bandwidth. The power DAC becomes a coder which generates the high speed multi-level format, feeding the EOM (Electro-Optical-Modulator) driver input by staying in the linear regime. During first experimentations on DAC system, it has been observed that it's very sensitive to high frequency mismatch, insertion losses and of course non-linear effect. That is the main reason why the HENIAC French project has focused on studying and developing packaging solutions for new very high speed DAC circuits realized in an indium phosphide (InP) double heterojunction bipolar transistor (DHBT) technology and leveraging the Power-DAC concept [1]. This paper presents the microwave approach used to integrate a high speed telecommunication system in a small form factor, hermetic package. It describes research and development efforts to integrate Power-DAC functions into high speed packages. The work has been divided into three parts. Each part includes an SIP development. The first 'SIP_A' is fully coaxially equipped and implements several chips to realize an overall 2-bit Power-DAC function [2, 3]. The second 'SIP_B' and the third 'SIP_C' include all RF inputs in BGA form, while RF outputs stay in coaxial connector form, in order to stay compatible with the standard EOM coaxial inputs. The second SIP includes two 2–bit-Mux-Power-DAC functions [4] and the third SIP includes two 3-bit-Mux-Power-DAC

functions [5]. These SIP are intended to enable next generation 400-Gb/s and 1-Tb/s optical communications systems [6]. Discussion on SIP_C characterization is not included here and will be published later when more developmental work is completed. For hermetic reasons, the package has been studied and developed by considering HTCC (High Temperature Co fired ceramics) techniques. Evaluation boards are developed using PCB (Printed Circuit Board).

II. SIP_A

This SIP_A present four independent NRZ (Non Return to Zero), data access working up to 28GBps. These input accesses are internally pair multiplexed, using the 'MUX-A/B' multiplexer chip to provide two 56GBps NRZ data bit rate lines. Then these two NRZ 56GBps data lines are combined using the 'CODER' electronic coder to provide the 4 levels, 56GBps output data shape. The chip associations, obliges particular clock management function integration in order to drive each of the 2 multiplexers chips clock access with synchronization from 28GHz to 32GHz. Herein synoptic of the SIP_A is described in the Fig.1.

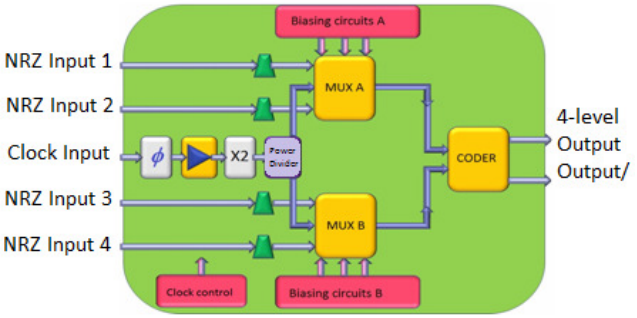

Figure 1:SIP_A Synoptic

Considering the complexity level of the development, it has been discussed to demonstrate the 'clock management' function capacity before integrated it in the package. Also, because of the synchronization need between the two multiplexer chips, it has been choose to introduce crossing between two high speed propagation supports. This crossing structure is described in the Fig.2. It has been decided to integrate, in the same package, the coding function and the clock management function. We choose to define the clock input frequency access at the bit rate half value. By this way, the phase shifter function is getting more feasible using GaAs MMIC in the 14GHz to 16GHz bandwidth than in the 28GHz to 32GHz bandwidth. Also, the impact of some clock residual signal propagation, in the used common substrate, or directly, in the package space, can be better reduce at higher wavelength. Considering phase shifter output amplitude variation, one side depending on the working frequency and the other side, depending on the phase control configuration. We decided to insert, an amplifier between the phase shifter and the frequency multiplier circuits. The amplifier is configured to work in compression regime as a limited function. By this way, the amplitude at the frequency multiplier input is less dependent on the phase state configuration. Finally, this is helping to reach low ripple on the integrated 'clock management' function frequency bandwidth from 28GHz to 32GHz.

We found that, the integration of components coming from different nature (MMICs, QFN, connectors…) needs a tradeoff between technology compatibility and microwave performance. For this reason, we have chosen to use a common substrate to interconnect all devices in the SIP_A. This substrate is compatible with SMD (Surface Mount Devices) techniques and bonding process, by this way, the chips output access is directly bonded to the transmission line which is, also, directly brazed to the SIP_A output coaxial connector pin. We choose to use an eight layers PCBs substrate composed by three 'RO4350' (Rogers) top layers and five 'FR4' (Flame Retardant 4) DC routing down layers. This was done to ensure the performance of the crossing multilayer HF transition. This 3D simulation model structure is presented in the Fig.2 and this photography structure is presented in the Fig.3.

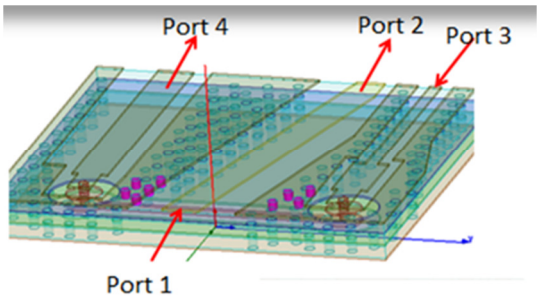

Figure 2: Multilayer HF transition in SIP_A simulation model.

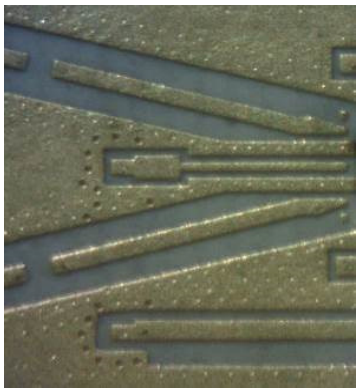

Figure 3: Multilayer HF transition in SIP_A structure photography.

The Fig.4. presents the obtain |S43| simulated and measured results of the structure presented in Fig.2 and in Fig.3. The insertion losses are about 2dB at 50GHz and the input and output return losses stay under -8dB from DC to 50GHz. These results are sufficient for the targeted applications and provide encouraging results for future development on wide bandwidth multilayer transition.

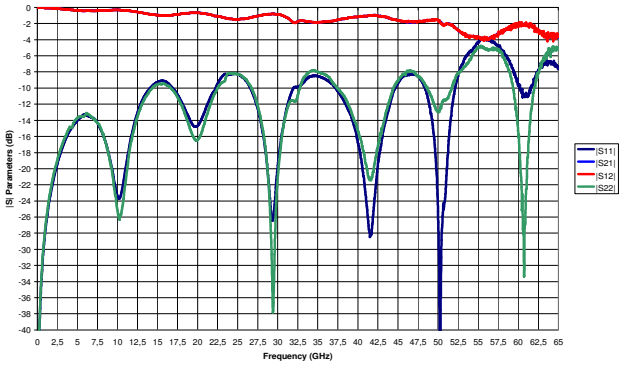

Figure 4: On probes, |S| parameters measurement results of the structures presented in the Fig.2 and Fig.3.

The Fig.5.a and Fig.5.b shows respectively, the SIP_A photography and 56GBps measured output eye diagram.

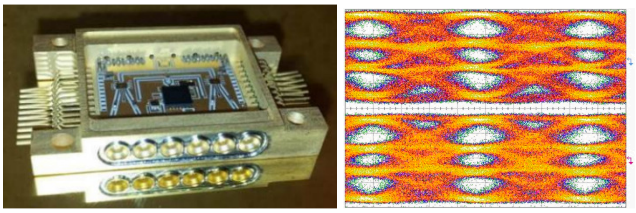

Figure 5: 'a': SIP_A photography and 'b': 56GBps Output Eye diagram, 500mV/div, 5ps/div.

III.SIP_B

The function demonstrated in the Fig.1 has been fully integrated in a single coder chip. This chip has been, dually integrated in the SIP_B in order to emulate a 200GBps transmission system. This SIP_B presents eight independents, BGA, data access working up to 28GBps NRZ and two independents, BGA, clock access working up to 28GHz. These data inputs access are combined 4 by 4 using two identical chips (CODER A/B, see Fig.6), to provide two pair of 4 levels, 56GBps output data shape. The BGA package has been studied in order to include a GLIPTOP heat sink located directly under the chips bottom. By this way, thermal dissipation is improved in comparison with a multilayer ceramic ground plane.

The consequent numbers of chips data inputs, requires a tradeoff for interface substrates. For the same reason mentioned at the SIP_A level, we decided to conserve PCB substrates for the output transmission lines, but we add thin film interfaces substrates in order to ease the five high frequency input access routing per chips. The thin film substrates are made using Alumina in 127µm of thickness. The minimum line width used is 100µm and the minimum gap used is 50µm. Grounded conductive vias are used to improve the shielding guide of each transmission lines. 3D-EM simulations have been pursued in order to obtain low insertion losses as 0.5dB up to 40GHz, and to limit the phase difference between each data lines to 10ps.

An evaluation board is used to report the BGA package of the SIP_B. This board includes delay lines on each data inputs to ensure the required phase skew optimization in order to avoid the potential output eye diagram phase distortion. It's also includes clock management function in order to drive each coder clock independently. The clock management function has been fully achieved by the use of SMD device reported on the evaluation board. This allow the phase control of the 28GHz-32GHz clock signal, at the input of the SIP_B, BGA package by tuning a trimmer on the evaluation board. The synoptic of the SIP_B is described in the Fig.6.

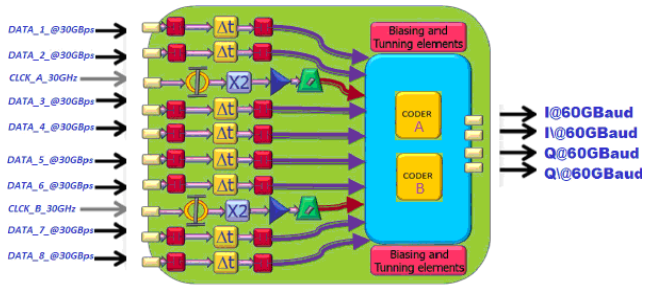

Figure 6:SIP_B Synoptic

Thanks to differential outputs available at the delay lines level. Using an embedded GPPO SMD connector, it has been very helpful to monitor the phase of each line during the measurement. The Fig.7.a and Fig.7.b shows respectively, the SIP_B photography and 56GBps measured output eye diagram.

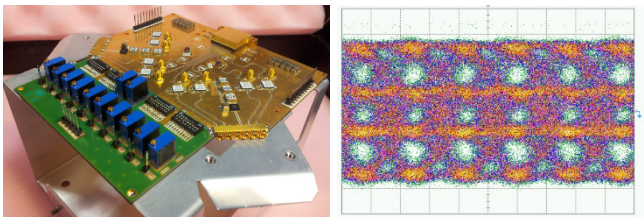

Figure 7.a: SIP_B photography and figure 7.b: 56GBps Output Eye diagram, 300mV/div, 10ps/div.

IV. SIP-C: BGA Transition

The SIP_C BGA transition photography is presented on the Fig.8. The HTCC BGA package is empty and reported on a PCB test substrates by solder operation. Then the probes (ACP40), with a 400µm pitch are used to do the CAL_LF measurements (green curves) using TRM (Transmission Reflective Match) technique. The probe connected to the VNA port 1 is placed inside the package. The probe connected to the VNA port 2 is placed outside the package, at the PCB level. For CAL_HF measurements (purple curves), the same procedure has been followed to complete measurements from 41GHz to 60GHz.

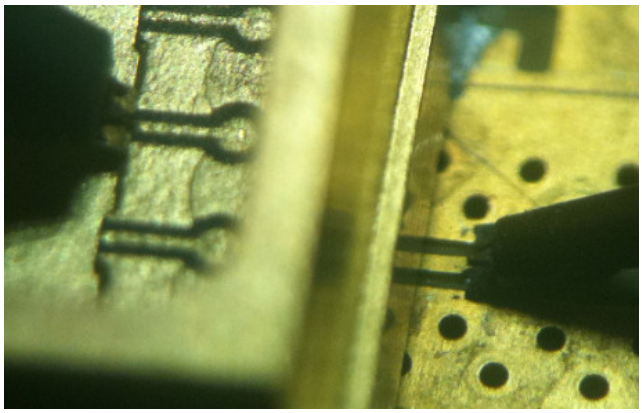

Figure 8:SIP_C, BGA transitions on probes measurement

The Fig.9 presents the obtain |S21| simulated and measured results of the structure presented in Fig.8. The insertion losses are decreasing continuously considering the frequency increase to 1.25dB at 41GHz. This measure results represents 0.03048dB/GHz.

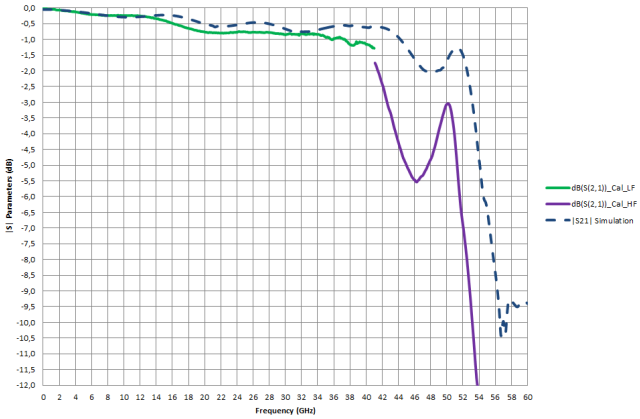

Figure 9: SIP_C, |S21| simulated and measured results

The Fig.10 presents the obtain |S11| simulated and measured results of the structure presented in Fig.8. The input return losses stay under -12dB from DC to 40GHz.

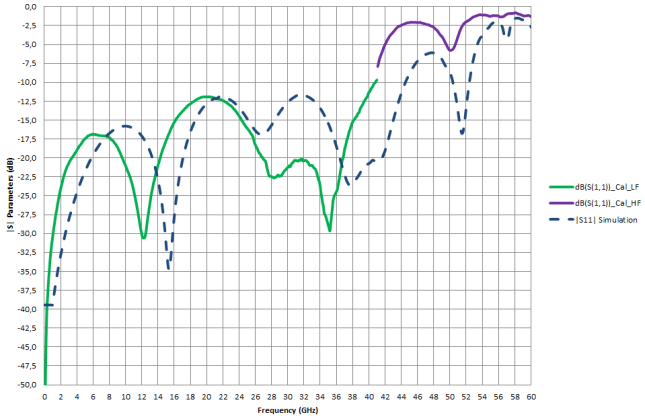

Figure 10: SIP_C, |S11| simulated and measured results

The Fig.11 presents the obtain |S22| simulated and measured results of the structure presented in Fig.8. The output return losses stay under -12dB from DC to 41GHz.

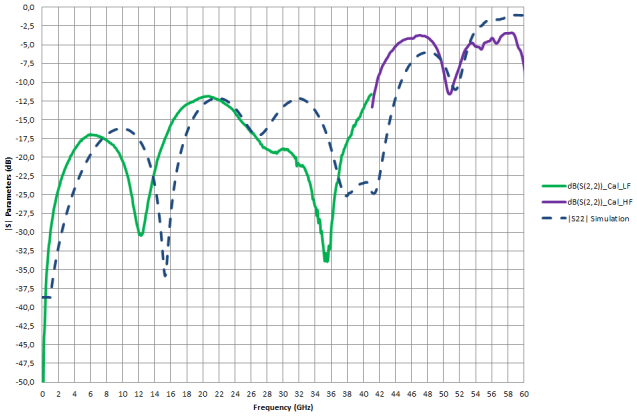

Figure 11: SIP_C, |S22| simulated and measured results

The Fig.12 presents the measured group delay variations of the structure presented in Fig.8. The group delay variations are about 2,5ps from DC to 25GHz. After, a positive 10ps deviation can be observed through 40GHz.

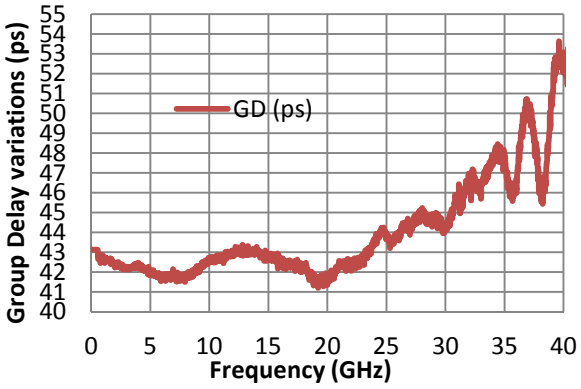

Figure 12: SIP_C, GD21 measured results

V. Conclusion

A new design of BGA transition for 'SIP_C' has been studied, simulated and measured. The proposed structure is based on a HTCC technology. Good correlations have been demonstrated between the measurements and the obtained simulation results from DC, up to 40GHz.

The 'SIP_B' study demonstrated the technical tradeoff by using thin film technology substrate for high number of chips input HF access and using a PCB substrate for linking a reasonable number of two output access.

The simulated and measured results of the 'SIP_A' study demonstrated that using a common PCB substrate to link high speed function chips with a limited number of three HF accesses, in a same package help to combine advantages of SMD and bonding techniques over 56GBps. Also, high frequency, multilayer transitions in PCB can help crossing data transmission lines and clock lines with an operating bandwidth of 50GHz.

High speed multiple DAC functions integrated in BGA packages are new considerations, which greatly contributed for future high speed optical network improvement. We are currently working on SIP_C demonstration and planning to deliver demonstration sets.

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