Bond Over Active Circuitry Design for Reliability

Stevan Hunter[1,3],

Jose Martinez[2], Cesar Salas[2], Marco Salas[2], Jason Schofield[2], Steven Sheffield[2], Kyle Wilkins[2],

Bryce Rasmussen[3], Troy Ruud[3], Jim Workman[3]

[1]Idaho State University, [2]Brigham Young University Idaho, [3]ON Semiconductor, Pocatello, ID

Contact: stevan.hunter@onsemi.com, *This work supported by ON Semiconductor*

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2011/1/000249/2343681/isom-2011-tp2-paper4.pdf by guest on 28 November 2022

Abstract

This paper discusses layout design rules for successful Cu wire bond-over-active-circuitry (BOAC) in 0.18 micron and other IC technologies having Al metallization interconnects (two-level metal and up) in SiO_2 dielectric, with W vias. The resulting bond pad structures effectively address BOAC pad reliability concerns, permitting Au or Cu wire bonding on relatively thin top metal. Cu wire bond is attractive on BOAC designs for lower cost than Au wire, while improving the thermal capability of the product. But Cu wire bond has presented even more challenges than Au wire bond due to higher stress to the pads during bonding, typically leading to increases in underlying films deformation and cracking. The new BOAC pad layout rules are based on the physical thin films principles, substantiated and refined through analysis of a large volume of experimental and product qualification data in various IC technologies. Interconnect layout beneath pads which follows the BOAC design rules creates more robust bond pad structures, preventing Al films deformation while strengthening the dielectric against cracking, and permitting free-form Si device design beneath. Substantial freedom in interconnect design is permitted in all metal layers beneath the pad, but the rules for top via and top-metal-minus-one layers are more restrictive than the rest. The BOAC design rules do not require any changes in wafer processing, they do not prevent the adding of redistribution or other layers for solder bumping or the like, but they do enable smaller die size and less expensive wire bond without jeopardizing bonding reliability.

***Keywords**: bond pad, wirebonding, Cu wire, pad design, pad layout, wirebond reliability*

Introduction

It is desirable to offer IC designers a BOAC (bond over active circuitry) reliable pad structure allowing "freeform" interconnect circuitry layout and Si devices including electrostatic discharge (ESD) protection below the pad window for smallest die size. Such a pad structure must able to withstand the mechanical stress of multiple wafer probe operations, ball bond stress from wire types including Cu, and other assembly stresses without cracking or weakening of the bond. It should be robust enough for high reliability applications, without increasing pad aluminum (Al) thickness or changing processes, and without adding costs. Additionally, it is desirable to have a method for determining potential locations on a die where a bond pad placement may be feasible without extensive modifications to underlying circuitry. In this work we report how the design of the BOAC circuitry in a pad can help to achieve these objectives simultaneously.

Traditional pad structures consist of sheets of metallization across the pad window in all metal levels, connected to the pad metal by via arrays. These pad structures have the same basic film stacks in CMOS 0.5um to 0.18µm technology nodes, which are featured in this work (see Fig. 1). Each metallization layer consists of aluminum-copper (Al(0.5%Cu),) film, which we will simply refer to as "Al", clad on top and bottom by thin refractory metal films, typically titanium - titanium nitride (Ti/TiN). Metallization layers are sandwiched between chemical mechanical polished (CMP) silicon dioxide (SiO_2) dielectric layers, which may contain small amounts of modifying elements such as boron (B), phosphorous (P), or fluorine (F) in lower dielectric layers. Traditional pad layout design rules prevent

any unrelated interconnect circuitry and silicon (Si) devices from being within a certain distance of pads due to the potential effects of mechanical stresses and ESD events.

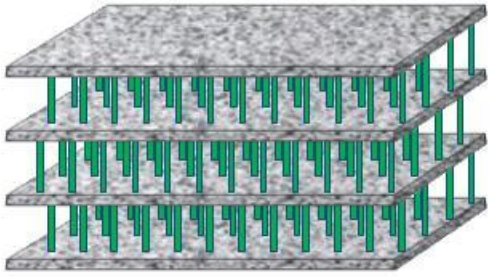

Figure 1 Illustration of a traditional Al - SiO_2 metallization 4-level metal pad structure with W vias

Each bond pad is part of an electrical circuit on the IC which is expected to function properly in use conditions as well as to provide the required ESD protection for the IC core circuits. The bond pad metal itself is traditionally an exposed portion of the metal top (MT) layer which we will refer to as the pad Al.

A bond wire attaches to the pad Al to enable electrical connection to the leads of the integrated circuit package. This connection can be a weak point in the overall product reliability and must be carefully engineered in practice for acceptable results. Nevertheless cracks easily form in the top intermetal dielectric (IMD) SiO_2 film at points of highest stress, with evidence of significant deformation in the metal top minus one (MT(-1)) metallization. Pad cracks and deformation seem to be tolerated to some extent in commercial grade ICs, but cracking or other bond pad damage is unacceptable in high reliability ICs due to the structural weakening.

Economic drivers have caused ESD protection devices and general interconnect circuitry to encroach or move into the traditional pad regions. BOAC is already commonplace, but the potential for cracks and other unknown issues increases concerns of designing BOAC into high reliability products. Cu wirebond may be also chosen for high reliability products, especially those in high temperature service. But Cu wirebond stresses the pad structure more than Au wirebond, increasing sub-layer films deformation and the potential for cracking, creating serious concerns regarding how to implement high reliability BOAC. Figures 2 and 3 are example photomicrographs of pad damage on pad test structures as viewed in the "cratering test", after removal of the bond wire and the pad Al film. Note how the cracks "follow" the top vias, as in a "connect the dots" drawing, highlighting a primary reliability concern in traditional pad structures.

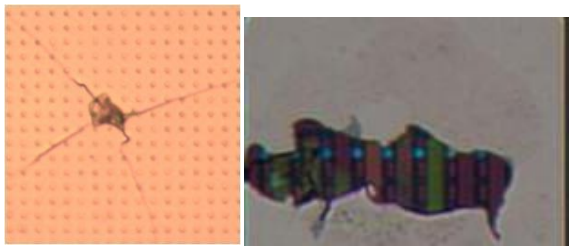

Figure 2 Cratering test reveals (left) slight wafer probe damage enhanced greatly by bonding on a traditional pad structure, (right) TiN voiding and divot in the top SiO_2 of a BOAC pad structure without top vias

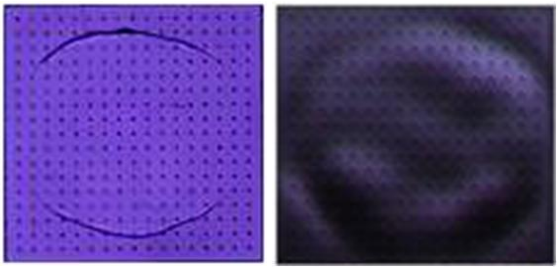

Figure 3 Cratering test reveals (left) bonding cracks on a traditional pad, (right) "ripple effect" from a the same type of Au ball bond on another traditional pad structure

The "ripple effect" observed in Fig. 3 (right) is caused by Al deformation in MT(-1) metallization and consequent bending in the top IMD SiO_2 film. Figure 4 illustrates this point, showing a focused ion beam (FIB) cross section of a "divot" associated with a long bonding crack that was observed in a cratering test. The initial vertical crack that started at the top of the top IMD SiO_2 is due to excessive tensile stress caused by the "hill" of Al in the MT(-1) metallization below. Note how the MT(-2) is deformed as well, causing the IMD above it to bend slightly, contributing to the overall film stack profile.

Downloaded from http://meridian.allenpress.com/isom/article-pdf/2011/1/000249/2343681/isom-2011-tp2-paper4.pdf by guest on 28 November 2022

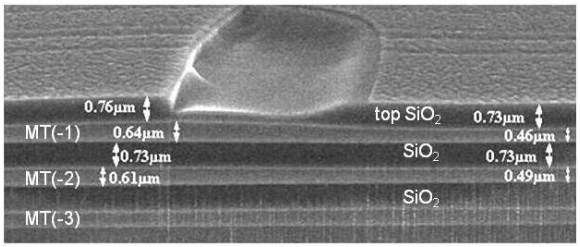

Figure 4 FIB cross section after the cratering test from a similar Au wirebond as in Fig. 3, showing a crack (upper left) and resulting divot in the top SiO_2 related to the Al film deformation below

Cu wire is preferred for new commercial products due to its lower cost as compared to Au wire. The increased electrical and thermal conductivity of Cu wire as compared to Au wire are beneficial for improved reliability as well. In fact, smaller diameter Cu wire to meet the same current flow requirements as larger diameter Au wire enables smaller pad size and pitch for die area reduction, further aiding in the design of lower cost die. The common strategy of significantly thickening pad Al to reduce Cu wirebond stress to the underlying fragile pad structure is not optimal for cost or high reliability.

The photos below show the differences in pad ripple after cratering test on traditional pad structures with 3 different pad Al thicknesses. Standard Au wirebond on a 3um pad Al film still causes significant sub-layer films deformation, though not enough to for SiO_2 cracking in this case.

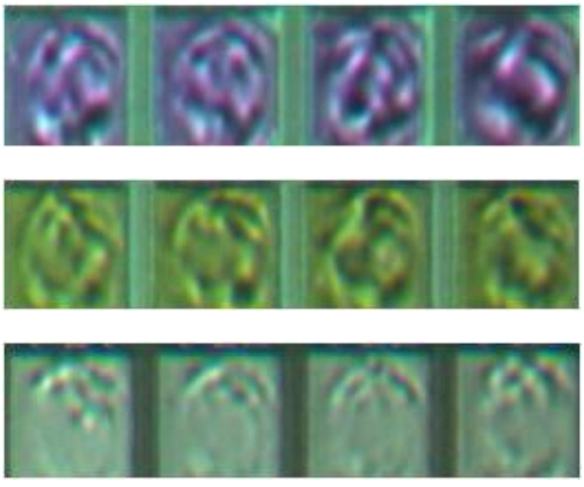

Figure 5 Cratering test "ripple effect" photos for Au ball bonding on a traditional pad structure with different pad Al thicknesses. (Top) 1um pad Al, 7% of pads cracked with this amount of ripple; (middle) 1.5um pad Al, 4% of pads cracked with this amount of ripple; and (bottom) 3um pad Al, with no cracking observed.

Design Rules Needed for Low Cost, High Rel BOAC

BOAC effectiveness in the circuit design requires the freedom to design interconnect circuitry in all metal levels below MT as well as unrestricted placement of Si devices and other components. Top IMD cracking in the pad window is an obvious threat to interconnects running through the pad region and must be prevented for successful designs. Al deformation in interconnect circuitry is unacceptable in high reliability parts due to higher resistance and compromised electromigration (EM) performance of metallization with compressed thickness. The type of Al deformation seen in Fig. 4 should not be permitted in a high reliability metal interconnect.

Low cost methods for implementing BOAC without adding new materials may designate only the MT and upper levels of metal and via layers as the "bond pad stack", with some special features or restrictions employed; then allow some circuitry in the pad region beneath. Some of the available methods don't actually prevent cracking in the top IMD, and none facilitate free-form layout of BOAC interconnects in all layers beneath MT without other cost-increasing or process change modifications. Thick pad Al is typical for Cu wirebond due to the increased bonding stress to a fragile pad structure beneath, but this adds cost and may cause design tradeoffs if thicker MT is implemented. Other BOAC methods are also too restrictive or add cost in some way, and may require modified or additional manufacturing equipment and requalification for changes in process or materials.

Previous work by our team has shown how the SiO_2 cracking relates to the sub-layer Al deformation [1, 2]. Our primary strategy for enabling lowest cost high reliability Cu wirebond on BOAC pads is to ensure that the interconnect metals do not deform under the pad, even under harsh wafer probe and harsh wirebond conditions. This effectively prevents the SiO_2 cracking and other pad damage. The BOAC interconnect circuitry itself can be designed to strengthen the pad structure, preventing its own deformation, thus preventing SiO_2 cracks, and

Downloaded from http://meridian.allenpress.com/isom/article-pdf/2011/1/000249/2343681/isom-2011-tp2-paper4.pdf by guest on 28 November 2022

facilitating high reliability applications. The more robust pad structure can in fact tolerate much more stress, opening the way for Cu wirebond to also be implemented for both lower cost and higher reliability without necessarily having to alter thickness in the metal top layer.

BOAC pads can be very sensitive to IMD cracks due to interconnect circuitry running through the pad structure. Cracks may be detected as electrical leakage if they join different electrical nodes together. The various readout points during reliability stressing (i.e. for example 0hrs, 48hrs, 168hrs, 256hrs, 512hrs, and 1008hrs,) provide an opportunity to detect a leakage increase due to pad cracks, as well as other degradations in the assembly and circuit. Thorough reliability testing becomes more crucial with Cu wire bonding on BOAC pads due to the higher bonding stress and increased likelihood of crack or other damage. Additional mechanical checks are helpful, because cracking that may have been initiated will still not be detected easily. In our work, additional BPS and BS, followed by cratering test are evaluated after the reliability stressing for comparison with results of unstressed bonded parts. The pad ripple assessment during the cratering test inspections is valuable. As mentioned, traditional pads in cratering test are seen to have much deformation of underlying Al, with visible strong ripple, which is a good indicator of a pad's propensity for cracking even when the cracks are not visible in the cratering test [3].

For Al metallization embedded in a CMP'ed SiO_2 dielectric film stack, prevention of the sub-layer Al deformation is accomplished by ensuring reduced pattern density of the Al interconnect circuitry within the pad window. Al films, being weak in compression but strong in tension, tend to deform into hills and valleys upon high stress to the pad, including some plastic deformation that remains, causing the optical ripple effect. Probing stress is mainly a down force and usually includes a lateral scrub motion in the pad Al film. Thermosonic ball bond includes down force pressure of the ball plus ultrasonic energy providing small high frequency lateral motion that promotes IMC formation and bond ball adhesion. The SiO_2 films are strong in compression but weak in tension, tending to crack when bent in conformance with the deformed Al film beneath. Sufficient bending of SiO_2 over an Al "hill" will exceed its tensile strength at the top to initiate a crack, while bending into an Al "valley" can initiate a crack at the bottom of the SiO_2. This type of deformation, ripple, and crack initiation are commonly observed on our test structures representing traditional pads, where we have been able to easily adjust wafer probe and bonding recipes to crack 100% of the pads.

Top vias are discouraged in the pad window due to their weakening effect. Another concern in considering higher stress to thin pad Al is to provide sufficient mechanism for absorbing the high ultrasonic bonding energy. The presence of metal features and vias in sub-layers are beneficial for this.

The example design layout guidelines of Table 1 (see [4]) for Al – SiO_2 BOAC pads, have been developed based on extensive experimentation with a variety of pad test structures in multiple manufacturing technologies. Note that MT thickness (pad Al thickness) is a primary factor in the design guidelines. Pattern density within the pad window is restricted for MT(-1) and MT(-2).

MT	Very thin	nominal	THICK
MT(-1) density ***MT(-1) width***	0-50% dense, *very narrow*	0-75% dense *narrow*	0-85% dense *not as narrow*
MT(-2) density ***MT(-2) width***	25–75% dense *wide*	15-90% dense *wider*	15-95% dense *widest*

Table 1 Example pad window interconnect design rules for an Al – SiO_2 interconnect technology, taking into account the effect of top metal thickness

Experimentally, the ripple effect after cratering test is a convenient method to assess the robustness of the BOAC structure. If ripple is suppressed through appropriate design of the BOAC circuitry, indicating that no significant metal deformation is occurring even after harsh wafer probe and harsh bonding conditions, then cracks related to metal deformation will of course not be present. As an example, layout rules were implemented with values appropriate in the specific IC process. The BOAC circuitry layout in the pad window produced a much more robust pad as demonstrated by the absence of ripple effect in the cratering test photos of Figure 6.

Downloaded from http://meridian.allenpress.com/isn/article-pdf/2011/1/000249/2343681/isom-2011-tp2-paper4.pdf by guest on 28 November 2022

Figure 6 Ripple effect is not present on these BOAC pads after bonding. These test pads are on the same die as the traditional pads in Fig. 5 top, with 1um pad Al thickness, for a direct comparison. MT thickness and standard or harsh bonding makes no difference in "ripple" on a robust pad structure – there is no deformation in sub-layer films, and no cracking or other pad damage.

Top vias may be allowed in BOAC layouts they if sparsely populated, assuming compliance with the restrictions in pattern density of MT(-1). Layout guidelines for MT(-3) and any sub-layers below that are "looser" than for MT(-2), as these interconnect metals are physically more distant from the highest stress region. Full sheets of metal (100% pattern density) are not recommended in any metal sub-layer within the pad window.

Bond Pad and Wirebond Reliability Discussion

Cu wirebond is desirable for high rel parts despite the harsh mechanical stress to the pad during bonding, except for the risk of oxidation or corrosion which must be addressed in wire production, storage, and packaging. Cu-Al intermetallic compound (IMC) tends to be very thin yet strong. It grows much more slowly than the Au-Al IMC in Au wirebonding. In our reliability testing of 1mil Cu wire ball bond, Cu-Al IMC still remained thin without bond strength degradation after 2000hrs high temperature storage life (HTSL) at 175ºC in a plastic package (Figure 7). The remaining pad Al is still separated from the Cu ball by a thin Cu-Al IMC. The edge of the ball is seen just starting to curve up at the right side, with pad Al extending to the right below the ball. Thin TiN and top IMD SiO_2 are seen across the bottom of the figure. This bond will be advantageous in high temperature use due to the slow IMC growth and lack of voiding, with continued low electrical resistance and good heat transfer.

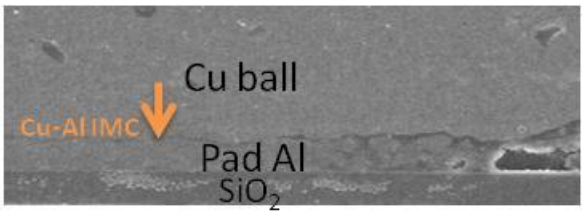

Figure 7 Edge of a Cu ball bond after 2khrs HTSL @ 175ºC by XSEM showing pad Al still remaining, not consumed into IMC. Thin TiN on top of SiO_2 is at the bottom.

In contrast, for the 1mil Au wirebond, we observe that the Au-Al IMC had already consumed most of the pad Al and formed large Kirkendall voids after this stress. Figure 8 shows an example, with no pad Al remaining. The IMC adheres well to the TiN, but is much stiffer and becomes more brittle with thermal stressing. Au-Al IMC is also much higher in electrical resistivity and the voiding continues to degrade this with thermal stressing.

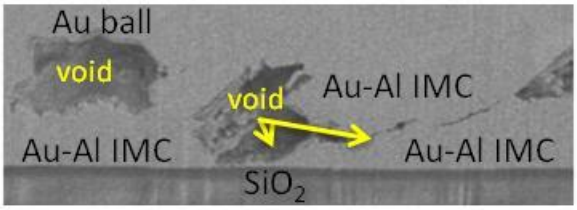

Figure 8 Edge of a Au ball bond after 2khrs HTSL @ 175ºC in FIB cross section, showing that the pad Al has been consumed into the Au-Al IMC under the ball, and large Kirkendall voids have appeared. Thin TiN on top of SiO_2 is at the bottom.

The BOAC structure beneath the ball bonds of Figures 7 and 8 are shown to be physically robust enough to withstand harsh wafer probe, and harsh wirebond (Au wire, "harsh" bonded Au, harsh Au(1%Pd) wirebond, Cu wirebond), and the rest of the assembly processing. There are no cracks or other pad damage observed, even after extended reliability testing. Cu wirebond on such pads allows wide flexibility in pad Al thickness for high rel parts, whereas Au wirebond for high temperature applications should be limited to relatively thin pad Al due to the rapid and continuing Au-Al IMC growth.

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2011/1/000249/2343681/isom-2011-tp2-paper4.pdf by guest on 28 November 2022

BOAC Design for High Reliability

For intended high reliability BOAC designs with Cu wirebond, we might further reduce the risk of cracking or other pad damage by considering the effects and interactions of the various layers and being more conservative in applying layout limits. We here discuss a 4-level metal example. For a pad with nominal pad Al thickness, we choose the "nominal" column of the Table 1 where we see that the MT(-1) pattern density guideline is 0 to 75%. Deformation and cracking risk may actually be further reduced if we impose a 0% to 50% restriction for the MT(-1) interconnect features in the pad window, effectively strengthening the upper structure with more SiO_2 just below the pad metal. In addition, we may be more conservative on the "narrow" metal width between spaces, slots or holes, so a more conservative approach would be to use a limit closer to the "very narrow" value in the "Very Thin" MT column. Such interconnects in MT(-1) may include wide busses that contain slots or holes to reduce the density, and multiple lines of small width, with spacing such that the overall pattern density within the pad window is no more than 50%. Because cracks from wafer probing tend to interact with the MT(-1) pattern, chamfering of any metal feature corners is appropriate. Uniformity in the pattern density is recommended for high reliability pads, especially in MT(-1) so some feature adjustment in location, placement of openings, or dummy metal fill may be appropriate within the pad window.

Top vias are not recommended in the probing region for cases of harsh, repeated wafer probe testing. Nor are top vias recommended in the pad window for harsh bonding on thin pad Al. So in this high reliability design, the top vias should be moved outside of the pad window.

Now considering MT(-2) interconnect design within the pad window, we encourage sub-layer features to absorb harsh ultrasonic stress due to the Cu wirebonding, while staying within the guidelines for pattern density to prevent Al deformation. If the MT(-1) density is near 0%, then the MT(-2) should approach its maximum pattern density, while if the MT(-1) is closer to 50%, then the MT(-2) pattern need not be so dense. Pattern uniformity is also recommended in MT(-2) layout for high reliability. Vias between MT(-2) and MT(-1) are also encouraged, so dense vias should be placed where possible.

The MT(-3) interconnect layout through the pad window is of less concern but should not exceed about 95% in pattern density, and the openings should be somewhat uniformly placed to be conservative. Vias are encouraged between MT(-3) and MT(-2). MT(-3) will have contacts to the Si for devices in a 4-level metal design, without any restrictions in layout of contacts or devices relating to the pad window region.

The BOAC pad layout principles discussed are easily adapted to accommodate different MT thicknesses and differing numbers of interconnect layers. For a 2-level metal pad design with nominal MT thickness, we combine the knowledge from the table with other experimental data to suggest 50% to 75% pattern density limits in Metal 1 (MT(-1)).

Reliability Tests for Wirebond on BOAC

Wirebond reliability has always been important in ICs. Various reliability qualification tests stress the pads and wirebonds. Reliability tests of traditional pads with Au wirebond assess the electrical integrity and resistance of the wirebond and pad structure by leakage, shorts and opens, and ESD testing. An IMD crack within the pad window of a traditional pad doesn't cause an issue electrically in this type of design, though it weakens the structure and may compromise long term bond integrity. If a crack were to propagate outside the pad it could cause a leakage path or short to a different electrical node.

Temperature cycling and thermal shock tests strain the materials interfaces and heighten the likelihood of films delamination or crack propagation, as well as to emphasize adverse effects of brittle Al_2Au growth of Au-Al IMC. An electrical high resistance or open may be caused at the Au wirebond interface due to oxidation or contamination, improper or excessive IMC formation, Kirkendall voiding, or films delamination. HTSL and high temperature operating life (HTOL) stresses thermally promote additional IMC growth and voiding at the bond interface. Moisture preconditioning (MC) includes high

Downloaded from http://meridian.allenpress.com/isn/article-pdf/2011/1/000249/2343681/isom-2011-tp2-paper4.pdf by guest on 28 November 2022

temperature thermal cycles and humidity, and the highly accelerated stress test (HAST) adds voltage as well. Electrical leakage or opens may be detected if cracks or delaminating edges are present at the IC surface. Mechanical shock (MS) and vibration variable frequency (VVF) tests potentially check for a very poor bond. ESD and LU (latchup) testing ensures that the electrical protection circuitry connected to the pad operates properly within acceptable limits after assembly.

Destructive mechanical reliability testing of traditional pads with Au wirebond includes bond pull strength (BPS), ball shear (BS), and the cratering test. In BPS and BS tests, the force at which the break occurs must be higher than the acceppted "safe" limit, and the failure mode is also noted. These mechanical tests help to detect poorly adhering bonds, film adhesion issues, and bonds severely weakened by cracks, and craters. Both Au and Cu wirebonds to robust pads are tested similarly.

The wirebond and pad Al are removed in the cratering test, and the underlying pad films are inspected for damage by optical microscope. Cratering damage is typically seen as cracks in the top IMD, divots in the IMD, or craters from parts of the pad structure breaking out. The optical ripple effect visible in cratering tests highlights the pad sub-layer films deformation and bending, as discussed.

In our reliability testing of wirebonding on robust BOAC pads with relatively thin pad Al, all results are "pass" for the various wire types used, but an interesting comparison between Au and Cu wirebond stands out. We confirm that the Cu wirebond is stable, with much less evidence of degradation after stress as compared to Au wirebond which degrades in both TC and HTSL stressing. BPS and BS data after 2000 temperature cycles -65C to 150C showed the Cu wire bonds being significantly stronger in both tests than Au, as expected. BPS and BS data after 2000hrs HTSL at 175ºC indicates no difference for Cu in BPS, but 10% stronger values for Cu in BS values. The Cu wire BS test after TC all sheared off the Al, as has always been seen in our unstressed Cu BS tests. However, all of the HTSL stressed Cu wirebond pads showed some TiN lifting off the top IMD in BS testing. The Cu-Al IMC has apparently consumed enough pad Al that the Al does not shear off so easily after such a long HTSL bake at 175ºC. In contrast, the Au wire data shows degradation in both tests by greater spread in the HTSL stressed pads, with twice the standard deviation value for Au BPS, and 4 times the standard deviation value in BS data.

Our data shows that unlike Au bonding, pad Al thickness need not be such a strong factor in long term reliability for Cu bonding on a robust pad structure. Another positive attribute of Cu wire is that its stiffness reduces the tendency for bending undesirably during packaging. But Cu wire is susceptible to oxidation and corrosion, problems which Au wire does not have. So package reliability testing should include checks for Cu wire corrosion and oxidation due to moisture stress at high temperature and package molding compound chemistry. Precise electrical testing before and after stress can detect wire or bond interface resistance changes. Scanning electron microscope (SEM) inspection of bonds and wires after decapping the parts following reliability stress is also appropriate prior to doing the additional BPS, BS and cratering tests because oxidation or corrosion of Cu wires may be detected visually. Cross sectioning the ball bond by polishing or FIB and then viewing by SEM is required to assess items such as pad Al "splash", IMC formation and thickness, voids, and pad metal displacement remaining (PMDR). Product reliability qualifications nearly always include ESD and Latch-up testing, with new pad designs as an integral part of this performance. BOAC pads and robust non-BOAC pads (adhering to the same guidelines, but without the intermetal circuit connections or Si devices beneath the pad window) have all passed these required electrical tests as implemented in their various products.

Reliability Qualification of the Pad Library

Robust BOAC pad implementation into manufacturing is tedious, because the pad itself is treated as a component in an IC design, which should be qualified through reliability testing before use. The first recommended task is to create a good pad layout design rule check (DRC) in the process or technology of interest. This DRC may be used to ensure that all of the various pad layouts conform to

Downloaded from http://meridian.allenpress.com/isn/article-pdf/2011/1/000249/2343681/isom-2011-tp2-paper4.pdf by guest on 28 November 2022

the BOAC pad rules. Non-BOAC pad cells which conform to the rules will be robust as well, and should be included in the library to replace traditional pad cells potentially permitting the choice of Au or Cu wirebond, for example, without additional cost. Pads with ESD protection and basic circuit under pad interconnects may also be designed as library cells, perhaps including generic busses through the pad window for connection of various electrical nodes that may be practical in typical designs. Such busses in the pad window need not be hooked up in the circuit, but they still can serve their purpose in creating the robust pad structure. Library pad cells must be qualified by manufacturing in a test chip or actual product through a suite of reliability tests prior to manufacturing release. A number of BOAC and non-BOAC robust pad designs can potentially be qualified together for "intrinsic" reliability behavior on the same test chip. Such pads may be further qualified for high reliability applications as they are included in product reliability qualification tests that include multiple lots and extended stressing.

Once a design library of qualified BOAC pad cells is available, layout designers may be given the freedom to modify them for specific applications. As long as the layouts still pass the DRC, they will be robust against cracking. Of course, fewer changes in the previously qualified structures reduce the risk of having a new issue in a high reliability application.

Another useful application for the pad layout DRC is for "pad anywhere" needs. A layout designer could place a pad window "anywhere" on a substantially completed circuit and run the pad DRC check. If the DRC passes, the pad may stay. If not, the designer will need to decide if the interconnect circuitry in the failure region of the pad window can be modified appropriately, or else the proposed pad must be moved to a different location. Designers are naturally very cautious about the placement of bond pad metal "anywhere" due to concerns about wafer probe, bonding, and assembly stresses to that site, especially if the pad Al is not very thick. A well implemented DRC check can correctly reveal the locations on a die layout that will be sufficiently robust for bonding, removing the guesswork and worry. Such DRC checks have been easily developed to ensure robust pad structures.

BOAC pad library cell designs have been qualified in various technologies having Al – SiO2 interconnect with multiple test chips and products, through extended reliability stress testing followed by additional BPS, BS, and cratering tests. Pads that are robust to cracking have passed all reliability qualifications with 1mil Au ball bonding, with both standard or harsh bonding recipe (harsh: purposely higher ultrasonic and lower stage temperature in Au bonding intended to cause cracking, or Cu wirebond instead), in both IC and discrete circuit technologies. The important caution still remains in high reliability applications regarding Cu wire's tendency to oxidize or corrode, so this must be addressed carefully in the assembly engineering of a high reliability product.

Summary

Reliability challenges for Cu wirebonding on lowest cost BOAC pads in 0.18µm and other IC technologies having Al - SiO_2 metallization can be substantially overcome by careful layout design of the pad structure. Example BOAC pad layout guidelines are shown, which can be developed into specific design rules for a given technology based on experimental data. When followed, the layout rules ensure that pads are much more robust against cracking from wafer probe and bonding stresses. Such BOAC pads have been reliability tested with extended stresses, with additional BPS and BS testing followed by cratering test, targeting high reliability products. A ripple effect assessment aids in predicting a pad's tendency for cracking, even though cracks may not be visible in the standard cratering inspection. Robust pads show very little or no ripple. BOAC pad layout rules can be easily applied in DRC check software, and both BOAC and non-BOAC library pads can be designed in conformance to the rules. These robust pads permit a wider range of wafer probe processes and choice of bonding wire types without having to increase the pad Al thickness. A variety of robust pads for a design library may be qualified through reliability stress testing on test chips or actual products. BOAC pad library structures can be placed in a die layout, and may then be modified as desired for the particular product design, with assurance of robustness to cracking as long as the BOAC pad DRC check passes. The concept of a robust BOAC "pad anywhere"

Downloaded from http://meridian.allenpress.com/isn/article-pdf/2011/1/000249/2343681/isom-2011-tp2-paper4.pdf by guest on 28 November 2022

placement by the use of a DRC check is introduced for further freedom in die layout.

Future Work

Further experimentation, finite element simulations, and continued reliability qualification testing are underway to refine specific design rules and extend robust BOAC pad designs to more manufacturing technologies.

Acknowledgements

Special thanks to Rhica Loredo of ON Semiconductor Philippines, and Daniel Vanderstraeten and Guy Brizar of ON Semiconductor Belgium.

References

1. Hunter, et al, “Use of Harsh Wafer Probe to Evaluate Various Bond Pad Structures”, IEEE SWTW, Jun 2011
2. Hunter, et al, “Use of Harsh Wire Bonding to Evaluate Various IC Bond Pad Structures”, IMAPS EMPC2011, Sep 2011
3. Martinez, et al, “IC Bond Pad Structural Study by Ripple Effect”, IMAPS 2011, Oct 2011
4. Hunter, et al, “Physically Robust Interconnect Design in Bond Over Active Circuitry for Cu Wire Bonding”, IMAPS / SEMI Wirebonding Workshop, Jul 2011

Downloaded from http://meridian.allenpress.com/isom/article-pdf/2011/1/000249/2343681/isom-2011-tp2-paper4.pdf by guest on 28 November 2022