Thin-Film Signal and Power Redistribution Layers Based on AL-X and Cu

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Abstract

Use of unpackaged die in advanced integrated systems (i.e., 3-D integrated systems) calls for dense interconnection schemes with controlled impedance for high-speed signal routing and minimal impedance for efficient power distribution. We have evaluated a new material set for use in a thin-film-based redistribution layer (RDL) that consists of Asahi Glass AL-X spin-on low-k dielectric polymer and electroplated copper metallization. This technology allows fan-out and interconnection of high-speed signals and power to/from die pads on pitches sufficiently less than 100 μm directly to companion die over short distances or for transition to underlying board metallization for longer transmission distances that may require lower signal loss. This technology is demonstrated using Si wafers onto which the thin-film RDL is fabricated. We have developed and described the fabrication procedures used to construct multiple interconnected layers of AL-X / Cu, which are compatible with standard wafer level packaging (WLP) processes. We have also evaluated the performance of this technology for high-speed digital signal transmission by characterizing frequency parameters (i.e., S parameters) of single-ended and differential strip-line transmission line structures. We have optimized transmission line geometries for transmission of signals at rates greater than 25 Gbps. In addition to high-speed signal redistribution capabilities, we have characterized power redistribution capabilities of this technology. Results of the signal and power integrity measurements and simulations performed in this work are presented.

Key words: thin-film, redistribution, signal integrity, power integrity

1. Introduction

Achieving the tight integration sought after in modern 3-D integrated systems is increasingly requiring the use of unpackaged die. To accommodate the extreme pin densities found on these die, the interconnects used to route both high-speed signal and power lines must also be much more dense than currently possible with traditional printed circuit board (PCB) technologies. One solution to address this problem lies in the use of redistribution layers (RDL) to fan out from the high pin density on the die to a lower density that can then be routed through a PCB.

Use of a thin-film materials set consisting of AL-X 2010 and Cu to fabricate such a RDL structure will be demonstrated. AL-X possesses many characteristics which make it suitable for use in this fabrication including a low dielectric constant (D_k = 2.6), low dielectric loss (tan δ = .001), and excellent planarization capability [1]. Once deposited, these planar AL-X layers allow for Cu deposition through the use of electroplating. Very smooth surfaces with minimal surface roughness are an additional advantage of this technology. The photolithography used in this process allows for minimum feature sizes on the order of 5 μm, which provides substantial flexibility in the design of RDL structures. This fabrication process is detailed in the next section.

Of particular interest for any RDL is its performance at the high frequencies required for high-speed digital communication. RDL test structures have been built and evaluated for their frequency characteristics up to 50 GHz. Simulations have also been performed to model the expected behavior of these structures. These results will be used to show that high-speed signal lines in this technology perform sufficiently for

signal transmission at 28 Gbps over necessary distances in a differential configuration.

Power distribution structures for use with LTCC boards have also been evaluated in simulation. Methodology used for calculating impedance of RDL structures is discussed and applied to provide impedance measurements for these structures.

2. Thin-film Fabrication Process

The aforementioned stack-up of thin-film redistribution layers (TF RDLs) is comprised of highly planar and smooth layers of the spin-on dielectric polymer AL-X 2010 and an electroplated conductor (Figure 1). Processing on Si and LTCC substrates includes steps that establish copper pillars as via connections between copper conductor layers. Chemical mechanical polishing (CMP) is used to achieve a high degree of surface planarity and material thickness control for each subsequent layer in the steps described below:

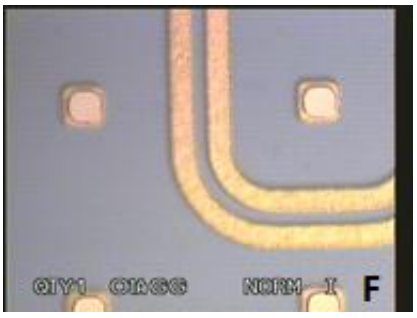

Figure 1.a: Single TF RDL layer top down view.

Figure 1.b: TF RDL Cross Section.

STEP A: The pattern is defined through photolithography using a photoresist amenable to the plating chemistry. The electroplating process requires a conductive seed layer, which must be deposited on the substrate, prior to patterning, by means of thermal evaporation or some other thin-film deposition technique (i.e., atomic layer deposition (ALD)). Shown in Figure 2.

STEP B: Pillars (vias) are over-plated by a thickness of a few microns past desired height (i.e., 14 microns total thickness for our present case). Shown in Figure 2.

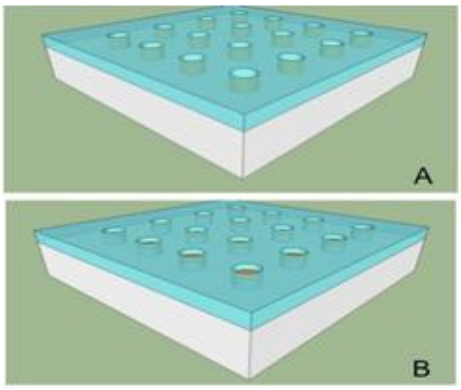

Figure 2: Photolithography and Electroplating.

STEP C: The photoresist is removed to expose the pillars and to allow for seed layer removal. Shown in Figure 3.

STEP D: The dielectric is spun over the substrate and pillars (i.e. 16 microns total thickness). Shown in Figure 3.

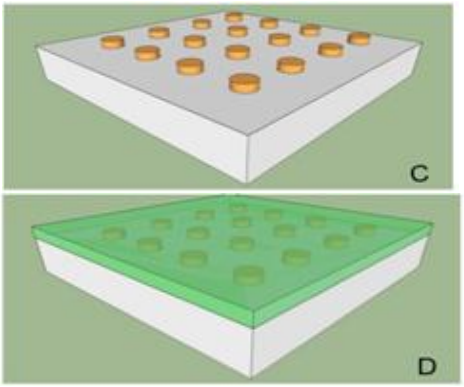

Figure 3: Photoresist Removal and AL-X deposition.

STEP E: Chemical Mechanical Polishing (CMP) is used to remove sufficient material to achieve a highly planar surface with uniform metal and dielectric thicknesses. (i.e., 10 microns total layer thickness). Shown in Figure 4.

STEP F: A copper conductor is defined through seed layer deposition, photolithography and plated to connect to the pillars. After photoresist removal and dielectric deposition the top surface is again thinned and smoothed using CMP. Steps A-F can be repeated to form a second redistribution layer. Shown in Figure 4.

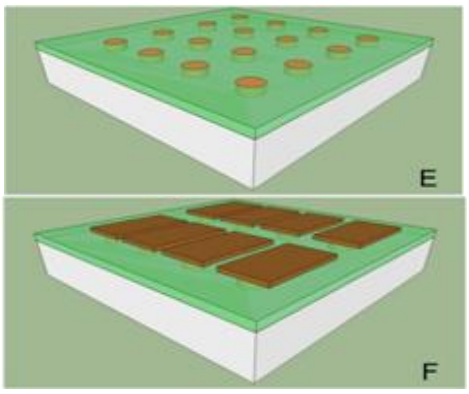

Figure 4: Highly planar surfaces are required over multiple redistribution layers.

3. Signal Integrity

Simulation

To predict the behavior of fabricated TF RDL signal lines, Ansoft HFSS 14 was used to generate simulated S parameters for both single-ended and differential stripline transmission line configurations. HFSS was chosen due to its ability to model structures in full 3-D, which allows for closer approximation of via performance.

In both configurations, 10 µm thick AL-X layers and 3 µm thick Cu layers were used with a 10 µm line width and 30 µm square vias space 35 µm from the line and from other vias. Spacing between lines was set to 8 µm for the differential configuration. Top and bottom Cu ground planes were used with a Cu signal layer placed inside two layers of AL-X; stitch vias were included to connect the ground planes. Port impedance was set to 50 Ω for single-ended lines and 100 Ω for differential lines with the Driven Terminal solution type selected [2]. All simulations model a 1 inch long line with no attached launch structure, A differential structure is shown in Figure 5.

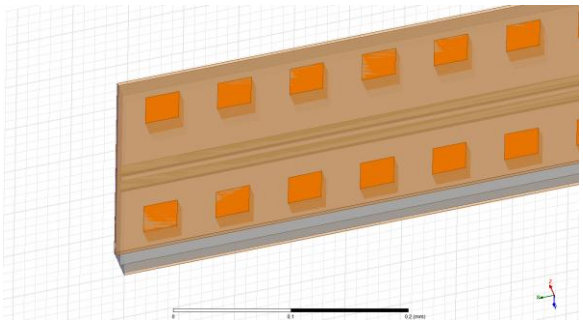

Figure 5: HFSS Model of a Differential Line.

To verify that the estimated line width would yield a 50 Ω line, a single-ended configuration was simulated first. Figures 6 and 7 present simulated S parameters for this configuration.

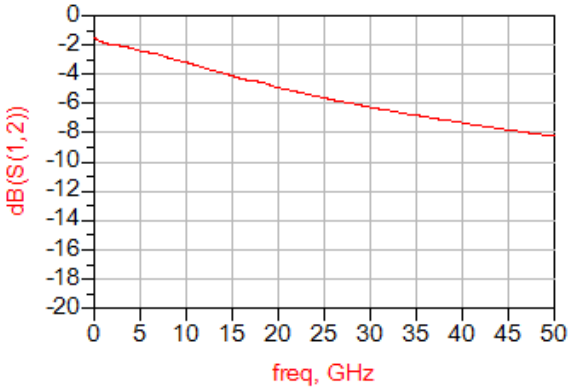

Figure 6: S_{12} for a 1 inch Single-ended Line (simulation).

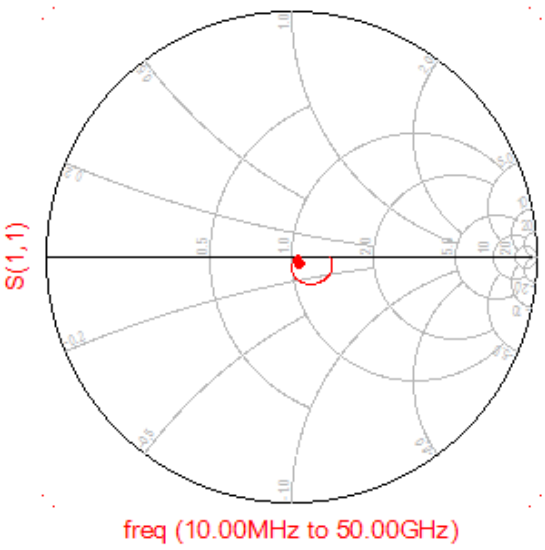

Figure 7: S_{11} for a 1 inch Single-ended Line (simulation).

These figures demonstrate that the TF RDL lines suffer from increasingly high loss as frequency increases (Figure 6) but maintain a good match to 50 Ω up to 50 GHz (Figure 7). From these results, it is expected that loss of a RDL signal line will be approximately 8 dB/in at 50 GHz, with an improvement of approximately 1 dB/in less loss for every 10 GHz decrease in frequency.

While single-ended lines provide insight into a technology's performance, most modern high-speed transmission requires the use of differential lines for the improved noise rejection and reduced crosstalk effects they can provide. To better demonstrate the differential mode performance of these structures, mixed-mode S parameters were generated from simulation; of these, only the differential-to-differential (S_{DD}) are included in discussion of differential results. Simulated results of a differential configuration are shown in Figures 8 and 9.

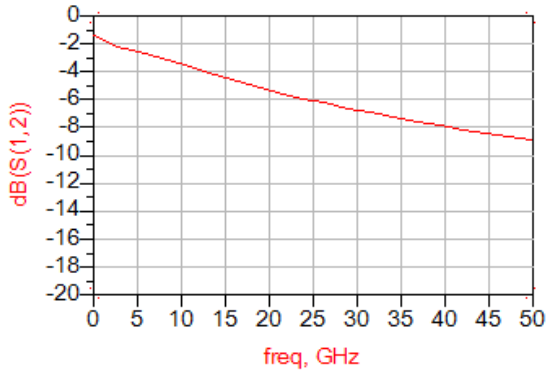

Figure 8: S_{DD12} for a 1 inch Differential Line (simulation).

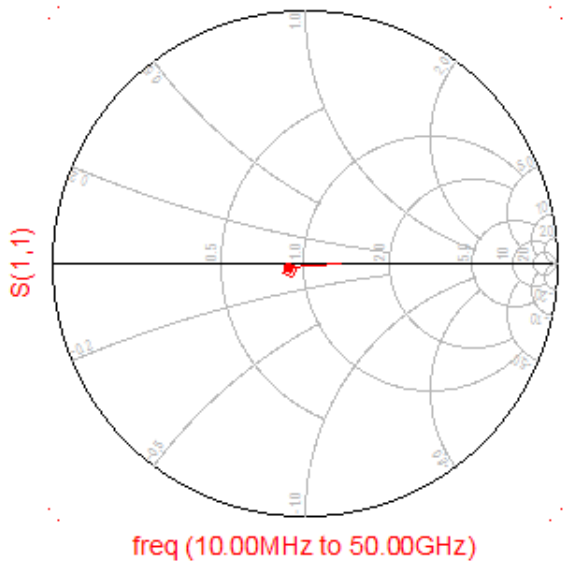

Figure 9: S_{DD11} for a 1 inch Differential Line (simulation).

The differential configuration demonstrates slightly increased loss when compared to its single-ended counterpart; the increase is approximately 1 dB/in at 50 GHz but decreases to an insignificant difference at 25 GHz. This increased loss is due to reduced line-width compared to single-ended structures required due to coupling between the lines causing a reduction in characteristic impedance.

Measured Data

Thin-film RDL structures corresponding to those described in the above simulation section were fabricated on a 4 inch Si wafer using the previously described fabrication steps. To allow for physical measurement using probes, a minimal launch structure was added to the design on both ends of the stripline transmission lines. Structures were probed with GGB Industries 50A (2.4mm) GSG or GS/SG probes. Calibration was performed to the probe tips and the fixture removal function provided by Agilent PLTS 2012 was used to de-embed the launch structures.

Measurements were performed using an Agilent PNA-X N5245A (4-port). The frequency was swept from 10 MHz to 50 GHz with 5000 data points and an IF bandwidth of 1 kHz. Results for insertion loss and return loss for a single-ended stripline transmission line are shown in Figures 10 and 11.

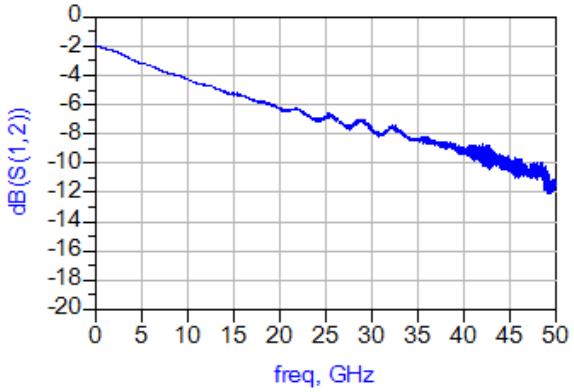

Figure 10: S_{12} for a 1 inch Single-ended Line (physical).

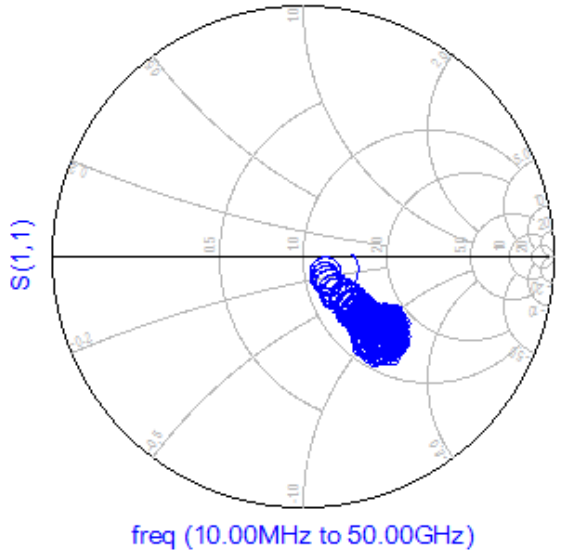

Figure 11: S_{11} for a 1 inch Single-ended Line (physical).

These results demonstrate somewhat lower high frequency performance than expected from simulated results. At 50 GHz, the physical structure exhibits approximately 4 dB/in more loss than the simulated structure; this difference decreases to less than 2 dB/in at 30 GHz but does not disappear until the frequency is decreased to near DC.

Because the test equipment, cables, connectors, and probes used were rated for a maximum frequency of 50 GHz, some of the performance disparity can be attributed to the testing setup. A more important difference can be found by noting the less ideal match presented in Figure 11. This figure indicates that the physical structure as fabricated is inductive and will require additional fabrication process optimization work for more ideal performance. The major fabrication issue is optimization of the CMP process to provide optimal dielectric thickness. Metallization thickness and line-width control are sufficient to produce desired performance. We also note that we regularly observe roughness less than 25nm, which should cause a negligible increase in insertion loss.

As with the simulated differential configuration results, the physical results show a slightly increased loss for the differential configuration. The results for insertion loss and return loss for differential stripline transmission line structures are presented in Figures 12 and 13.

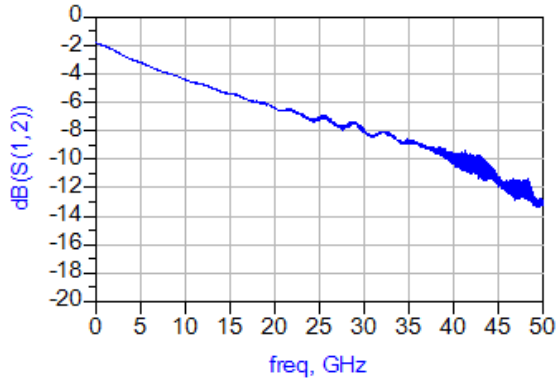

Figure 12: S_{DD12} for a 1 inch Differential Line (physical).

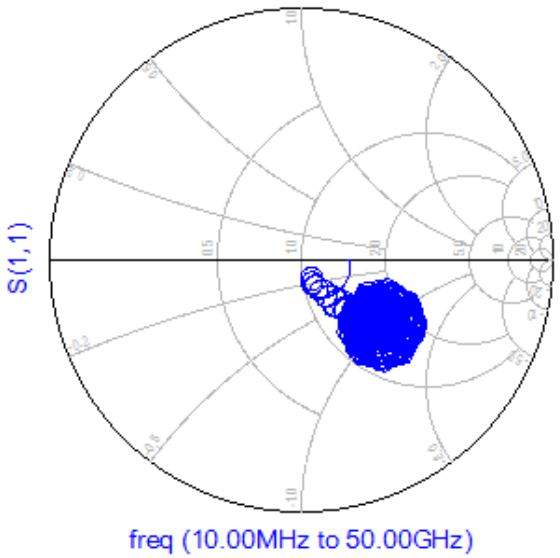

Figure 13: S_{DD11} for a 1 inch Differential Line (physical).

From near DC to approximately 30 GHz, the differential measurements are identical to the single-ended measurements; beyond 30 GHz, the differential structure produces 1 dB/in more loss than the single-ended structure. Examining Figure 13 reveals that the two structures are similarly (non-optimally) matched for lower frequencies with the difference in matching appearing and becoming more prominent as the frequency is increased.

Despite the fact that physical structures were found to have higher loss and be less optimally matched than expected, their simulation counterparts indicate that, with improved fabrication techniques, this technology allows for

construction of RDLs with high performance over a wide frequency range. It is anticipated that future structures will even more closely match expected results as fabrication tolerances are reduced.

Link Performance

To expand on the frequency characterization presented in the previous section, high-speed link simulations were also performed using data measured from the physical structures. Because single-ended lines are unsuitable for this type of link, a differential configuration was used. Link simulations were performed with Agilent ADS 2010.10 using AMI models of the high-speed transceivers available on Altera's Stratix V GT FPGA [3].

A transmitter running at 28 Gbps fed by a PRBS source was connected to a receiver implementing DC gain and fixed equalization by an S parameter block using the data presented in Figures 12 and 13. No optimizations were enabled on the transmitter. Figure 14 shows the performance of this link.

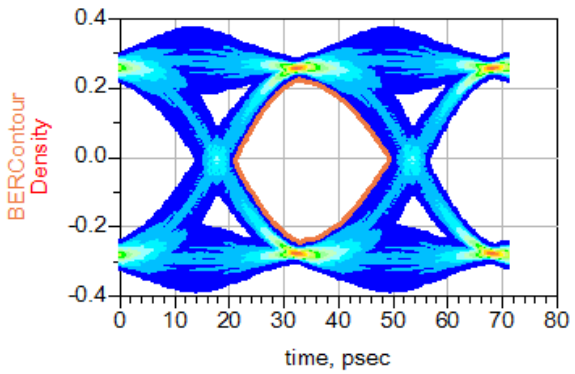

Figure 14: Eye Diagram and BER Contour for a 28 Gbps Link.

The bit-error rate (BER) contour shown was constructed for a BER of 10^{-12} (i.e., one error in every 10^{12} bits transmitted). Both this contour and the associated eye can be seen to be completely open, indicating that the link is able to run virtually error free at 28 Gbps. With pre-emphasis and de-emphasis capabilities enabled on the transmitter, it is expected that transmission at this rate can occur through lines significantly longer than the 1 inch line used in this paper.

4. Power Integrity

To serve as a redistribution layer for power and ground nets the interconnect network must exhibit a minimal impedance over a broad frequency range rather than a controlled 50 Ω impedance. We desire this low impedance over a range of frequencies that allows the power distribution network to respond to the current spectrum of switching loads.

Measurement Capabilities

A series of LTCC substrate structures were designed, simulated, and fabricated to demonstrate measurement capabilities from the low MHz range to multiple GHz. These substrate structures consist of a microstrip with 1-, 3-, or 15-via connections shunting the signal and ground conductors. The signal width is 1 mm, via diameter is 6 mils, and the substrate is 20x40 mm and features coaxial connectors.

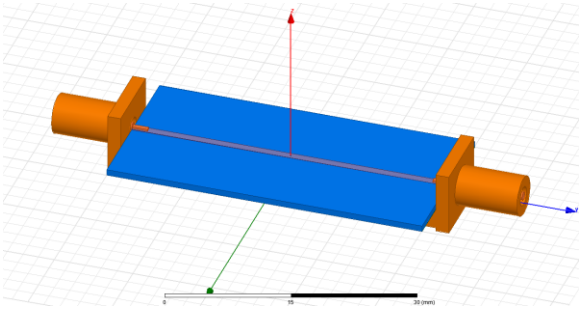

Figure 15: LTCC Substrate Microstrip DUT.

The LTCC structures were simulated using Ansoft HFSS 14 and a 2-port driven modal simulation from which both the impedance and scattering matrices could be extracted. As the DUT impedance in question is much smaller than 50 Ω it can be assumed that the entire signal from port one into the DUT is reflected, and that the impedance can be found from the voltage observed at port two. The current creating this voltage is comprised of both the incident and reflected current [4]. This first order analysis gives an estimate of the impedance as the ratio of the measured and incident voltage (S_{21}) multiplied by 25 Ω. To gain more precision a second-order solution can be found using the equation below [4-5] and a full two-port calibration at the connector plane [5].

$$Z_{DUT} = 25\ \Omega \times S_{21}/(1-S_{21}) \quad (1)$$

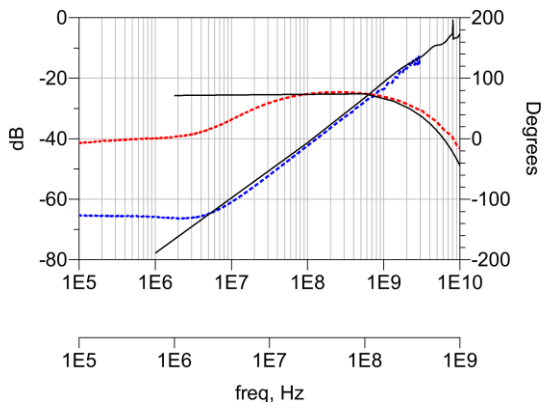

Figure 16: S_{21} (phase shown in red with smaller sweep range) of 1-via shunt DUT measurement with Agilent E5016B s-parameter measurement compared to simulation using HFSS 14.

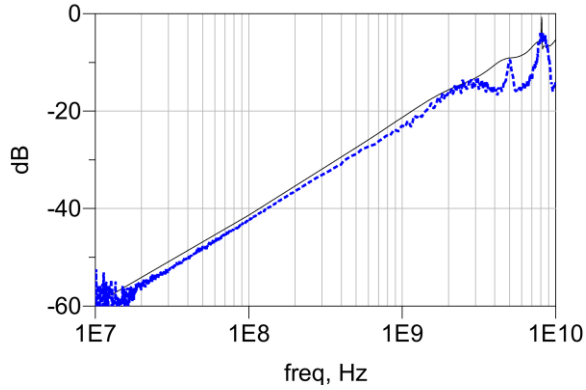

Figure 17: For higher frequency S_{21} measurements an Agilent E8364B was used; and is again compared to simulation (solid black line) of a single-via DUT within HFSS 14.

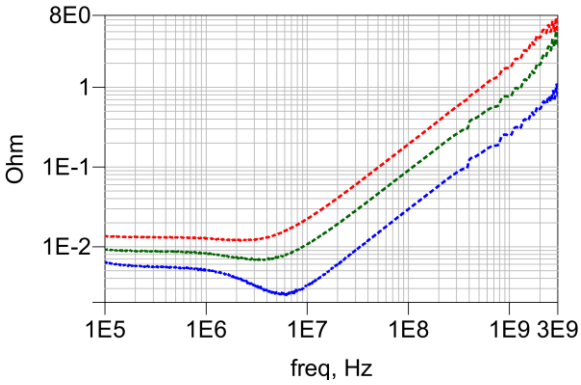

Figure 18: $|Z_{Tranfer}|$ from S_{21} of 1-, 3-, 15-via DUTs shown in red, green and blue respectively. (Measured on Agilent E5016B)

Measurements made of the DUT group represented in Figure 15 are of the transfer impedance and are limited in frequency range due to the use of soldered coaxial connectors. Measured and processed results are shown in Figures 16 to 18. To achieve more precise measurements at higher frequencies it is necessary to use wafer probes on either the substrate or the RDL directly [5]. The use of wafer probes also allows for more flexibility when making self-impedance and transfer-impedance measurements. To achieve agreement with the self-impedance (shown as a solid red line in Figure 19) through measurement it was necessary to solder additional coaxial connectors onto ports one and two; placing both network analyzer ports on the same DUT port and terminating the open DUT port with 50 Ω. [5]

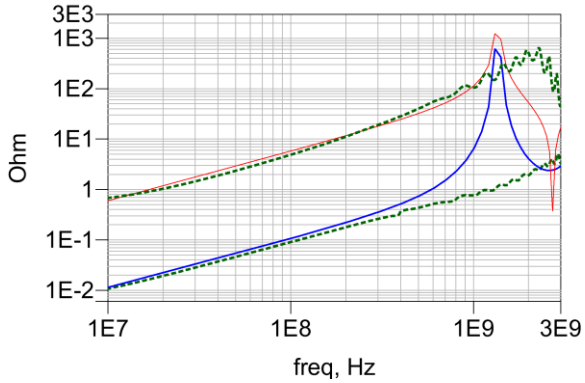

Figure 19: Self- and transfer-impedance from S-parameter measurement of the 3-via DUT (green, using E5016B) and simulation using HFSS 14, where self-impedance is shown in red and transfer impedance in blue.

Simulation

The methodology used in the previous section to show agreement between LTCC substrate simulation and measurement can be applied to power distribution characterization structures fabricated from AL-X and electroplated copper as well. To mimic the LTCC DUT group simulation of a thin-film microstrip design (27 µm line width, 3 µm metallization height, 10 µm dielectric height, and 1" length) was performed. Signal-ground shunt via connections were given a radius of 5 µm and placed in a single via, two parallel via, or six parallel via (Figure 20) configuration.

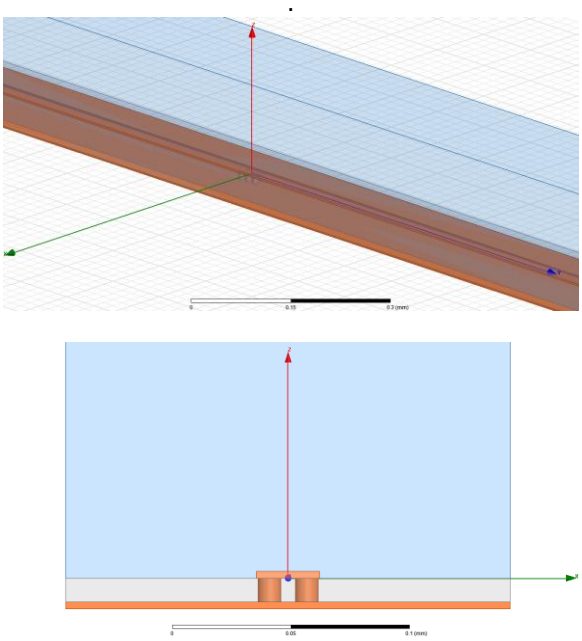

Figure 20: HFSS 14 model of thin-film shunt-through microstrip DUT without signal launch. Top: 3D perspective view. Bottom: View from edge of structure.

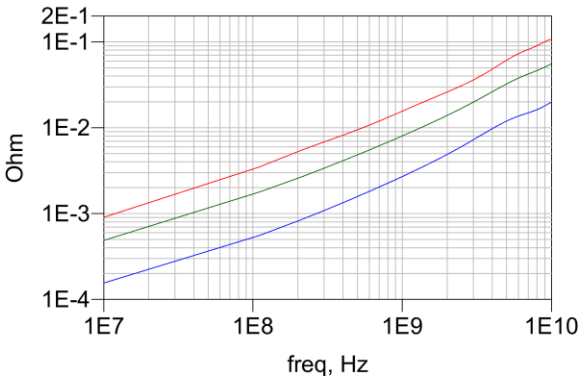

Figure 21: |Z| from S_{21} of 1- , 2-, and 6- vias in parallel as simulated using HFSS 14, shown in red, green and blue respectively.

The simulation output in shown in Figure 21 shows a similar, albeit lower magnitude, impedance profile to what is shown in Figure 18, and speaks to the possibilities of using AL-X and copper based thin-film redistribution layers for power distribution networks requiring dense fan-out/in of device and substrate power rails.

5. Conclusions

It has been shown that TF RDLs built using the fabrication process described in this paper are capable of required performance for high-speed signal redistribution. Although measured loss appears relatively high, links running at up to 28 Gbps have been shown (through simulation) to close successfully. The performance afforded by the minimum feature size and minimal surface roughness of this technology will allow for RDLs to be constructed that will accommodate the high density of bare die interconnects, the demanding signal integrity required to reliably transmit high-speed signals and the power integrity to allow clean and efficient power distribution networks.

With additional fabrication process refinement, it appears that transmission of high-speed signals over longer distances and at higher rates will be possible in this technology. Work on current issues including impedance matching and power distribution networks discussed in this paper is underway.

6. References

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