"Front-end-ization" of the Back-End

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Abstract

The trend towards 3D stacking and advanced packaging has significantly altered the requirements for manufacturing tools in the back-end. Techniques and processes being adopted are beginning to resemble the front-end of 20 years ago but with updated and more affordable cost-of ownership capabilities. As an example, 0.5um defect inspection would have been considered a front-end requirement 20 years ago. Today TSV and advanced packaging techniques such as fine-pitch RDL are demanding 0.5u level inspection but at perhaps 10x improvement in wafer throughput and 20x improvement in COO. Other Front-end capabilities ranging from metrology to Advanced Process Control (APC) that are being adopted by the back-end will also be discussed.

Key words

Assembly, Advanced Packaging, Bumping, fine pitch Copper pillar, TSV, 3D Packaging, Stepper, Wafer Inspection, Metrology, Advanced Process Control.

I. The drive for finer pitch

The smart-phone and tablet industry has driven thinner and smaller packages which, in turn, drove the rapid adoption of fine pitch inter-connect technologies such as Copper Pillar bumping. While Cu Pillar bump diameter and height have been shrinking, an even finer pitch and width requirement is that of the Re-Distribution Layer (RDL). In the last few years, we have seen RDL pitch and width shrink from over 20 microns pitch and spacing to 10 microns pitch and spacing with customers pushing for 5x5.

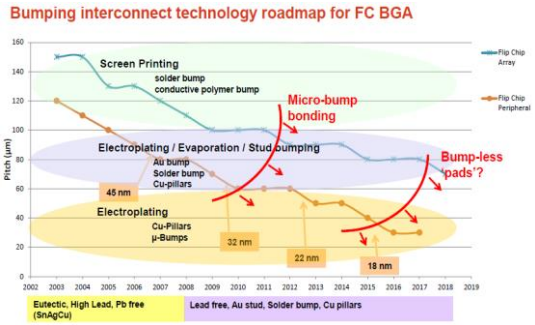


Figure 1. Change in Flip-Chip pitch and change in technology

As can be seen in Figure 1, the decreasing pitch has driven a significant change in process technology [1] from screen printing to where we are today with electro-plated Cu Pillar bumps. As the process technologies have become more sophisticated, so have the equipment and fab requirements. What may have been an acceptable environment for a squeegee paste based screen printer is not acceptable for a double sided Cu Pillar bumped wafer that is headed for a TSV stack.

Leading equipment and software technology suppliers such as Rudolph Technologies, who have only been present in the front-end as recently as 5-10 years ago, are shifting their focus to the back-end.

II. "Front-end-ization"

A. Lithography

Although "Front-end-ization" is not an actual word, anything can be "verb-ified". Typical back-end interconnect technologies went through such a "Front-end-ization process". The early years of bumping used screen printing

as the primary deposition technology. As the pitch continued to shrink and the use of photo-lithography combined with alternative metal deposition techniques such as electroplating was adopted, full-field contact/proximity aligners were used to pattern the wafers. Issues with using aligners for 300mm wafers in advanced packaging [2] are well documented – run-out, in ability to accommodate wafer warpage, pitch limitations, mask cost, sidewall angle, aspect ratio and resolution. As the industry has moved on to the use of steppers in advanced packaging, today, even the 1X stepper technology is approaching its limits and 2X steppers are being adopted. Advanced packaging technologies such as CU Pillar with the increased level of metallization on one side or state-of-the-art embedded die packaging approaches such as the Epoxy mold compound based Embedded wafer-level Ball Grid Array (eWLB) can exhibit severe wafer warp as high as +/-6 mm[3]. Increased Depth of Focus (DOF) and working distance are important to achieve steep side walls and CD uniformity across the wafer. 2X stepper technology like the Rudolph JetStep system offers past Front-end capabilities to today's Back-end packaging and interconnect applications.

	2X Stepper	***1X Stepper***
Working Distance	17mm	2mm
Depth of Focus @ 2um	+/- 15um	+/- 5um
Depth of Focus @15 um	+/- 80um	~ +/- 10um
# of steps (300mm wfr)	28	44
Printable Field Size	52 x 66mm	26 x 68mm
~Throughput (750mJ/cm^2)	83 wph	66 wph

B. Closed loop Lithography

The Front-end has deployed techniques such as closed loop lithography to improve Cpk (process capability index) for several years. After exposure and resist development, metrology tools perform CD (Critical Dimension) and overlay metrology across the wafer. This information is fed back to the stepper through a software package that incorporates Run-to-Run Control (R2R), a subset of well known Front-end Automated Process Control (APC) techniques. R2R software tweaks the recipe settings for the next lot. Then the next lot is exposed and goes to the same cycle of metrology and R2R. The net result is a lot tighter Cpk of key parameters such as Overlay and CD variation across wafer.

Figure 2. Closed loop metrology in Advanced Packaging

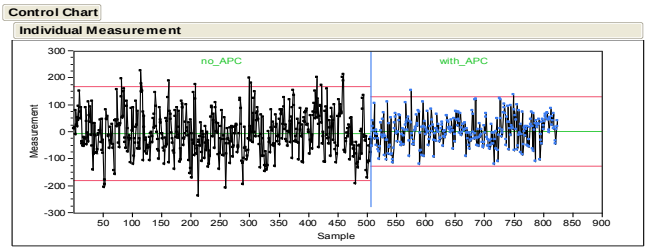


Figure 3. Cpk improvement after implementing R2R

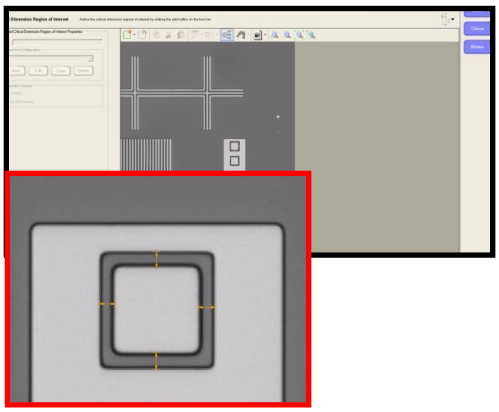
Figure 3 shows the improvement in CD Control across a wafer after implementing R2R.

This used to be the domain of Front-end only. Now this closed loop metrology is also becoming commonplace for Back-end applications. A possible setup is a Macro Inspection system such as the NSX 320 from Rudolph combined with the matching Process Works R2R software.

C. Inspection

Measurements of CD or overlay in the Front-end required a dedicated system. In the Back-end, the first implementation of CD and Overlay measurements were performed on a microscope. Today macro inspection systems such as the NSX 320 from Rudolph are deployed at various process points up and down a typical Cu Pillar bump line, all the way from post-develop to post-etch and outgoing QA. These systems are typically equipped with lenses that have magnifications ranging from 10um resolution to 0.5um. Optional 50X objectives have been deployed to provide resolution down to 0.2um. With these lenses, measurement accuracy of 80nm and repeatability of 40nm 3 sigma is

possible. Back-end fabs have begun to integrate CD metrology and Overlay metrology using the already deployed NSX 320 with very little impact to capital budget and saving valuable floor space by avoiding a microscope.



Wafer 15 Count	Average Measure
1	5.0922
2	5.1457
3	5.0828
4	5.202
5	5.2031
Ave	5.14516
Std Dev	0.057623
Repeat	98.88%
3*Std Dev	0.172869

Wafer 14 Count	Average Measure
1	4.0616
2	4.0676
3	4.0657
4	4.0685
5	4.0095
Ave	4.05458
Std Dev	0.02534
Repeat	99.38%
3*Std Dev	0.076019

Figure 3. Box in box metrology at 0.5um resolution

The impact on capacity is marginal. In one study of a 300mm
wafer with 5 measurement points/die, the entire wafer and all dies took approximately 148 secs.

D. Metal Films Metrology

High end metal films metrology systems have been commonplace in front-end applications for several years now. The pico-second ultrasonic laser reflection based Metapulse from Rudolph has become the standard in all leading edge fabs for measurement of High-K metal stacks in the Front End-of-line (FEOL) and Cu CMP in the Back End-of-Line (BEOL). As UBM (Under Bump Metalization) stacks are growing increasingly complex, and as their overall thickness is gaining on importance, , determining the thickness of each metal layer becomes key. Individual films have critical roles to play in successfully packaging multiple devices

- Barrier to diffusion
- Electromigration
- Mechanical integrity
- Resistivity

Table 1 shows importance of each metal layer.

UBM and RDL are key process steps not only for Cu Pillar but also TSV. Figure 4 shows the results of measuring Au and Pd profile across the wafer. As leading semiconductor operations develop their UBM and RDL processes, Front-end metrology techniques are increasingly important to ensure that key metal films have the desired thickness and uniformity across the wafer.

Film	Use Case	UBM	RDL	Bump
Ti, TiW	Barrier layer under Cu pad to prevent diffusion into pad and proper adhesion for PVD process	√	√	
Al,Cu	Conductive pad or RDL trace (Cu). Typically EP or Sputter	√	√	√
Ni, NiV	Barrier to prevent diffusion into Cu pad	√		√
Pd	Typically applied over Ni. Pd acts as a protective layer preventing oxidation of Ni either from the ambient or during packaging and assembly operations	√		√
Au	Bump/pillar surface finish. Typically over Ni, protects Ni from oxidation, and if solder is subsequently applied; gold diffuses into the solder during reflow process.	√		√
SnAg	Tin Silver Solder cap over Cu pillar bump			√

Table 1. Metal layers in a leading UBM stack and their function

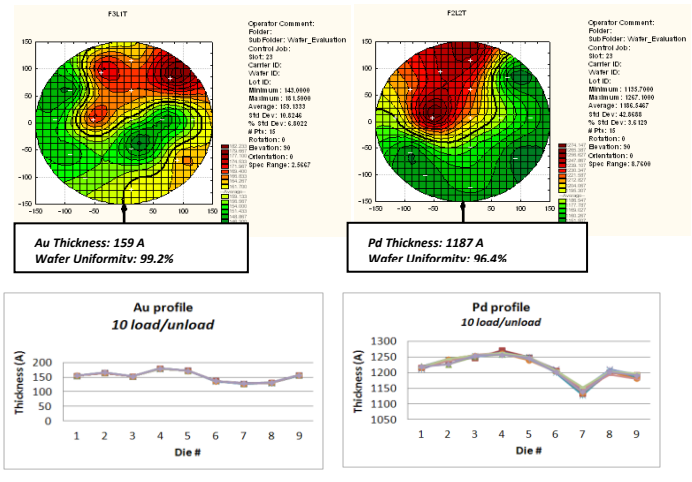


Figure 4. Under Bump metallization- Within wafer Uniformity profile

E. Automated Process Control (APC)

Two key technologies that have been deployed in the Front-end under the umbrella of APC are R2R and Fault-detection and Classification (FDC). Think of Run-to-run as cruise control for your car and FDC as indicators that, while you may be maintaining speed, your tire pressure is running very low. The use of R2R in the Back-end in conjunction with steppers has been illustrated. Increasingly fabless companies are mandating that bump and wafer-level Chip scale package (WLCSP) lines deploy FDC across the board for all equipment.

One key tool that was targeted for FDC was saw. For WLCSP based on wafers at nodes below 45nm using low-K, issues arise at singulation due to de-lamination and cracking of the Inner-layer Dielectric (ILD). Singulation of WLCSP is a two-step process – laser grooving followed by saw.

The saw system has a number of key parameters that determine its impact on the device. Using FDC to trigger these parameters and then analyze the inter-relationship between each variable allows for signals to be generated and timely interdiction in the event a process may go awry.

Table 2 shows the key parameters and how they affect the saw process. The key parameters act as input variables to monitor. Output being detection of an event which potentially could need interdiction.

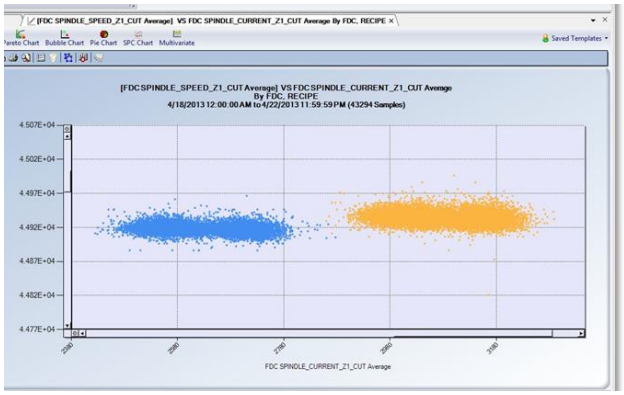


Figure 5. Plot of spindle speed vs. spindle current of two tools running identical recipe. One on right runs at slightly higher speed at much higher current.

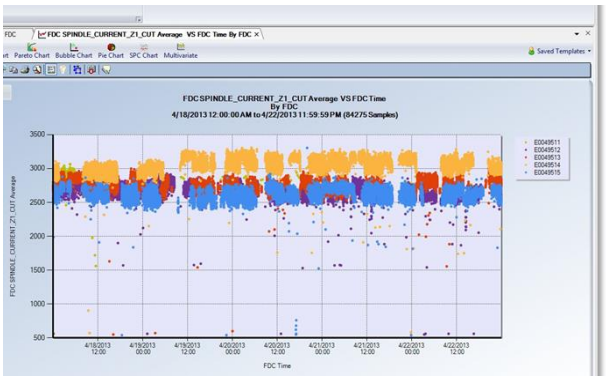


Figure 6. Comparison of tool behavior. Orange chart signals outliers.

Sensor	Impact
Spindle Speed & Current	Typically control speed by adjusting current. Speed is typically designed with the blade type (grit size and concentration, blade length, bevel) for optimal blade wear. Determines removal rates, but anomalies will create defects (chipping) or breakage (blade).
Table Speed	With spindle rotation determines removal rates and uniformity. High speed will induce chipping, but low speed reduces throughput.
Vacuum	Controls holding of wafer in position. Poor vacuum will easily lead to "flying die" (especially under high water pressure). Too much vacuum may cause wafer breakage.
Water and Air Pressure	Controls the wafer and blade cooling and debris removal on the cutting table and around the blade (jets in shower, spray, left and right side of blade). Determines the final defect level in the spin table.
Blade Aging (mm or lines)	Blades have a limited life and will have higher chipping or possibly incomplete cuts if ran beyond specifications including periodic blade dressing (sharpening) and checks (BBD and NCS checks).

Table 2. Key saw parameters and impact to saw process

Displayed in Figure 5 is the Plot of spindle speed vs. spindle current of two tools running identical recipe. In Figure we see a comparison of tool behavior. Orange chart signals outliers. One on right runs at slightly higher speed at much higher current.. FDC can reveal conditions such as "tool out of operating range" for each piece of equipment and in comparison to others. FDC,a proven Front-end technique, enables early detection of tools that are not operating optimally and are likely to either generate defective dies or otherwise negatively impact the process.

III. Conclusion

All of the Front-end techniques are inexorably making their way into the Back-end. Reduction Steppers, macro inspection equipment for Overlay and CD control as well as advanced Metrology and APC techniques are being used in leading edge Advanced Packaging fabs to produce high yields, minimize scrap and prevent outlying defects from leaving the fab.

Acknowledgment

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