On the Origins, Status, and Future of Flip Chip & Wafer Level Packaging

Alan Huffman[1], Philip Garrou[2]
[1]RTI International, 3040 Cornwallis Rd, RTP, NC, 27709 (919)-248-9216; huffman@rti.org;
[2]Microelectronic Consultants of NC, RTP, NC (919)-248-9261; philgarrou@att.net

Abstract

As IC scaling continues to shrink transistors, the increased number of circuits per chip requires more I/O per unit area (Rent's rule). High I/O count, the need for smaller form factors and the need for better electrical performance drove the technological change towards die being interconnected (assembled) by area array techniques. This review will examine this evolution from die wire bonded on lead frames to flip chip die in wafer level or area array packages and discuss emerging technologies such as copper pillar bumps, fan out packaging, integrated passives, and 3D integration..

Key words: flip chip, wafer level packaging, 3D integration

Introduction

Flip chip assembly describes the face-down electrical interconnection of electronic components onto chip carriers, PWBs or other substrates, by means of conductive bumps, such as solder balls, between the device and the substrate.

Flip chip (FC) is one of three common bonding techniques, along with wire bonding (WB) and tape automated bonding (TAB). When these techniques are used to mount a chip directly on a substrate this is referred to as direct chip attach (DCA). When that substrate is a printed wiring board or glass or flex, the resulting structures are called chip-on-board (COB), chip-on-glass (COG), chip-on-flex (COF) respectively. When bumped die are first mounted on an interposer (package) to fan out interconnect to courser pitch and then mounted on a PWB they are called flip chip in package (FCIP), or more clearly described as an exact package with acronyms like FC-BGA. To delineate more clearly which type of bonding is used to create a COB structure, flip chip on board can also be referred to as F-COB or FCOB. [1, 2]

Ideally, the device package structure should be small and add as little additional interconnect length as possible (to minimize electrical performance degradation). Flip chip technology allows improvements to be made on both of these criteria, enabling smaller overall package sizes, area array interconnect footprint, and improved electrical performance.

A Historical Look at Flip Chip Evolution

The concept of interconnecting a chip in a face down or "flip chip" orientation can be traced back to IBM's introduction of their system 360 mainframe computer in 1964 [3]. The original concept employed solder coated copper balls placed between the chip pads and the corresponding pads on the circuitized substrate [4]. In 1969 controlled collapse chip connection (C-4) replaced copper balls with solder balls. The surface tension of the molten solder, confined to a solder wettable pad area by glass passivation, served both to align the chip on the substrate and maintain the proper standoff for reliability [5].

Solder bumping in the next two decades was mainly confined to high end main frame computer companies like IBM, NEC, Fujitsu and Hitachi because it was limited to ceramic packaging due to the mismatch between the coefficient of thermal expansion (CTE) of Si and PWB [3 ppm/°C vs. 16 ppm/°C (FR4)]. The solder joints are under severe stress during each temperature cycle which can induce solder cracks after a few hundred temperature cycles.

In 1987 Nakano of Hitachi revealed that flip chip die mounted in ceramic packages had much better reliability when the area between the die and the substrate (surrounding the solder balls) was encapsulated with an epoxy "underfill" [6]. In 1992, Tsukada of IBM Japan published reports that FC chips could be reliably attached directly to PWB laminate if the chips were similarly underfilled [7]. This announcement drove the packaging community to take a hard look at flip chip technology in a broader application space. The development drew significant attention from those interested in miniaturizing cell phones, pagers, camcorders and other portable products.

In the mid 1990's Motorola became a major advocate for flip chip on laminate for consumer applications [8]. Production of the Motorola pen pager in 1993 used FCOB [9]. By 1996 Motorola had introduced FCOB into the StarTac handset. In 1996 it was estimated that ~ 500MM FCOB units were being produced worldwide [10].

In the same timeframe, lower cost bumping processes were being developed at Unitive, Inc. (spin out of the Microelectronics Center of NC) [11-12] and FCT (Flip Chip Technologies) the joint venture of Delco and K&S. [13]. Their developments of lower cost UBMs (FCT - Al/Ni-V/Cu; Unitive - Ti/Cu/Ni) and solder deposition technologies (FCT - stencil printing; Unitive - plating), and use of repassivation and redistribution, in combination with Tsukada's revelation that bumping could be used reliably on laminate, opened the door for widespread acceptance of this high performance interconnection technology.

At first there was some resistance to accept these new technologies due to IBMs insistence that reliable C4 could only be achieved with the phased Cr/Cu/Au UBM and evaporated high lead solder (97/3), i.e. their standard process [14] . These concerns were alleviated for good in 1999 when Intel announced the use of Ti/Ni UBM with 97/3 Pb/Sn for their microprocessor packaging technology [15].

The FCT and Unitive technologies were licensed by the key assembly houses and mid-size IC houses as they initiated production in the early 2000's including: ASE, Amkor, STATSChipPAC, SPIL, National Semiconductor, and others. Most of the world's production is done today using these or similar technologies. In fact, evaporating phased Cr/Cu and high lead solder through a molybdenum mask did not scale to 300 mm, so not even IBM is using such technology today on 300 mm wafers.

Advantages and Disadvantages of Flip Chip

Flip chip technology brings with it a number of unique advantages and disadvantages. Some of the notable advantages are:

Electrical performance - Flip chip delivers the best electrical performance of all commonly available assembly techniques. FC (vs. WB) reduces the resistance, inductance and capacitance of the connection. This is shown at 2.4 GHz (wireless) in Fig. 1.

In addition, power distribution is becoming a significant electrical performance criterion [16]. On a WB device, power is distributed to the center of the die on a long bus causing significant IR drop (voltage drop due to resistance in the line), whereas with flip chip, power can be distributed directly to the center of the die minimizing IR drop.

I/O density - Flip chip gives the greatest I/O connection density. While WB connections are limited to the perimeter of the die, driving die sizes up as the number of connections increases, FC, an area array assembly technique, uses the whole area of the die and thus can accommodate many more connection pads at the same or significantly reduced pitch. This was never more apparent than when Intel's Pentium P5 could not take advantage of a 0.5 um to 0.35 um CMOS technology shrink because the chip dimensions had to be maintained to obtain the required WB I/O pitch. This is depicted in Fig. 2 [17].

Fig. 1: Electrical Performance of FC vs. WB at 2.4 GHz [16]

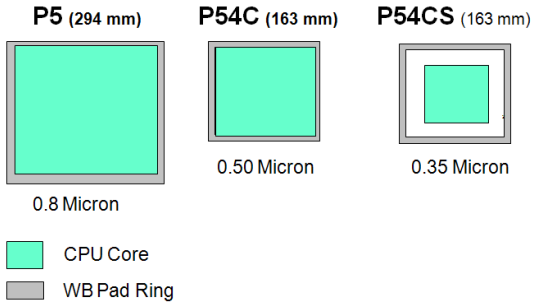

Fig. 2: Intel P5 Shrinks

Size - Eliminating package lead frames and/or WBs reduces the required board area by up to 95% and requires far less height and weight. FCOB is the simplest minimal package as shown in Fig. 3.

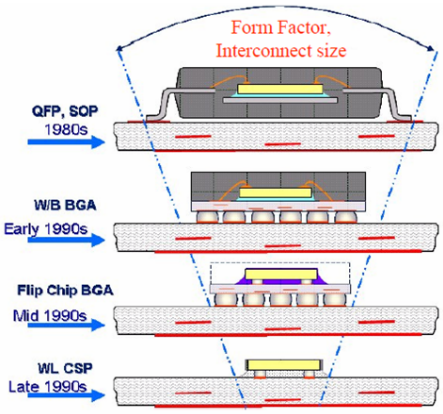

Fig. 3: Size reduction achieved with FCOB or WLP (Ref: Infineon)

Cost – In high volume production, flip chip can actually be the lowest cost interconnection. Thus, its use in cost-sensitive (i.e. automotive) and consumer applications (i.e. cell phones).

Cost reduction is traditionally achieved in the IC industry by (1) increasing wafer size which results in more ICs per wafer, and (2) decreasing feature size. Normally, even with the increased cost of the equipment, the increased production capacity more than offsets this cost. This is ***not*** true for traditional IC packaging, because as number of ICs or dies per wafer increases, one must linearly increase the number of wire bonders, molding machines, testers, and handlers. Since wafer-level packaging is fabricated on the wafer, it realizes the same economic advantages as ICs. WLP has been widely adopted as a low cost, high density packaging solution [25]. Fig. 4 shows typical low pin count WLP applications.

Thermal performance – Flip chip provides enhanced thermal performance over WB due to the increased number of joints and their closer proximity to the device. This also leaves the back of the chips free for attachment to heat sinks for further thermal performance improvements.

In addition to these advantages over other interconnection methods, flip chip has also created some specific issues that should be noted.

Thermal Fatigue – One of the limitations of FC is how large of a chip can be bonded and still maintain structural and electrical integrity over a lifetime of thermal cycling. The CTE difference between the chip and the substrate causes a shear stress to be exerted on each pad during a thermal excursion. This stress is largest for connections furthest away from the center of the chip, (maximum distance from neutral point [DNP]). Reliability can be improved by removing I/O at the corners of a device, which are under the most strain. Strain on the solder joints can also be lowered by increasing the spacing between the chip pad and the substrate pad, creating a larger gap by using larger solder balls. Thermal fatigue was a significant impediment to the widespread adoption of FC until the influence of underfill was discovered in the late 1980's (see below).

Electromigration – Electromigration is the physical movement of solder material as result of current flow, device junction temperature, and time [18]. HTOL testing (high temp operating lifetime) is done to determine reliability under high (application specific) currents. Control of solder alloy composition can be used to minimize electromigration. For instance, it is known that the SnPbCu near-eutectic alloy minimizes electromigration and improves reliability by a factor of 3 over SnPb [19]. Lead-free solders such as SnAg (3.5%) and SnAg(3.5%)Cu(0.6%) are also more resistant to electromigration, although they have higher reflow temperatures.

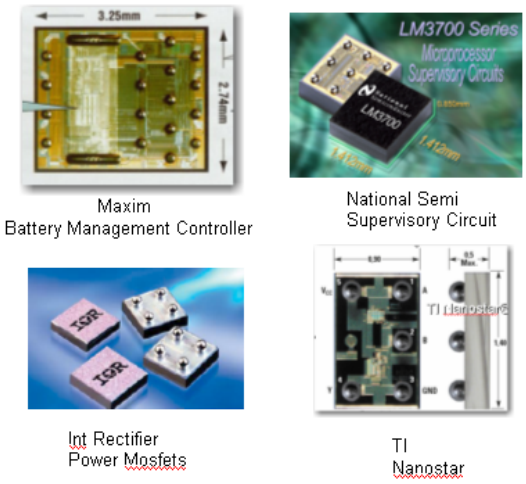

Fig.4: Typical WLP Applications

Matching I/O/ Pitch – Incorporating a FC onto a PWB circuit requires matching the chip I/O pitch with the pitch of the PWB pads. Standard PWB pad pitch is typically 500 um or larger while standard FC pitch is typically 150 or less. This "interconnect gap" is depicted in Fig. 5.

The options are (a), to use a high density interconnect (HDI) as the substrate or (b), to use an interposer of the same high density laminate to fan out the pitch to the pitch on a standard PWB. The latter, which is flip chip in package (FCIP) or BGA, is usually the preferable low cost option since it uses far less of the expensive HDI laminate. This extra packaging certainly degrades the electrical performance, but less so than packaging with lead frames and/or WBs. BGA is typically chosen as the packaging format as shown in Fig. 6. In any circuit

design, this trade off of required chip I/O vs. fan-out package cost vs. board pitch/board cost needs to be examined and optimized.

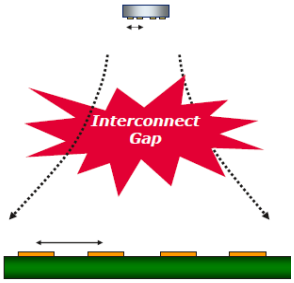

Fig. 5: The Chip / PWB Interconnect Gap (Infineon)

For low I/O devices, the bump pitch can be fabricated or redistributed (see below) to a 500 um or more pitch for DCA. In order to avoid the stress-related failures that would develop from thermal cycling of 125 um or smaller diameter balls, the solution is to place larger individual balls on the pads (250 um+ diameter). For small chips (5-6 mm or less), these chips can be surface mounted without underfill, providing additional cost savings. This concept was first proposed by Sandia Labs in 1994 [20,21]. The first commercialization of such a product was by the Delco/K&S start-up Flip Chip Technologies (FCT) which introduced the UltraCSP™ in 1998 [22, 23]. Soon afterward Unitive came out with their equivalent Xtreme™ CSP [24].

Over time the nomenclature for such structures changed from mini-BGA, to wafer level chip scale package (WL-CSP), to the simpler "wafer level package"or WLP. WLP describes a package which is fully fabricated on the wafer before dice and subsequent surface mount. WLP was reviewed in 2000 [25, 26].

Repassivation

In repassivation (Fig. 7) a polymer is applied to the wafer to serve as a stress buffer layer, a planarizing medium, and a final passivation layer. This technology is used when the solder bump is larger than the final metal pad (as is the case for WLP) and serves to buffer the stress of the bump from the brittle nitride or oxynitride passivation. As previously noted, larger (taller) bumps show increased reliability.

Redistribution

One impediment to the use of FC was/is the lack of area array designed chips. This was addressed in the early 1990's by the development of redistribution layer (RDL) technology.

Redistribution is defined by the addition of metal and dielectric layers onto the surface of the wafer to re-route the I/O layout into a new, larger pitch footprint. Redistribution is shown in cross section in Fig. 8. Such redistribution requires thin film polymers (secondary passivation) and metallization to reroute the peripheral pads to an area array configuration and under bump metallurgy (UBM) to create reliable solder joints. The rerouting metallization is typically aluminum or copper.

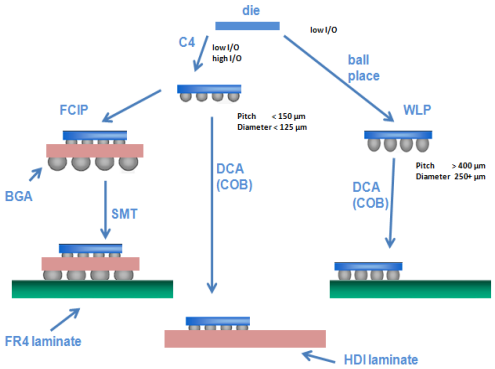

Fig. 6: Solder Ball Attachment Options

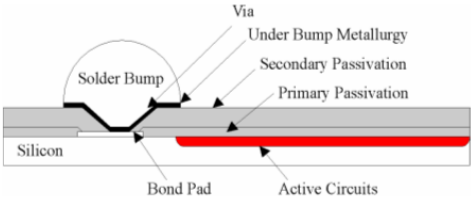

Fig 7: Repassivation

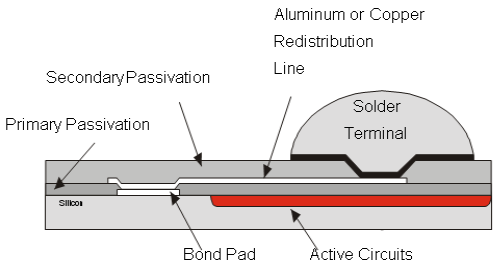

Fig. 8: Redistribution

The redistribution trace can be fabricated directly on the primary passivation (SiN or SiON) (as shown in Fig. 8) or can be routed over a layer of secondary polymer passivation when it is necessary to add compliancy to the system for reliability considerations. These are typically called bump on nitride (BoN) and bump on polymer (BoP), respectively. Redistribution and repassivation technology also provides environmental and mechanical protection.

Underfill

After the Tsukada announcement that underfill mechanically couples the chip to substrate to restrain movement between the two interfaces, many years of study went into determining optimum polymer properties for underfill. Fraunhofer IZM – TU Berlin was the first to identify that the CTE of the underfill should be matched to that of the joint (~ 25 ppm/°C for eutectic solder) and not the chip or the substrate for maximum reliability [27]. Underfill has been found to significantly decrease the effect of CTE mismatch, as shown in Fig. 9 [28].

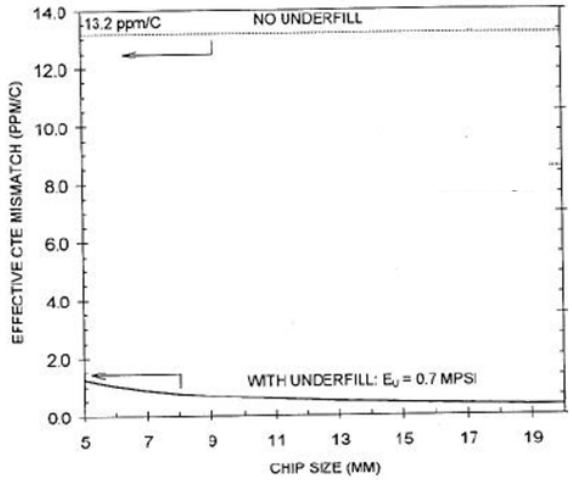

Fig. 9: Underfill Effect on CTE Mismatch [28]

Initial capillary flow underfill showed high viscosity, slow flow, and curing times of ~ 6 hrs. Faster flow and faster cure materials were quickly developed by a number of suppliers [29]. Pre-applied underfill (also called "no flow") where fluxing, solder reflow, and underfill curing occur in the same process sequence, requires formulations that are stable at solder reflow temperatures and are then cured at higher temperatures [30]. Although much R&D has occurred on such materials they have not yet been widely adopted in commercial production, mainly because they are not typically filled with CTE matching materials (i.e. silica) and therefore have CTEs that do not match the joint.

Molded underfill (MUF) uses epoxy molding compound (EMC) and transfer molding to fill the flip chip gaps and encapsulate the chip at the same time. A 4X increase in throughput vs. capillary underfilling was reported [31]. Molding can also be done at the wafer level [32].

Although CSP assemblers would rather not underfill, since this process takes time and thus decreases throughput, many handheld devices are underfilled as an extra precaution because some WLP / PWB combinations cause twisting during thermal cycling which causes solder failure. The recent development of fast cure, no flow underfill materials and full wafer molding technology may make these more attractive options in the future.

60% increases in thermal cycle lifetime have been reported when the solder joint is partially encapsulated by technologies such as the FCT "Polymer Collar" which supports the bump at its base [33], or the Lord Corp. wafer level solder brace technology shown in Fig. 10 [34].

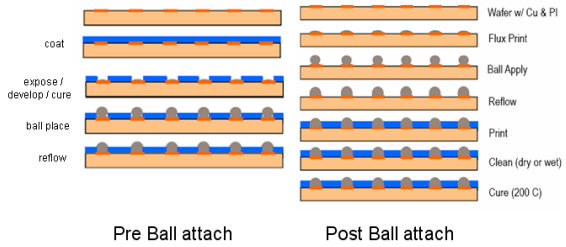

Fig. 10: Lord Corp. Solder Brace Technology

Future Developments for WLP Technology

Although WLP is now considered to be a well-developed and mature technology, there are a number of areas for further development currently being pursued by the industry. Cost reduction is always a predominant driving factor in the development of new WLP technologies, but the development of new approaches for advanced and next generation applications remains important as well.

Copper Pillar technology

Copper pillar technology replaces the traditional collapsible solder bump with a cylindrical copper connection with a solder cap, as shown in Fig. 11. Copper pillar bumps are more rigid and allow assembly with a small solder volume on top of the pillars, which has several significant benefits. First, the standoff gap can be kept high, even at very fine pitch. The smaller solder volume prevents excessive spread out on wettable surfaces, even without a solder mask barrier. Additionally, the non-collapsible nature of the copper bump allows the pitch to be reduced, providing higher I/O density. Some other advantages of copper pillar bumps include:

- Greater conductivity (25X > solder balls)
- Lower electrical resistance, lower inductance
- Lower thermal resistance (3X better than with solder balls)
- Better resistance to electromigration
- Smaller chip size due to reduced pitch

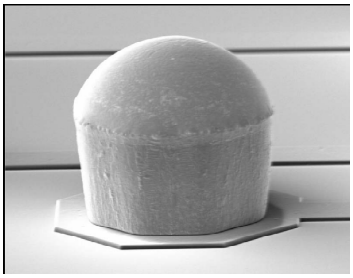

Fig. 11: Cu pillar bump with SnAg solder cap (40 µm pillar height / 25 µm cap height) (IME)

Copper pillar technology is currently used commercially in high performance devices such as microprocessors (Intel introduced copper pillar bumps in 2006 in their 65-nm Presler and Yonah microprocessors [35]) and they are increasingly being seen in RF SiPs (system in package). Cost differential between copper pillars and solder bumps is typically 20-30% depending on volume. The technology has been licensed to several large global assembly houses i.e. Amkor by Avanpack Solutions (APS) [36].

Fan Out Packaging

As die sizes shrink with each CMOS node, the amount of chip area available for bump I/Os is decreasing, but there is still the need to preserve both bump size and count for reliability and to maintain package footprint. One solution, fan-out packaging, relies on embedding singulated die in molding compound and then using repassivation and redistribution processes to form the bump array over the Si and mold compound (Fig. 12). Processes such as Freescale's Redistributed Chip Package (RCP) [37] and Infineon's Embedded Wafer Level BGA (eWLB) [38] are two examples that have recently been receiving significant industry attention.

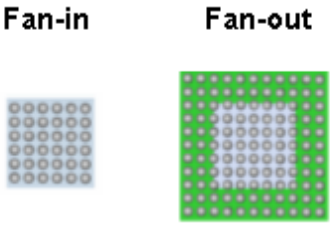

Fig. 12: Fan-in vs. Fan-out Packaging

In the eWLB process a carrier wafer is laminated to dicing tape and KGD are placed face down to create a "reconfigured wafer". This wafer is then compression molded to encapsulate it and the wafer carrier and tape are removed. The molding compound is used to carry the fan out area and to protect the chip backside. A redistribution layer is created on the now exposed die faces, solder balls are placed, and the die singulated. This process sequence is shown in Fig. 13.

In 2008 Infineon licensed eWLB to ST Microelectronics and STATS ChipPAC. ASE and Amkor are actively engaged in fan out packaging as well. The main challenges that eWLB faces include: co-planarity, warpage, die movement, film wrinkle, voids, incomplete fill and mold bleeding [39].

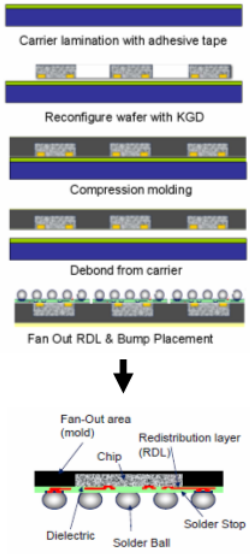

Fig. 13: Process Sequence for Fan-Out Packaging

Lower Cost WLP Technologies

In some cases, it is the cost and not the reliability of the WLP that is the issue. In order to reduce the cost of WLP, companies such as Amkor have developed new WLP structures that reduce the number of redistribution and repassivation layers, as well as changing the UBM structures. These solutions provide a reduced fabrication cost while maintaining a reduced, but acceptable, level of reliability [40].

Passive Integration

Passive functions can be fabricated directly on a completed wafer during thin film redistribution by thin film processing [41]. A schematic cross-section of a representative thin-film integrated passive process is presented in Fig. 14. Such processes offer a range of resistor, capacitor, and inductor components, plus a low inductance ground plane structure and transmission line routing to interconnect the passive components.

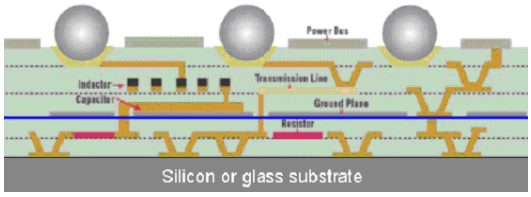

Fig. 14: WLP passive integration (IMEC)

3D Integration Technologies

3D integration represents the next generation of interconnect and integration technology, and relies on stacking devices and making connections between them through the use of through silicon vias (TSVs). This area has been heavily investigated for the last several years, with a number of basic process elements being developed and demonstrated by several institutions [42-44].

Fig. 15 illustrates the concepts of 3D integration, with subassemblies of hetero- and homogeneous devices connected through TSVs.

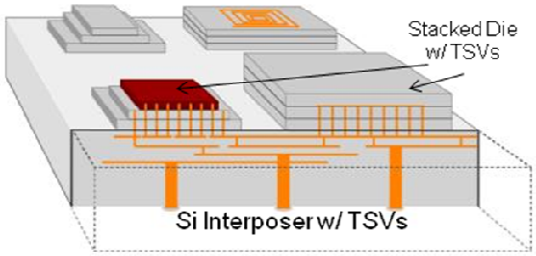

Fig. 15: Example of a 3D integrated module (RTI)

Some approaches to 3D integration utilize the same basic process ideas as WLP and flip chip; area array interconnects (many times with Cu-based bump interconnects as small as 5µm diameter [45]), repassivation and redistribution for signal routing, and wafer thinning (to lessen processing issues related to TSV diameter and depth). Other aspects of 3D integration present new problems to solve. For example, the assembly of 3D integrated systems typically requires thermocompression processes which are much slower throughput than solder reflow processes used for WLP assembly.

The combination of WLP and 3D integration technologies brings about an interesting construct: the silicon interposer. Used as an integration platform, Si interposers provide a CTE-matched substrate on which to assemble devices in close proximity with support for high I/O densities and fine pitch routing. Compared with state of the art organic laminate or ceramic substrates, Si interposers can provide finer feature dimensions for vias and lines. When TSV structures are integrated into the Si substrate, a so-called 2.5D integration solution is possible, providing significant advantages over 2D packaging strategies. Such structures are already being demonstrated for advanced applications by companies such as Shinko [46].

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