Advances in Wafer Level Processing and Integration for CIS Module Manufacturing

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Abstract

This article presents the advances in wafer-level processing and integration techniques for CMOS image sensor module manufacturing. CMOS image sensors gave birth to the low-cost, high-volume camera phone market and are being adopted for various high-end applications. The backside illumination technique has significant advantages over the front-side illumination due to separation of the optical path from the metal interconnects. Wafer bonding plays a key role in manufacturing backside illuminated sensors. The cost-effective integration of miniaturized cameras in various handheld devices becomes realized through the introduction of CMOS image sensor modules or camera modules manufactured with wafer-level processing and integration techniques. We developed various technologies enabling wafer-level processing and integration, such as (a) wafer-to-wafer permanent bonding with oxide or polymer layers for manufacturing backside illuminated sensor wafers, (b) wafer-level lens molding and stacking based on UV imprint lithography for making wafer-level optics, (c) conformal coating of various photoresists within high aspect ratio through-silicon vias, and (d) advanced backside lithography for various metallization processes in wafer-level packaging. Those techniques pave the way to the future growth of the digital imaging industry by improving the electrical and optical aspects of devices as well as the module manufacturability.

Key words: CIS module, BSI, wafer-level camera, wafer-level optics, wafer-level processing and integration

Introduction

Image sensors have come a long way since the first introduction of the charge-coupled device (CCD) sensor technology in the 1990's and made a big jump in the 2000's with the introduction of the CMOS image sensor (CIS) technology. CMOS sensors are faster, smaller, and cheaper than CCD sensors because they are more integrated and power-efficient, and manufactured in existing semiconductor chip plants. CMOS sensors were initially used for low-end cameras but recent improvements have made them more popular in various high-end cameras. CIS gave birth to the low-cost, high-volume camera phone market and CIS revenues have surpassed CCD image sensor's since 2007 [1].

When it comes to illumination approaches, backside illumination (BSI) has significant advantages over front-side illumination (FSI) on the ground that BSI brings light in through the thinned backside of the silicon substrate to the photosensitive area [1,2]. As shown in Fig. 1, with the conventional FSI approach the amount of light reaching the photosensitive area is significantly reduced by the multiple wiring layers that convert photons into electrons, whereas the BSI technique separates the optical path from the multi-layer interconnects, thus eliminating the influence of the CMOS metal layers on the light path. The enabler for this vertical separation is thinning the backside of the silicon wafer on which the CIS devices are fabricated so the light can impinge on the sensor pixels with minimum attenuation by the silicon.

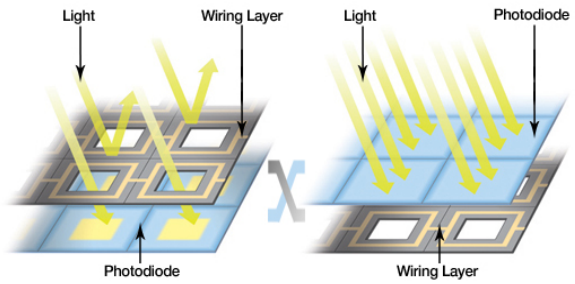


Figure 1. Comparison of FSI and BSI structures (source: Fujifilm).

Before the silicon wafer is thinned to the appropriate thickness, the front-side of the CIS wafer must be bonded to the carrier wafer to provide a sufficient mechanical strength during and after backside thinning. As illustrated in Fig. 2, the BSI image sensor is built with the CMOS technology starting with a photodiode and subsequently building an electrical circuitry on top of it. At the end of the sensor fabrication process, the opening of the photodiode to the incoming light is needed, followed by additional process steps required for integrating color filters and lenses. Wafer bonding can provide the proper process to practically transfer the CMOS sensor flipped upside-down onto a substrate and allow substrate thinning and wafer-level sensor fabrication [2].

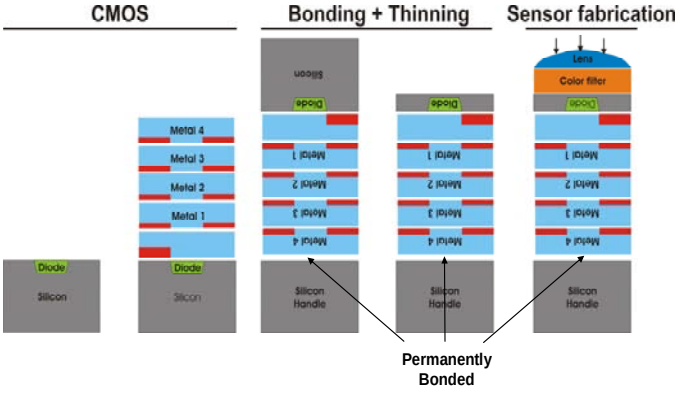
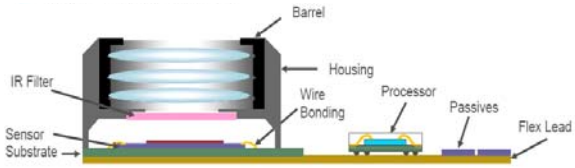


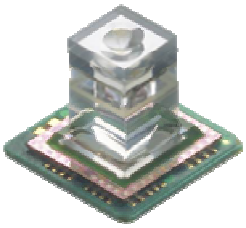
Figure 2. BSI image sensor manufacturing based on wafer bonding techniques.

Image sensor modules (or camera modules) are more than just image sensors – they are systems made up of a number of components assembled together [3]. A cost-effective integration of miniaturized cameras in cellular phones or other mobile electronics is realized through the introduction of the CIS wafer-level camera (WLC) modules manufactured with wafer-level processing and integration techniques. Besides reducing the amount of labor required, the number of components required to build the camera module is also reduced with the WLC approach. Fig. 3 compares two types of camera modules [3]. Packaging methods for those CIS modules in mobile devices are progressing from chip-on-board (COB) with wires to wafer-level chip scale packaging (WL-CSP) with bevel contacts, and finally to through-silicon via (TSV) interconnected WL-CSP.

Wafer-level camera is defined as "wafer-level manufacture of all parts of a solid state camera that are then combined at the wafer level" [4]. The final manufacturing step is wafer dicing, which frees complete and individual camera modules. However, the first generation of WLCs is not manufactured according to the methodology suggested by the above definition. Practically the optical area of an imager die is much smaller than the die area because of the other electronics each chip contains, as shown in Fig. 3(b). This results in a mismatch in population between the lens wafers and the device wafers. Consequently it is economically more favorable to make the optical components at the wafer level, dice it into individual optical stacks and then conduct die-to-wafer assembly to build camera modules [3,4]. Dicing the populated semiconductor wafer yields completed camera modules. Today wafer-to-wafer stacking of lens wafers onto CIS wafer is being developed by many of camera module manufacturers to improve the module manufacturability.



(a) conventional, assembled camera module



(b) wafer-level camera module

Figure 3. Two types of camera modules (source: Tessera).

As part of key components in the WLC, wafer-level optics (WLO) can be manufactured on transparent wafers instead of using individual molding techniques. WLO is a novel technology that is designed to meet the demands for smaller form factor, higher resolution and cost-effective pricing in the next generation of camera phones [5]. The optical components are typically fabricated with the replication method on glass wafers. The entire camera may be aligned and assembled at the wafer level, and subsequently diced to form individual camera module.

This article presents the advances in wafer-level processing and integration techniques for CIS module manufacturing. We developed various technologies enabling wafer-level processing and integration, which improve the electrical and optical

aspects of devices as well as the module manufacturability. Those technologies, paving the way to the future growth of the digital imaging industry, include (a) wafer-to-wafer permanent bonding with oxide or polymer layers for manufacturing BSI sensor wafers, (b) wafer-level lens molding and stacking based on UV imprint lithography for making WLO, (c) conformal coating of various photoresists within high aspect ratio vertical TSVs, and (d) advanced backside lithography for various metallization processes in wafer-level packaging (WLP).

Wafer-to-Wafer Permanent Bonding

In manufacturing backside illuminated image sensors a fully processed CMOS wafer is bonded to a blank carrier wafer and then back-thinned in order to open the photosensitive sensor area. The two main wafer bonding processes used for this process flow are low-temperature plasma-activated silicon oxide bonding and polymer adhesive bonding [2]. For low-temperature plasma-activated silicon oxide bonding, a CMOS wafer has to be planarized to meet the requirements of fusion bonding. The overall process flow, depicted in Fig. 4, comprises CMOS wafer processing, planarization, plasma activation, wafer bonding, sensor fabrication and CIS module manufacturing with lens stacking.

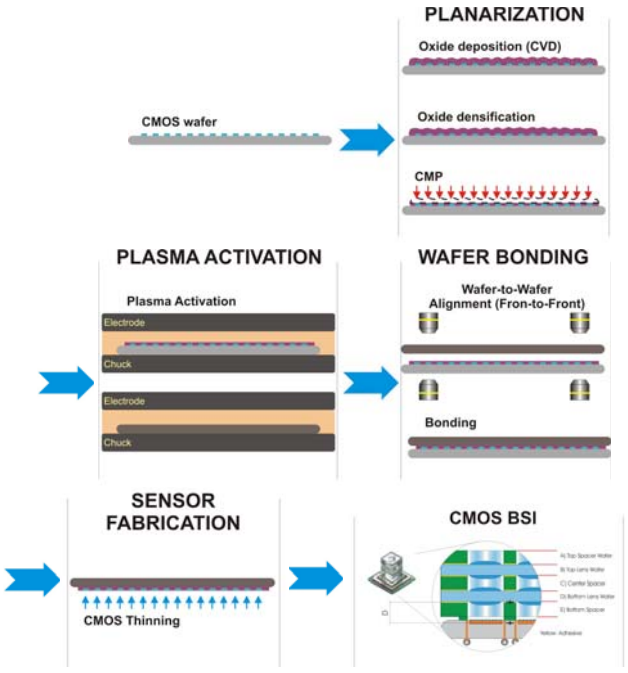


Figure 4. BSI CIS fabrication process flow using low-temperature plasma-activated silicon oxide bonding.

In order to obtain a flat surface for bonding, the CMOS wafer is first planarized using silicon oxide deposition (e.g., plasma-enhanced chemical vapor deposition (PECVD)) followed by oxide layer densification through thermal annealing. This step is for removing residual gas trapped in the oxide layer during the PECVD process. Without this step the trapped gas will usually accumulate at the interface causing large voids at the bonded interface. After densification the PECVD oxide layer needs to be polished using a conventional chemical mechanical polishing process.

After CMOS planarization the wafers are plasma activated and aligned using either edge-to-edge mechanical alignment (max. accuracy: ±50 µm) or optical alignment (max. accuracy: < 1 µm) depending upon alignment specifications. Wafers are typically brought into contact at room temperature for spontaneous bonding and then thermally annealed in a temperate range between 200 ºC and 400 ºC [6]. After the wafer bonding step the initial CMOS substrate is back-thinned, then the entire sensor structure is completed and then the camera module is built using wafer-level processing such as wafer-level packaging and lens stacking.

The second type of process used for this application is polymer adhesive bonding, where the planarization of the CMOS wafer is accomplished by a polymer bonding layer (no plasma activation is required). This bonding method brings the major advantage of high tolerance to CMOS surface topography as well as to particle contamination. It is known that polymer materials can fill gaps, compensate flatness variations and even incorporate particles with diameters in the range of the polymer layer thickness. The process flow is simplified in this case compared to the oxide bonding approach by replacing the oxide planarization with a polymer spin-coating or spray-coating process. However, with adhesive bonding there can be such risks as wafer backside contamination during coating process, alignment precision deterioration due to polymer layer compression, and material reliability concerns during subsequent processes [2,6]. A camera module can be built using the same wafer-level processes such as wafer-level packaging and lens stacking.

In some cases a cover-glass wafer with patterned cavity wall can be stacked onto the device wafer prior to backside TSV and WLP processes as illustrated in Fig. 5. The cover-glass wafer has mainly two functions; (i) working as a window for image processing and (ii) protecting an image sensing area from particles during backside TSV and WLP processes [7]. In order to stack the cover-glass wafer onto the device wafer polymer adhesive bonding is performed typically with a thermally-curable

adhesive layer, where the cavity wall on the glass surface may or may not be comprised of the same material as the adhesive material that enables the bonds.

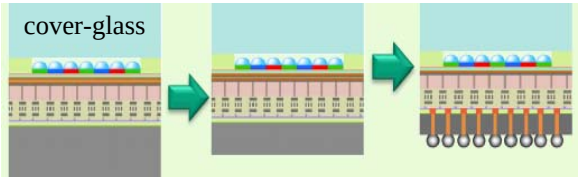


Figure 5. Backside processing with the cover-glass stacked onto the device wafer (source: Yole Development).

Wafer-Level Lens Molding and Stacking

Wafer-level optics consists simply of molding lenses on transparent wafers and stacking those lens wafers on the CIS wafer to create an optics system even though the actual execution of this process is very complex. The major steps of this process are (i) design of the optics, (ii) fabrication of the molds that form the lenses, (iii) molding of the lenses on the glass wafer, and (iv) alignment and bonding of the lens and spacer wafers to the CIS wafer. Conventional master stamp fabrication processes such as diamond or micro-milling, UV proximity printing, resist reflow, or gray scale lithography can be used to build a full field master [8-13]. From this master it is possible to make working stamps that are used to mold the actual lenses. The use of working stamps is important because it allows the expensive master to be protected and the working stamp can be made out of materials that maintain pattern fidelity but accommodate the total thickness variation (TTV) within a substrate.

However, there are such problems with full field masters as the high cost of diamond or micro-milling and the difficulty in controlling critical optical performance parameters such as lens axis tilt, lens-to-lens spacing and lens profile accuracy. Recent advances in UV nano-imprint lithography (UV-NIL) allow step-and-repeat molding for master manufacturing from a sub-master using commercially available systems [14]. Starting out from a single lens pin or mold, this technique replicates one or more lens at a pre-defined location at a time and then moves to a new area until the entire master substrate is imprinted [15]. An example of 200 mm master stamps is shown in Fig. 6. This process has the advantage of dramatically decreasing the machining time required and increasing the uniformity from lens to lens.

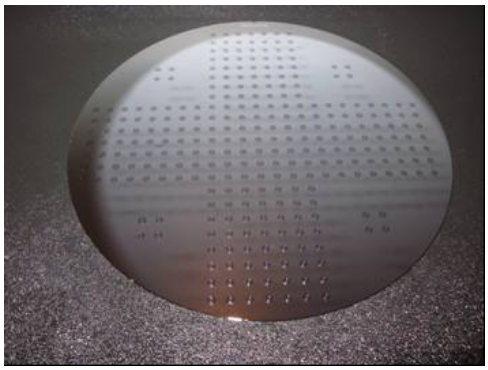


Figure 6. A 200 mm master stamp with 400 repeated lenses.

After the lens wafers and CIS wafer have been fabricated as shown in Fig. 7, the next steps are to align and bond the wafers together. This is typically done by aligning two elements and bonding them together using a UV curable adhesive and repeating the process until all the desired layers are bonded together. Alignment requirements are dictated primarily by the lens system design, and typical tolerances range from 5 to 25 µm per wafer [5]. Compared to the conventional camera technology, with which each lens system is individually molded and assembled, wafer-level alignment with alignment keys enables the use of precision alignment techniques, which helps maintain performance levels and reduces manufacturing costs.

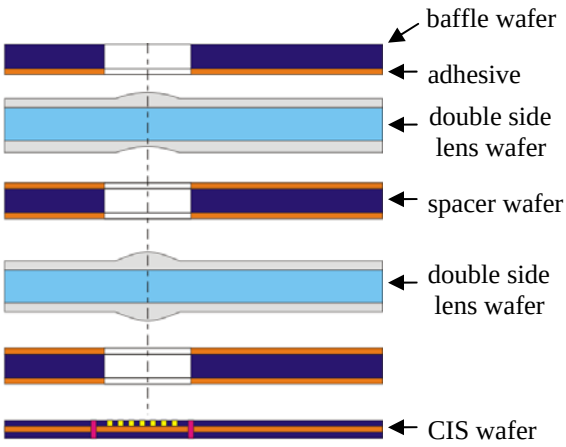


Figure 7. Lens, spacer and CIS stack prior to aligning and bonding.

Conformal Photoresist Coating Within TSV

TSV interconnection is becoming a mainstream interconnection method for camera module packaging. TSV processing for camera module packaging needs an advanced spray coating technique enabling conformal coating of various photoresists within high aspect ratio (HAR) vertical TSV interconnects. Conventional spray coating methods are not capable of coating conformally within HAR vias (causing too thick a layer on the top and lack of resist on the side), but with the new method (NanoSpray® coating) it is possible to conformally coat vertical vias and also to define patterns at the bottom of the deep vertical vias with the conventional proximity lithography [16].

The main applications with this new coating technique include (i) coating of a photosensitive organic insulation layer replacing a silicon oxide layer, (ii) coating of a photosensitive masking layer for proximity lithography to etch out barrier and insulation layers at the via bottom before copper plating (Fig. 8), and (c) coating of a passivation layer above copper conduction layer within TSVs. In Fig. 8 the copper conduction layer is plated after etching the insulation and barrier layers at the bottom of vias by using the NanoSpray® coated photoresist layer as an etch mask. Fig. 9 presents conformal coating results within various aspect ratios, where a variety of positive and negative photoresists can be applied within those vias according to application types.

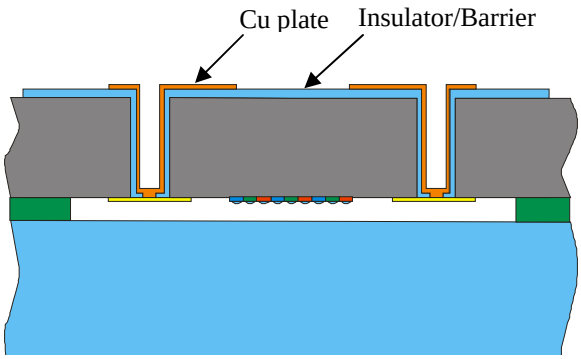


Figure 8. A schematic of the BSI CIS structure with a copper conduction layer plated within TSVs.

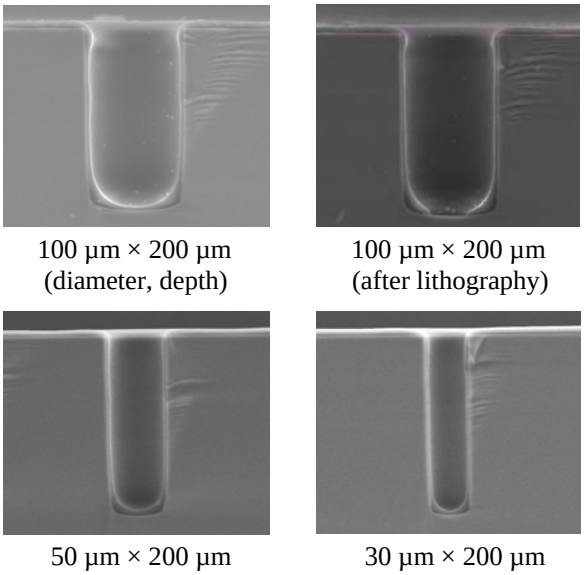


Figure 9. Conformal coating of photoresist with NanoSpray® coating within various TSV structures.

Advanced Backside Lithography for WLP

Lithography is always one of the major process steps for the new process development. Specific lithographic requirements for WLP processes, such as TSV interconnects, redistribution lines, copper pillars, and solder bumps as shown in Fig. 10, include (i) processing with a thick resist to form HAR TSVs, (ii) processing with bonded and thinned wafers (e.g., TSV backside alignment and processing), (iii) processing on high topography, (iv) compatibility with bonding processes, etc. In order to meet those requirements, following capabilities are essential for advanced lithographic systems, all of which are implemented into EVG's lithographic systems (e.g., IQ Aligner®);

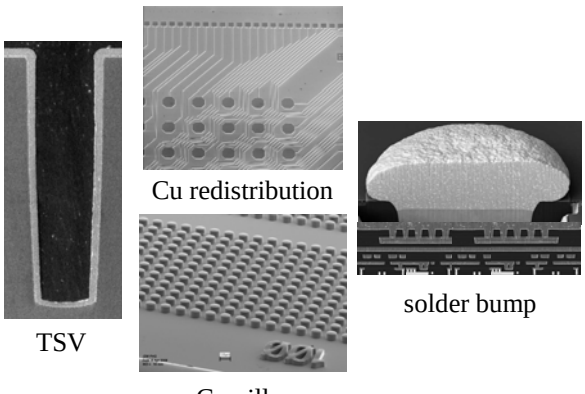


Figure 10. Various metallization processes for WLP (source: EMC-3D).

- Top side and bottom side microscopes with large gap optics (Fig. 11); Objective selection needs to be independent of the depth of focus (focusing with a z-motor can be performed instead). An alignment accuracy of less than 1 µm needs to be achieved regardless of the resist thickness.

- Backside alignment with transmitted IR; For the via-last approach, processing/aligning a thinned wafer on a silicon carrier or cover-glass wafer is needed by using transmitted IR, where alignment keys are buried at the bond interface. Alignment accuracy should be less than 1 µm in most cases.

- Bow-tolerant wafer handling with a special chuck design, and non-contact wedge-error compensation to prevent mask contamination during processing.

- Run-out error control through the temperature control of the mask and the wafer. Fig. 12 illustrates the significance of run-out error control during repeated processes.

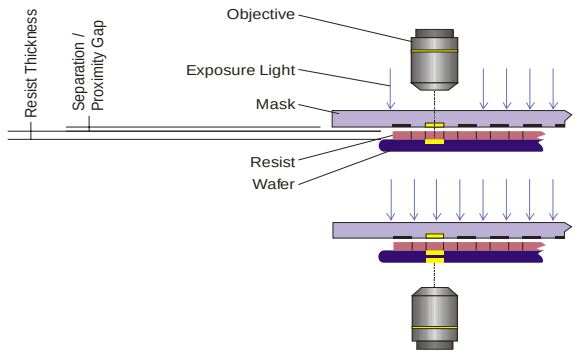


Figure 11. Top side and bottom side microscopes with large gap optics for WLP processing.

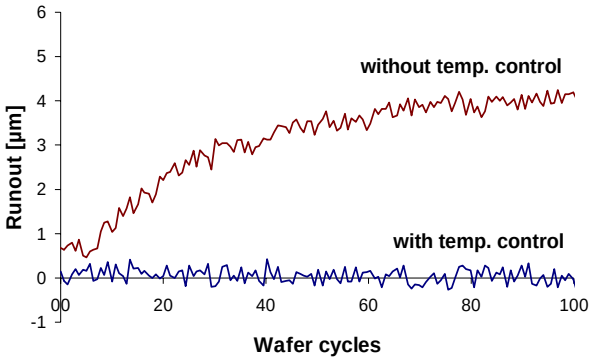


Figure 12. A run-out error as a function of wafer cycles with and without temperature control.

Conclusions

This article presented the advances in wafer-level processing and integration techniques for CIS module manufacturing. The cost-effective integration of miniaturized camera modules into cellular phones and other handheld electronics becomes a reality through the introduction of the BSI CIS camera module manufactured with wafer-level processing and integration techniques such as wafer-to-wafer permanent bonding, wafer-level lens molding and stacking, conformal coating of the photoresist within TSV, and advanced backside lithography for WLP metallization. Those wafer-level techniques pave the way to the future growth of the digital imaging industry by improving the electrical and optical aspects of devices as well as the module manufacturability.

In manufacturing BSI image sensors the fully processed CMOS wafer is bonded to a blank carrier wafer and then back-thinned in order to open the photosensitive sensor area. We developed both low-temperature plasma-activated silicon oxide bonding and polymer adhesive bonding methods, and compared the benefits and demerits of those two bonding approaches. In some cases the cover-glass wafer can be stacked onto the device wafer by using polymer adhesive bonding typically with a thermally-curable adhesive layer.

When it comes to WLO processes, we provide total solutions for (i) master stamp fabrication, (ii) lens molding, and (iii) aligning and stacking of the lens and spacer wafers to the CIS wafer. With the newly developed NanoSpray® coating technique, it is possible to conformally coat HAR vertical TSVs and also to define patterns at the bottom of the deep vias with the conventional proximity lithography. We also presented solutions for backside lithography techniques needed for various WLP metallization processes (TSV, redistribution lines, pillars, and bumps) with such characteristics and features as top-side and bottom-side microscopes with large gap optics, backside alignment with transmitted IR, bow-tolerant wafer handling, non-contact wedge-error compensation, and precise run-out error control.

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