Improving System Performance with eGaN® FETs in DC-DC Applications

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Abstract

The intermediate bus architecture (IBA) is currently the most popular power system architecture in computing and telecommunications equipment. It typically consists of a +48 V system power distribution bus that feeds on-board isolated converters, which in turn supply power to a 12 V power bus. From the 12 V power bus, the final power is delivered to the end loads by regulated non-isolated point of load (POL) converters. In this paper we demonstrate substantial system gains using enhancement mode gallium nitride power transistors in high frequency isolated and non-isolated DC-DC converters. These transistors, also known as eGaN® FETs, have been commercially available for over three years and are making significant inroads replacing the aging silicon power MOSFET.

Key words

GaN power device, high frequency power conversion, intermediate bus architecture, soft switching

I. Introduction

Distributed power systems are prevalent in telecommunications, networking, and high-end server applications and generally utilize a 48 V bus voltage adopted from the telecom industry. In the traditional distributed power architecture (DPA), from the 48 V bus voltage, a number of fully regulated isolated DC/DC point of load (POL) converters are used to deliver the required voltage and power to the individual loads. As communications, networking, and high-end server systems have become more complex, the voltages and currents demanded by the growing number of loads have increased significantly [1].

To simplify design and improve performance, the concept of intermediate bus architecture (IBA) has become widely accepted [2],[3]. The popular IBA approach employs a lower number of 48 V isolated bus converters to satisfy isolation requirements and supply an intermediate bus voltage which is generally 12 V. From the 12 V bus, the final power is provided to the loads by smaller, more efficient, regulated non-isolated POL converters.

To improve overall performance in the IBA, more efficient power devices are required. For silicon (Si) MOSFETs, the gains in performance have slowed as the technology has matured and approached its theoretical limits [4]. Gallium nitride devices have emerged as a possible replacement for silicon devices in various power conversion applications and as an enabler of new applications not previously possible. GaN devices are a high electron mobility transistor (HEMT) with a higher band gap, electron mobility, and critical electric field strength than silicon [5]. GaN technology, in its early stages, already outperforms the theoretical limits of MOSFETs in the metric of specific on resistance for a given breakdown voltage, as shown in figure 1.

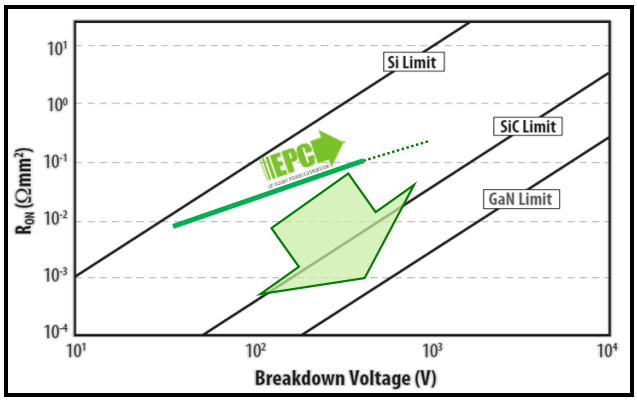


Figure 1: Theoretical and current eGaN FET on-resistance vs. blocking voltage capability for silicon, silicon-carbide, and gallium nitride devices

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II. Comparing Performance Metrics of GaN and Si Power Devices

A. *Hard Switching Applications*

The first commercially available enhancement mode gallium nitride transistors have a lateral structure with voltages ranging from 40-200 V. These HEMT transistors operate similarly to the traditional Si MOSFETs and can provide improved switching and packaging performance [6]. While specific on resistance for a given breakdown voltage, as shown in figure 1, demonstrates the ability of GaN transistors to significantly shrink the size of the power device compared to Si counterparts, this metric does not directly correlate to in-circuit switching performance.

In a traditional hard switching transition, the switching losses are impacted primarily by two device parameters, Q_{GD}, also known as the miller charge, which controls the voltage rising (T_{VR}) and falling speed; and Q_{GS2}, which is the portion of the gate source charge from the device threshold voltage to the gate plateau voltage, which controls the current rising and falling speed (T_{CF}).

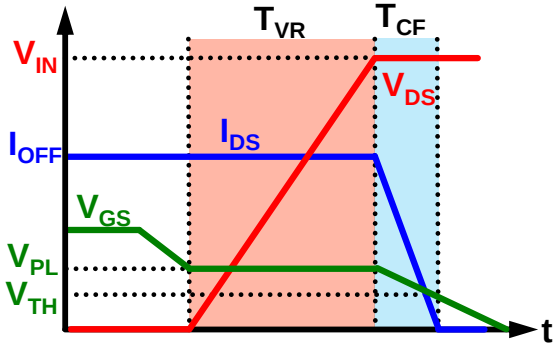


Figure 2: Ideal hard switching waveforms at device turn off transition

The turn off period, shown in figure 2, begins with a decrease of gate drive voltage; when the gate voltage reaches the plateau, the voltage across the device will begin to rise, being driven by the gate current, I_G. During the voltage rising period, the transistor encounters both current and voltage in the device, resulting in switching loss. For the voltage rising period, the device parameter determining loss is Q_{GD}. When the transistor voltage reaches the input voltage, the current in the device will begin to fall and more switching loss in the device will be incurred. For the current falling period, the device parameter determining loss is Q_{GS2}. The power loss during the turn off switching transition can be given by:

$$P_{SW(OFF)} = \frac{V_{IN} \cdot I_{OFF} \cdot (Q_{GD} + Q_{GS2})}{2 \cdot I_G} \quad (1)$$

Where V_{IN} is the input voltage, I_{OFF} is the device current at turn off, Q_{GD} is the miller charge, Q_{GS2} is the gate to source charge from the device threshold voltage to plateau voltage, and I_G is the gate driver current.

For the turn on switching losses, the same principles apply; minimizing the Q_{GD} and Q_{GS2} parameters will decrease switching losses incurred in a hard switching application. The turn on loss is given by:

$$P_{SW(ON)} = \frac{V_{IN} \cdot I_{ON} \cdot (Q_{GD} + Q_{GS2})}{2 \cdot I_G} \quad (2)$$

Where I_{ON} is the device current at turn on.

Switching figure of merit (FOM) [7]-[10] is used to compare the in circuit performance capability of a given device technology in different applications. In hard switching applications for the voltage and current ranges of eGaN FETs (40- 200 V) a useful figure of merit is derived to minimize the power loss contributed from the device conduction and switching losses which are given by:

$$P_{CONDUCTION} = I_{RMS}^2 \cdot R_{DSON} \quad (3)$$

$$= \frac{I_{RMS}^2 \cdot R_{DSON_SP}}{A_{DEVICE}} \quad (4)$$

$$P_{SWITCHING} = \frac{V_{IN} \cdot I_{OUT} \cdot (Q_{GD} + Q_{GS2}) \cdot F_{SW}}{I_G} \quad (5)$$

$$= \frac{V_{IN} \cdot I_{OUT} \cdot (Q_{GD_SP} + Q_{GS2_SP}) \cdot F_{SW} \cdot A_{DEVICE}}{I_G} \quad (6)$$

$$P_{LOSS} = P_{CONDUCTION} + P_{SWITCHING} \quad (7)$$

Where I_{RMS} is the RMS current conducted through the device, R_{DSON} is the on-resistance of the device, I_{OUT} is the output current, F_{SW} is the switching frequency, Q_{GD_SP} and $Q_{GS\ 2_SP}$ are the specific charges, and R_{DSON_SP} is the specific on-resistance for a given device area, A_{DEVICE}.

To determine the device parameters producing minimum losses, the derivative of (7) is taken with respect to A_{DEVICE} with dP_{LOSS}/dA_{DEVICE} set to zero. The optimal value of A_{DEVICE} is then determined, yielding the optimal die size, $A_{OPTIMAL}$.

$$A_{OPTIMAL} = \sqrt{\frac{R_{DSON_SP}}{(Q_{GD_SP} + Q_{GS2_SP})}} \cdot \frac{I_{RMS}}{\sqrt{\frac{V_{IN} \cdot I_{OUT} \cdot F_{SW}}{I_G}}} \quad (8)$$

Placing (8) into (7) yields the minimal power loss in terms of device parameters and circuit operating conditions.

$$P_{MIN} = \sqrt{(Q_{GD_SP} + Q_{GS2_SP}) \cdot R_{DSON_SP}} \cdot 2 \cdot I_{RMS} \cdot \sqrt{\frac{V_{IN} \cdot I_{OUT} \cdot F_{SW}}{I_G}} \quad (9)$$

Combining the device related parameters contributing to loss, a figure of merit to simply compare the in circuit performance capability of different device technologies can be given as:

$$FOM_{HS} = (Q_{GD_SP} + Q_{GS2_SP}) \cdot R_{DSON_SP} \quad (10)$$

$$= (Q_{GD} + Q_{GS2}) \cdot R_{DSON} \quad (11)$$

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For a given technology, a lower value of FOM will be able to reduce the power loss proportional to:

$$P_{LOSS} \propto \sqrt{FOM_{HS}} \quad (12)$$

In this equation P_{LOSS} is the power loss contributed from the device conduction and switching losses.

The comparison of the hard switching FOM for a 100 V eGaN FET and 80 V MOSFET devices is shown in figure 3, the eGaN FET has a 70% lower FOM than the best state of the art lower rated Si devices. For a 48 V converter, this translates to a device power loss reduction of almost a factor of two in hard switching applications by replacing Si MOSFETs with eGaN FETs.

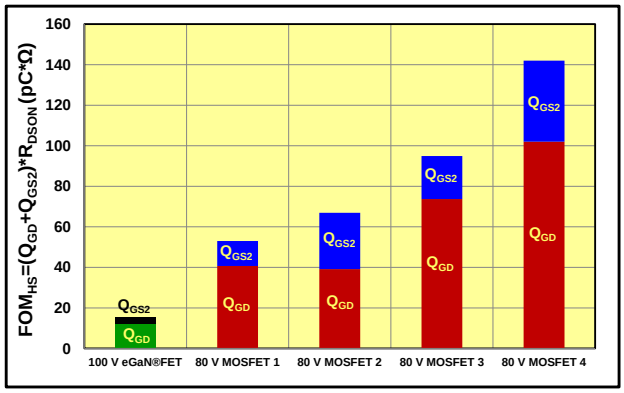


Figure 3: Hard switching figure of merit comparison for 100 V eGaN FET and 80 V MOSFETs (V_{DS}=0.5·device voltage rating, I_{DS}=15 A)

B. *Soft Switching Applications*

In soft switching applications the switching related losses are minimized by using techniques such as zero voltage switching (ZVS) and zero current switching (ZCS). With the reduction of switching losses, the Q_{GD} and Q_{GS2} terms that dominated losses in hard switching applications are no longer the critical device parameters determining circuit performance.

There are many different soft switching techniques and directly deriving an analytical FOM to minimize loss for the wide variety of soft switching methods into a simple metric to compare device technologies is not practical. In most soft switching applications the device output charge, Q_{OSS}, has a large impact on performance as it directly impacts the energy required to achieve ZVS. A reduction in energy required to achieve ZVS can result in reduced dead times and ZVS currents, providing both a longer power delivery period and lower RMS currents in a high frequency soft switching converter. Similarly, Q_{OSS} is also the main loss component in ZCS switching. The other major contributor to loss is the gate charge, Q_G, which is a major switching related loss in high frequency soft switching applications.

To compare the critical parameters that influence the in-circuit performance of different device technologies in soft switching applications, a figure of merit is proposed:

$$FOM_{SS} = (Q_{OSS} + Q_G) \cdot R_{DSON} \quad (13)$$

Where Q_{OSS} is the output charge of the device and Q_G is the gate charge of the device.

The comparison of soft switching FOM for a 100 V eGaN FET and 100 V and 80 V MOSFET devices is shown in figure 4. The eGaN FET offers over a 60% reduction in FOM compared to the best state of the art 100 V Si MOSFET, and around a 50% reduction over the best 80 V Si MOSFET. The significant reduction in soft switching figure of merit offered by GaN technology enables significant performance improvements in high frequency soft switching applications. The benefits of replacing a Si MOSFET with an eGaN FET in a high frequency resonant converter will be verified in the following section.

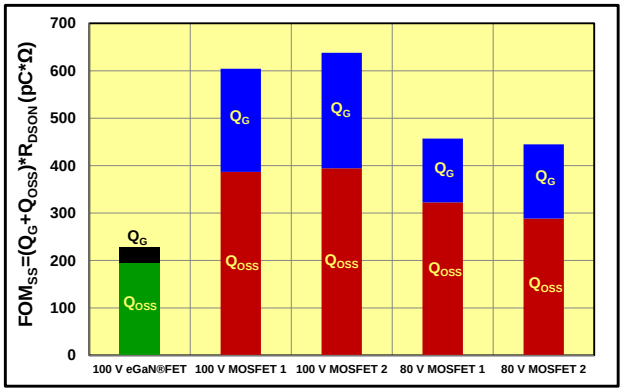


Figure 4: Soft switching figure of merit comparison for 100 V eGaN FET and 80 V MOSFETs (V_{DS}=0.5·device voltage rating, I_{DS}=15 A)

III. eGaN FETs in Resonant Isolated DC-DC Converters

To achieve improved efficiency at higher switching frequencies, resonant topologies may be considered. Resonant topologies are particularly beneficial in DC/DC transformer applications, also known as a DCX, or an unregulated bus converter due to the removal of the regulation requirements, allowing the converter to always operate at the resonant frequency. In a 48 V IBA, the final regulation to the loads is provided by smaller, more efficient, regulated non-isolated POL converters. This allows the bus converters to be operated as unregulated DC/DC transformers, improving efficiency and simplifying converter design [11]-[13].

To demonstrate the opportunities enabled by converting from silicon-based power MOSFETs to enhancement mode GaN devices in soft switching applications, we chose the topology as shown in Figure 5 that employed a resonant technique utilizing the transformer's magnetizing inductance (L_M) and resonance of the leakage inductance (L_K), together with a small output capacitance (C_O), to achieve zero voltage switching, limit turn-off current, and eliminate body diode conduction [12], [14].

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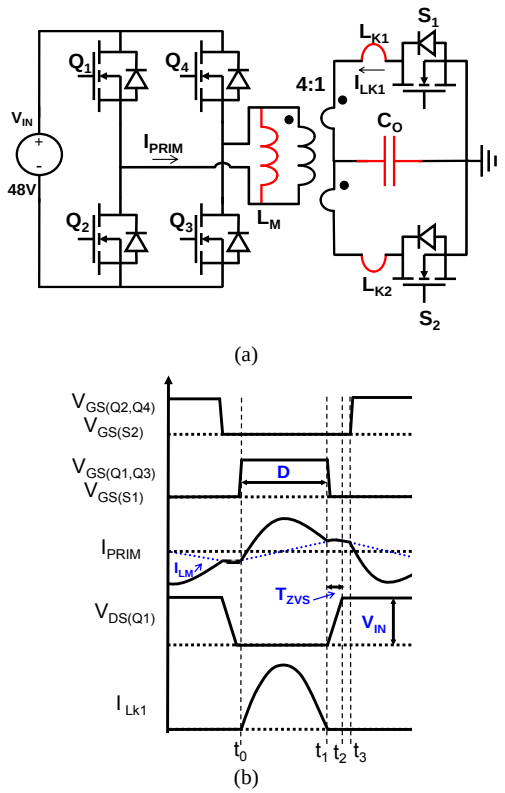


Figure 5: High frequency bus converter (a) Schematic (b) Operating waveforms

To obtain a direct comparison in performance between GaN devices and Si MOSFETs in an isolated converter, having identical layouts and using the same topology is critical. Isolated DC-DC converter performance is heavily dependent on topology selection, printed circuit board (PCB) layout, number of PCB inner layers, copper weight of inner layers, and the design of the transformer. To accurately compare the performance of GaN and Si in a high frequency resonant bus converter application, devices with similar on-resistance were selected, the same circuit topology was used, and a similar layout was maintained for both designs.

Two experimental prototypes, shown in figure 6, were designed and tested based on the schematic in figure 5(a) to run at a switching frequency of 1.2 MHz. Both PCBs were constructed with 12 layers and two ounce copper thickness for all layers. To accurately compare only device performance, these prototypes both had the same 3F45 Mn-Zn transformer core and identical windings designed from [15]. The placement of the primary side input capacitors and secondary resonant capacitors were similar for both designs to ensure similar parasitic inductances for the primary and secondary loops, with the only differences being those introduced by the different packages of the Si MOSFETs and eGaN FETs. By using eGaN FETs with lower specific on resistance and improved packaging, the active footprint area shrank significantly, reducing the power stage size by 30% compared to the Si MOSFET benchmark design.

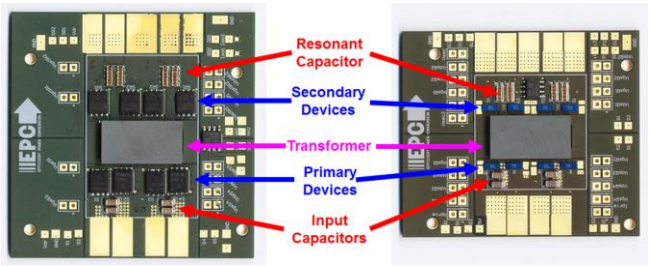


Figure 6: Experimental 48 V to 12 V bus converter prototypes operating at a switching frequency of 1.2 MHz constructed with (a) silicon MOSFETs, and (b) gallium nitride eGaN FETs

The experimental switching waveforms for the designs at 1.2 MHz are shown in Figure 7. Both designs have the same magnetizing inductance built into the transformer via an air gap to achieve zero-voltage switching during the device off state. Due to almost a factor of 2 decrease in output charge provided by the primary and secondary eGaN FETs, the ZVS transition is achieved in a proportionally shorter period, increasing the effective duty cycle and improving the overall converter performance. For the Si MOSFET design, the dead time required for ZVS was measured to be 87 ns and the effective duty cycle for each device was limited to 34%. With the faster switching eGaN FETs, the dead time was reduced to 42 ns resulting in a 42% duty cycle for each device while allowing for an extended power delivery period. From the switching waveforms, it can also be seen that the gate drive speed for the eGaN FET is significantly faster than the Si MOSFET counterpart even when driven with a lower gate drive voltage, providing both faster switching speed and reduced gate losses.

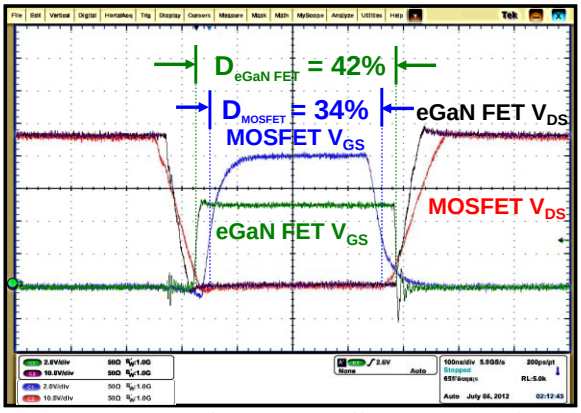


Figure 7: Switching waveforms showing effective duty cycle for primary side eGaN FET and Si MOSFET designs at F_S = 1.2 MHz, V_{IN} = 48 V, and I_{OUT} = 26 A, eGaN FET: EPC2001, MOSFET: BSC057N08NS3.

The comparison in efficiency between the two designs operating at 1.2 MHz is shown in Figure 8. The eGaN FET-based converter offers a one-percentage point

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improvement in peak efficiency over its Si MOSFET counterpart, resulting in about 25% less power loss. Since products based on this type of design are thermally limited, the reduction in power loss translates directly into higher output power handling capability. In this case, the eGaN FET converter can increase the output power capability by up to 65 W while maintaining the same total converter loss when compared to the benchmark Si MOSFET design. Assuming an approximate 12 W maximum power loss for both designs, the output power of the eGaN FET-based converter can be increased from 270 W to 325 W.

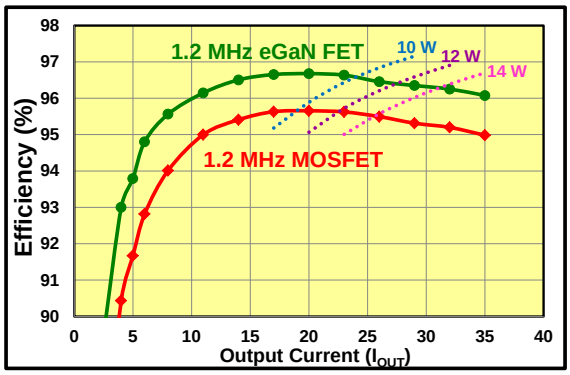


Figure 8: Experimental comparison between eGaN FET and Si MOSFET based V_{IN} = 48 V, V_{OUT} = 12 V, F_{SW} = 1.2 MHz resonant bus converters.

IV. eGaN FETs in Non-Isolated DC-DC Converters

The limited and ever decreasing motherboard area around computer processors that are available for power conversion has driven the need for ever decreasing size in point of load (POL) modules. Since the size of the magnetic components dominates the converter volume, frequencies are pushed higher to reduce magnetic volume, reducing efficiency and increasing power loss. Improvements in device hard switching performance can be directly translated into smaller power modules.

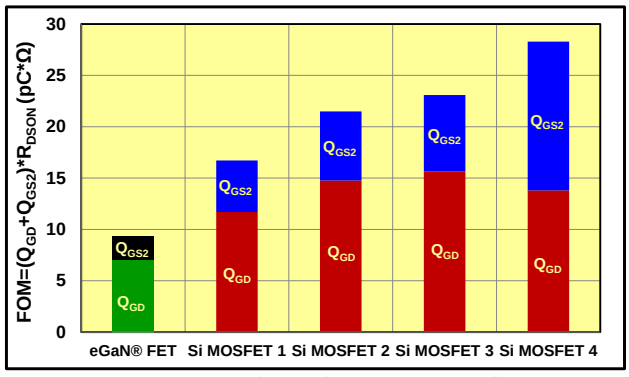
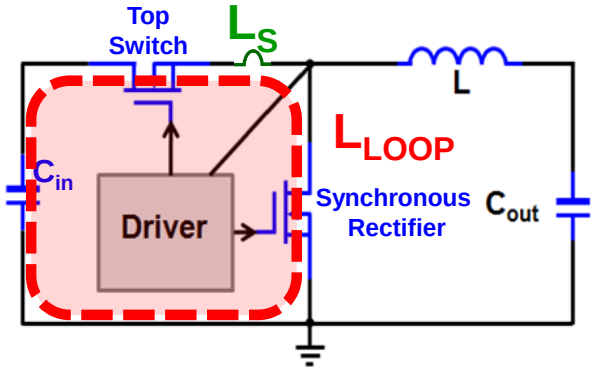
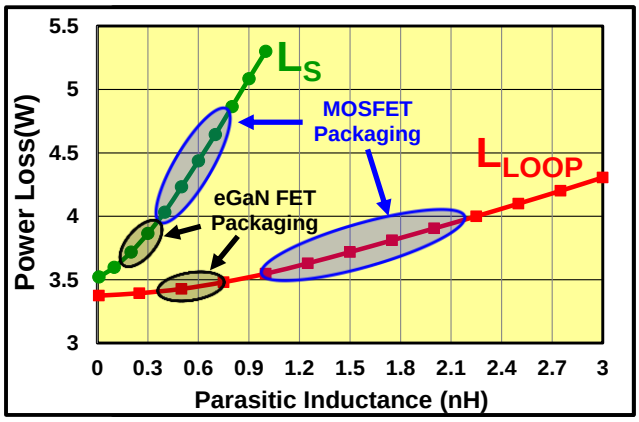


Figure 9: Hard switching figure of merit comparison for 40 V eGaN FET and 40 V MOSFETs (V_{DS}=0.5·Device voltage rating, I_{DS}=20 A)

From a hard switching FOM comparison, shown in figure 9, eGaN FETs can offer higher efficiency than 40 V Si MOSFET counterparts. In practical hard switching applications, FOM is just one of the contributors to achieving higher efficiency. To enable the high switching speed available from low FOM, low parasitic packaging and PCB layout is required. eGaN FETs were developed in land grid array (LGA) packages that not only have low internal inductance, but enable the user to design ultra-low inductance into their board. The PCB layout contributes to both the common source inductance (L_S), and the high frequency power commutation loop inductance (L_{LOOP}), shown in figure 10a. These parasitics greatly impact the loss of a converter, as shown in figure 10b. At EPC, we have developed an optimal layout [16] further enhancing the benefits of eGaN FET technology, providing additional efficiency gains and higher voltage operation capability.



(a)



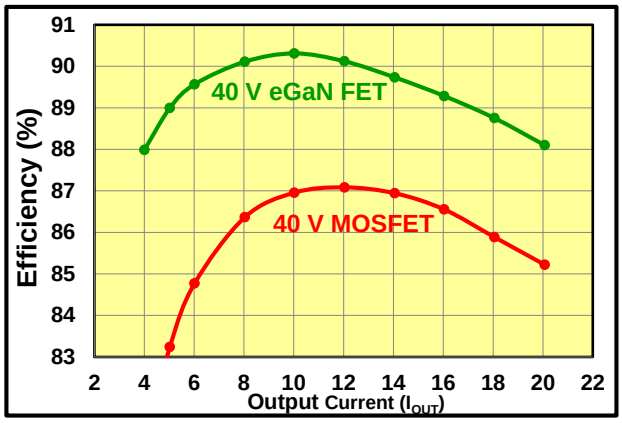
(b)

Figure 10: (a) Synchronous buck converter with parasitic inductances (b) Parasitic inductance impact on power loss (V_{IN}=12 V, V_{OUT}=1.2 V, I_{OUT}=20 A, F_{SW}=1 MHz, Top Switch: EPC2015, Synchronous Rectifier: EPC2015)

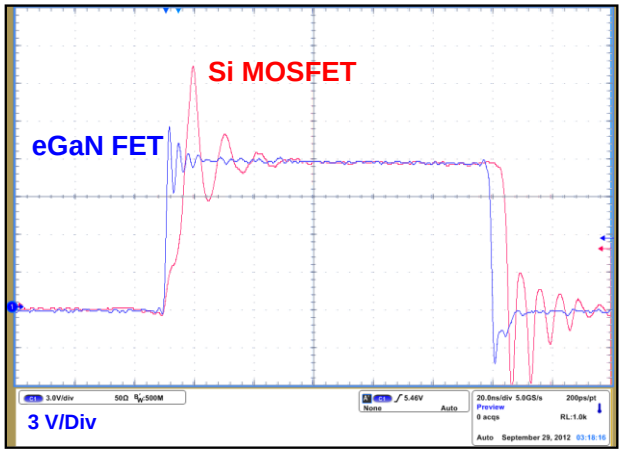
The efficiency comparison of buck converters operating at a 1 MHz switching frequency using state of the art 40 V Si MOSFETs and 40 V eGaN FETs is shown in figure 11a, the eGaN FET based design can improve efficiency over 3% when compared to the Si MOSFET. With the

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significantly reduced high frequency loop inductance provided by the ultra-low package inductance of the eGaN FET package in combination with an eGaN FET optimized PCB layout, a 500% increase in switching speed and a 40% reduction in voltage overshoot, as shown in figure 11b, can be achieved compared to the 40 V Si MOSFET benchmark.



(a)



(b)

Figure 11: (a) Efficiency comparison and (b) Switching node waveforms (I_{OUT}=20 A) of eGaN FET and MOSFET designs (V_{IN}=12 V, V_{OUT}=1.2 V, Fs=1 MHz, L=300 nH, eGaN FETS: T: EPC2015 SR: EPC2015, MOSFETs: T: BSZ097N04LSG SR: BSZ040N04LS G)

V. Conclusion

The availability of high performance eGaN FETs offers the potential to switch at higher frequencies and higher efficiency than possible with traditional Si MOSFET technology. eGaN FETs have a distinct advantage over silicon MOSFETs in both hard and soft switching applications. In this work, two figures of merits were proposed to compare device technologies for use in hard and soft switching applications.

The benefits of eGaN FETs in an IBA system with a 48 V isolated resonant bus converter first stage operating at 1.2 MHz and a 12 V non-isolated hard switching POL second stage operating at 1 MHz were demonstrated. By replacing silicon MOSFETs with eGaN FETs, the losses were reduced over 20% in both the isolated and non-isolated stages, providing superior system performance not achievable with Si technology. No matter what the application, gallium nitride technology offers the potential to improve performance and as this technology matures these benefits will only increase.

References

[1] M. M. Jovanovic, "Power Conversion Technologies for Computer, Networking, and Telecom Power Systems - Past, Present and Future," International Power Conversion & Drive Conference (IPCDC) St. Petersburg, Russia, June 8-9, 2011.

[2] M. Schlecht, "High Efficiency Power Converter," United States Patent No. 7,269,034.

[3] R.V. White, "Emerging On-Board Power Architectures," APEC '03, Eighteenth Annual IEEE, Volume 2, 9-13 Feb. 2003, pp. 799-804.

[4] A. Lidow, J. Strydom, M. de Rooij, and Y. Ma, "GaN Transistors for Efficient Power Conversion" Power Conversion Publications, 2012.

[5] N. Ikeda, S. Kaya, L. Jiang, Y. Sato, S. Kato, S. Yoshida, "High power AlGaN/GaN HFET with a high breakdown voltage of over 1.8 kV on 4 inch Si substrates and the suppression of current collapse", Power Semiconductor Devices and IC's, 2008. ISPSD '08. pp.287-290, 18-22 May 2008.

[6] D. Reusch, D. Gilham, Y. Su, and F. Lee, "Gallium nitride based 3D integrated non-isolated point of load module," in Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE, Feb. 2012, pp. 38 –45.

[7] A. Q. Huang, "New Unipolor Switching Power Device Figures of Merit," IEEE Electron Device Lett., vol. 25, pp. 298-301, 2004.

[8] I.-J.Il-Jung Kim, S. Matsumoto, T. Sakai, and T. Yachi, "New power device figure-of-merit for high frequency applications," in Proc. Int. Symp. Power Semiconductor Devices ICs, Yokohama, Japan, 1995, pp. 309–314.

[9] B. J. Baliga, "Power semiconductor device figure-of-merit for high frequency applications," IEEE Electron Device Lett., vol. 10, pp. 455–457, 1989.

[10] Y. Ying, "Device selection criteria----based on loss modeling and Figure of Merit", Thesis of Master of Science in Electrical Engineering of Virginia Tech, 2008.

[11] P. Vinciarelli, "Point of load sine amplitude converters and methods," U.S. Patent 7,145,786, Dec. 5 2006.

[12] Y. Ren, M. Xu, J. Sun, and F. C. Lee, "A Family of High Power Density Unregulated Bus Converters," IEEE Transactions, Power Electron, Vol. 20, no. 5, pp. 1045–1054, Sep. 2005.

[13] K. Matsuura, H. Yanagi, S. Tomioka, T. Ninomiya, "Power-density development of a 5MHz-switching DC-DC converter," Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE , vol., no., pp.2326,2332, 5-9 Feb. 2012

[14] Y. Ren, F.C. Lee, and M. Xu, "Power Converters Having Capacitor Resonant With Transformer Leakage Inductance," U.S. Patent 7,196,914, March 27 2007.

[15] D. Reusch and F.C. Lee, "High Frequency Bus Converter with Low Loss Integrated Matrix Transformer," Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE, pp.1392-1397, 5-9 Feb. 2012.

[16] D. Reusch and J. Strydom, "Understanding the Effect of PCB Layout on Circuit Performance in a High Frequency Gallium Nitride Based Point of Load Converter," Applied Power Electronics Conference, APEC 2013, pp.649-655, 16-21 March 2013.

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