Compressive-Post Packaging of Double-Sided Die

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Abstract
Double-sided module exhibits electrical and thermal characteristics that are superior to wire-bonded counterpart. Such structure, however, induces more than twice the thermo-mechanical stress in a single-layer structure. Compressive posts have been developed and integrated into the double-sided module to reduce the stress to a level acceptable by silicon dice. For a 14 mm x 21 mm module carrying 6.6 mm x 6.6 mm die, finite-element simulation suggested an optimal design having four posts located 1 mm from the die; the z-direction stress at the chip was reduced from 17 MPa to 0.6 MPa.

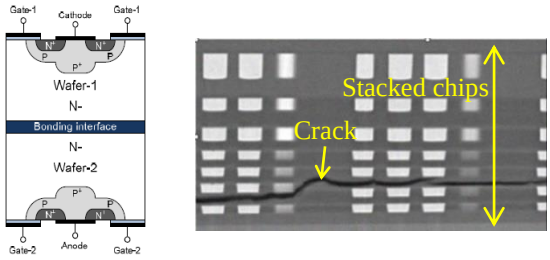
Key words
Bi-directional IGBT, compressive post, die cracking, planar module, thermo-mechanical stress, three-dimensional packaging.

I. INTRODUCTION

Chip-stack and double-sided packaging processes often encounter chip warping or cracking during solder reflow owing to mismatches among coefficients of thermal expansion (CTE) [1][2]. Die damage becomes more severe as semiconductor roadmaps call for thinner dice.

A packaging method using compressive posts is discussed herein as a means to reduce the thermo-mechanical stress on the die. The packaging of bi-directional IGBT (BD-IGBT) (Fig. 1(a) [3]) with planar joints is used for process development and verification. Unlike conventional bi-directional modules with two IGBTs and two diodes, the BD-IGBT chip can conduct and block currents in both forward and reverse directions [4]-[11]. The BD-IGBT can be fabricated by either a double-sided process or hydrophobic wafer bonding process (Fig. 1); previous studies showed that the latter had more symmetrical I-V characteristics in both directions [6]-[8]. The ultimate strength of the bonding interface is only 0.7 MPa, rendering this stress-sensitive chip a suitable candidate to test the effectiveness of the compressive-post idea.

In general, thermo-mechanical stress due to CTE mismatch is avoided in electronic packaging. However, the developed compressive posts take advantage of the CTE mismatch to counterbalance asymmetric expansion in the package. The compressive posts are formed around the die using solder balls that have higher CTE than silicon. During the cooling phase of the reflow process, the posts shrink more than the chip, compressing the chip and alleviating the tensile stress.



(a) (b)

Fig. 1. Bi-directional switch developed with a double-sided process (a) and stacked chips with crack due to thermo-mechanical stress during a packaging process [2][7] (b).

The structure of the bi-directional module and the expected peel stress are analyzed in Section II. The relation of the compressive posts to the reliability of the module are parametrically studied by ANSYS 13 simulation and experimentally verified in Section III. Section IV describes the packaged bi-directional module and electrical

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characteristics.

II. Thermo-Mechanical Stress in a Multi-Layer Structure

A. Layout of the Module

To reduce electrical and thermal impedances, an indented lead frame was developed to connect the chip's terminals to the package pins as shown in Fig. 2. The measured package inductance was 70% of wire-bonded inductance. The simulated maximum Von-Mises plastic strain at the die-attach layer was reduced to 54% of the strain in a solid copper lead frame. Thus, thermo-mechanical stress was mitigated without compromising the electrical and thermal advantages of the double-sided package.

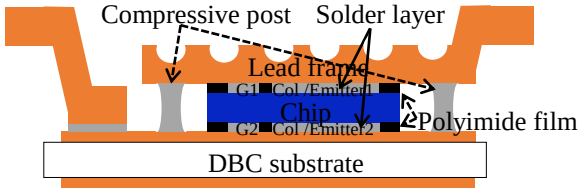

Fig. 2. Lay-up of the developed module with compressive posts.

B. Peel Stress of the Double-Sided Package

A solder layer between two materials experiences high thermo-mechanical stress due to differences in CTE [9][12]. The interfacial shear and peel stresses were modeled in [13][14] for the geometry illustrated in Fig. 3. The line AA represents the center of the model. The peel stress in Fig. 3 was derived from considerations of moment of equilibrium of the applied forces combined with shear stress:

$$P(x) = \frac{(h_1 D_2 - h_2 D_1)}{2D} \frac{(\alpha_1 \Delta T - \alpha_2 \Delta T)}{K \cosh(\kappa L)} \cosh(\kappa x) \quad (1)$$

where α_i is coefficient of thermal expansion of i_{th} material; ΔT is the change of temperature; L is length of the layer; and D_i is the flexural rigidity.

$$\kappa = \sqrt{\lambda \cdot K^{-1}} \quad (2)$$

where λ is axial compliance; K is stress compliance; and D is the flexural rigidity given by

$$K = K_0 + \sum_{i=1}^{2} K_i = h_i / G_i + \sum_{i=1}^{2} h_i / 3G_i \quad (3)$$

$$\lambda = \sum_{i=0}^{3} \left(1 - \nu_i^2\right) / E_i h_i \quad (4)$$

$$D = \sum_{i=0}^{2} E_i h_i^3 / 12\left(1 - \nu_i^2\right) \quad (5)$$

where h is the height of the layer; G is shear modulus; E is elastic modulus; and ν is Poisson's ratio.

Material properties in TABLE I were used in (1) - (5) to estimate the peel stress. Since the bonding interface has much weaker strength than the adhesion strength of the solder layer, the five-layer structure was divided into two parts along the bonding interface: the top side with lead frame, solder, and top half of the chip; the bottom side with bottom half of the chip, solder, and DBC substrate. Fig. 4 shows the calculated peel stress at top and bottom joints resulting from 150°C change. The peel stress increases from the center to the edge of the module. The top side experiences 2.48 times the peel stress of the bottom side. The peel stresses are induced in opposite directions, implying higher stress to the chip than single-side die attachment. Even though the peel stresses were calculated with simplified five-layer structure, the result showed the possibility of the die cracking with the double-sided package. In addition, the calculated peel stresses with different heights (h_0) in Fig. 5 shows that the thinner joint results in the higher peel stress. Therefore, it is advisory to avoid using thin (< 0.2mm) die-attach layer for the double-sided module.

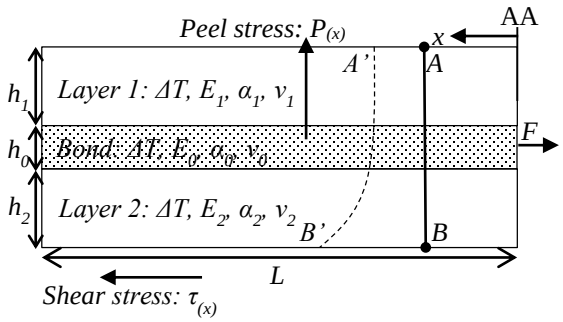

Fig. 3. 2D presentation of shear stress and displacement [13].

TABLE I
MATERIAL PROPERTIES FOR THE CALCULATIONS IN FIG. 4

Material	E (GPa)	G (GPa)	Poisson's Ratio
Copper	112.4	40.95	0.343
Silicon	32	43.91	0.28
Al_2O_3	303	125.21	0.21
Solder ($Sn_{63}Pb_{37}$)	110	11.59	0.38

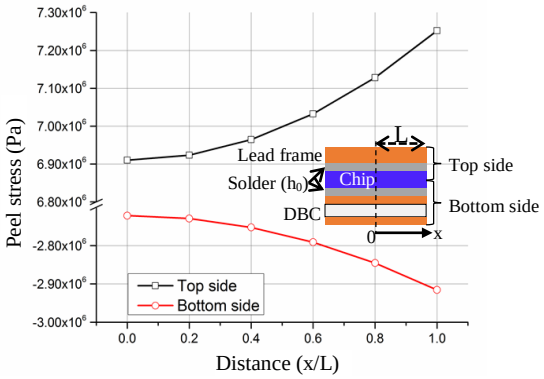

Fig. 4. Calculated peel stresses of the top and bottom joints (h_0 = 0.2 mm) using the model in Fig. 3.

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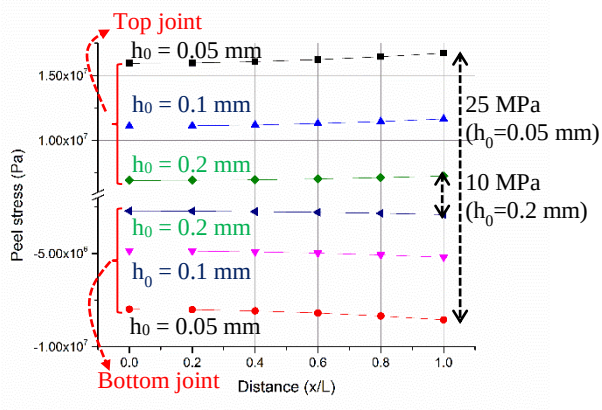

Fig. 5. Calculated peel stresses with different heights of solder layers (h_0).

III. Compressive Posts

A. Material Deformation in Double-Sided Package

Due to the asymmetrical deformation of packaging materials, an electronic package experiences residual stress. Fig. 6(a) illustrates the deformation of the double-sided module with a DBC substrate at the bottom and a copper lead frame on the top. As temperature of the chamber cools down from the stress-free temperature, the DBC substrate and copper lead frame shrinks at a higher rate than silicon chip. Both DBC substrate and lead frame bend away from the chip, inducing tensile stress on the die and solder joints. As analyzed in Fig. 4, the tensile stress detaches the bonded chips if it is higher than the bond strength. Compress posts were integrated into the package as shown in Fig. 6(b) to counteract the tensile stress.

High-temperature solder balls ($Pb_{93.5}Sn_5Ag_{1.5}$) were placed around the chip, and solder preforms ($Sn_{63}Pb_{37}$) were used as joining material. Representative packaging materials are listed in TABLE II in Section IV. As temperature of reflow chamber increases, both copper lead frame and DBC substrate starts expanding as indicated by dashed lines. Because the solder ball has higher melting temperature (T_m = 301°C) than solder preform (T_m = 183°C), it keeps the shape at the reflow temperature and forms a post. As the chamber temperature cools down below the liquidus temperature, solidified solder posts shrink more than silicon chip due to its higher CTE. The compressive posts pull down the lead frame and provide residual compressive force to the chip.

B. Parametric Study of Compressive Posts

To verify and optimize the concept in Fig. 6, the structure in Fig. 2 was modeled by ANSYS 13 as shown in Fig. 7. The model consists of the DBC substrate, solder layers, die, copper lead frame, and the solder posts. Material specifications and dimensions are in TABLE II in Section IV. The distance between the post and chip is defined as *d*, and the displacements of the lead frame and chip were monitored along lines AB and CD, respectively. The number of posts was varied from zero to six, and Fig. 7(b) shows the simulation model for a quarter of a module with four posts.

To analyze the influence of the gap between chip and post, distance (*d*) was swept from 0.5 mm to 2 mm with four and six posts. The Von-Mises plastic strains were monitored at the top solder layer and the compressive post (Fig. 8); the dashed line is for the case without post. When the distance (*d*) increases with four posts, the plastic strain decreases at the solder and increases at the compressive post. Four posts yield lower strains than six posts between 0.5 mm and 1.5 mm. Therefore, the best design is four posts separated by 0.75 mm to 1 mm from the die. The maximum Von-Mises plastic strain at the top solder layer decreases to 87.7% of the no-post value. The simulation suggests that the compressive posts yield reliable packaging process for the bonded chips and reduce stress on the die-attach layer.

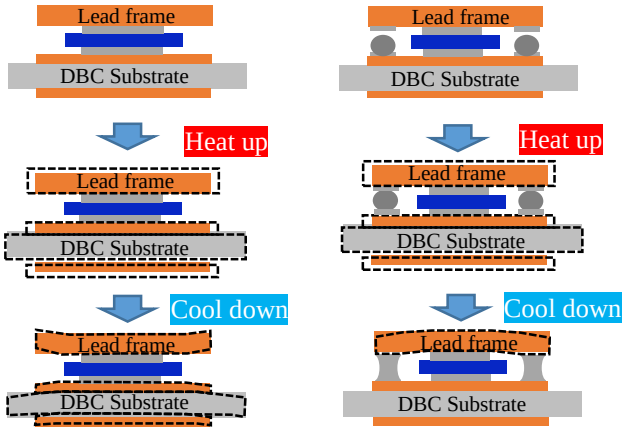

Fig. 6. Deformation (dashed line) in double-sided module without (a) and with compressive posts (b).

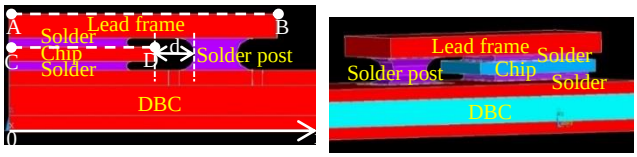

Fig. 7. Side view of the ANSYS simulation model (a) and the simulation model with four posts with dimensions in TABLE II.

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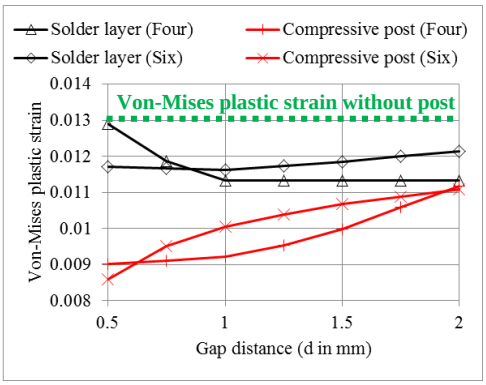


Fig. 8. Simulated Von-Mises plastic strains at the top solder layer and compressive post in Fig. 7.

Because the substrate and lead frame cover the die, the packaged chip is invisible after packaging. The height displacement of the copper lead frame was used to gauge the residual thermo-mechanical stress in simulation and experiment. Fig. 9 shows the simulated displacement along line AB in Fig. 7(a) when the temperature is stepped from 180ºC to 30ºC to emulate a cooling phase of the reflow profile. The measured displacement is plotted from the center to the edge of the module. When there is no post, the edge of the lead frame curves up by 3.25 µm as suggested by Fig. 6(a). The edge curves up by 0.70 µm and curves down by 3.70 µm as the number posts increases to four and six, respectively. Four posts are the safe choice because the high compression force from six posts might damage the chip.

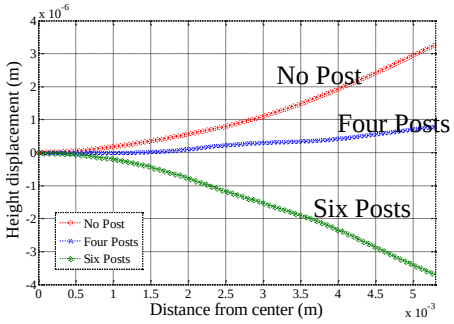
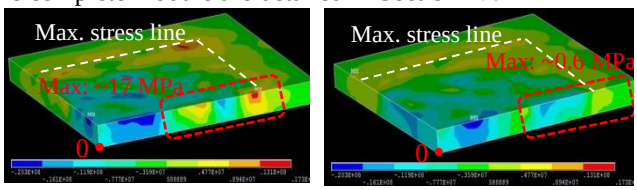


Fig. 9. Simulated vertical displacement of the lead frame along the line $\overline{AB}$ in Fig. 7(a) $(d = 0.75\ mm)$.

The Von-Mises stress on the chip is analyzed in Fig. 10(a) and Fig. 10(b) with conditions of no post and four posts, respectively. The maximum z-directional stress is found at the side of the chip attached to the copper lead frame; the terminating edge of the solder layer (bordered by the dashed line) experiences the highest stress. The maximum stress without the compressive posts was about 17 MPa, much higher than the expected strength of the bonding interface (~ 0.7 MPa). The photograph in Fig. 11 confirms the detachment of the bonded chips in the absence of the compressive posts; the cracked interface is consistent with the maximum-stress line in Fig. 10(a). The integration of four posts (Fig. 10(b)) reduces the maximum z-directional stress to 0.6 MPa; the line of maximum stress remains the same. The photograph in Fig. 12 confirms the integrity of the package after the addition of four compressive posts. The current-voltage characteristic and the breakdown voltage of the complete module are detailed in Section IV.



(a) (b)

Fig. 10. Z-directional stress in the chips (Fig. 7) without post (a) and with four posts (b).

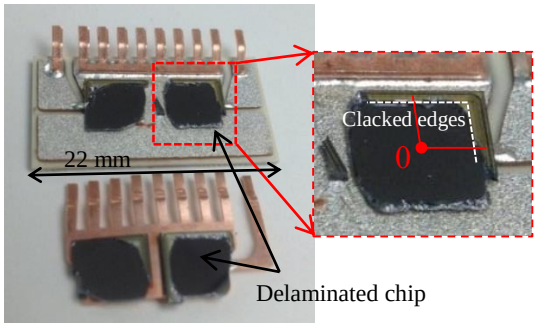


Fig. 11. Delaminated bi-directional dies without post (refer to the simulation result in Fig. 10(a)).

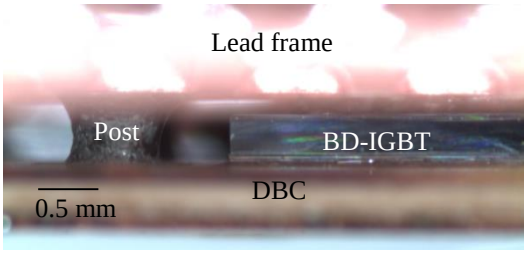


Fig. 12. Packaged bi-directional dies with four posts as modeled in Fig. 7 (refer to the simulation result in Fig. 10(b)).

C. *Experimental Verification*

Test samples with dummy dice and different numbers of posts were fabricated to verify the concept. Fig. 13 shows the fabrication steps. Silver-coated DBC substrates were prepared by wet-etching, and Cirlex fixtures were designed by for alignment of posts and chip. Solder preforms ($Sn_{63}Pb_{37}$) for attachment of die and solder balls were perforated to keep the solder balls in position. The surfaces of the copper lead frame were plated by Ni-Au to protect the surface from oxidization, and to keep the surface reflective for the curvature measurement by three-dimensional optical surface profiler (Zygo NewView™ 7300).

Fig. 14 shows the packaged samples with four and six posts. The surface curvature was measured before and after

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packaging along the line indicated in Fig. 13(d). The measurement results of three samples are shown in Fig. 15.

Since the curvature measurement shows the relative height differences on the surface, the differences between the minimum height and the maximum height were monitored. In the sample without post, the edge of the lead frame was bent up by 13.5 µm, implying residual tensile stress to the chip. The sample with four posts was still bent up at the edge, but the height difference was 5 µm, 37% of the no-post condition. When six posts were packaged with die, the edge was bent down by 17.5 µm. Even though experimental numbers are larger than the simulated values in Fig. 9, the impact of the number of posts on strain magnitude and polarity has been affirmed.

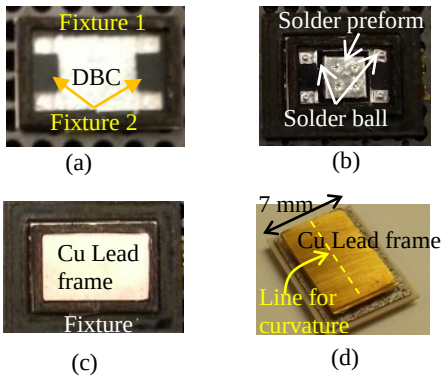

Fig. 13. Fabrication process of the samples for curvature measurement: (a) DBC substrate with fixtures, (b) solder balls and preforms, (c) Ni-Au-coated copper lead frame, and (d) packaged module after solder reflow.

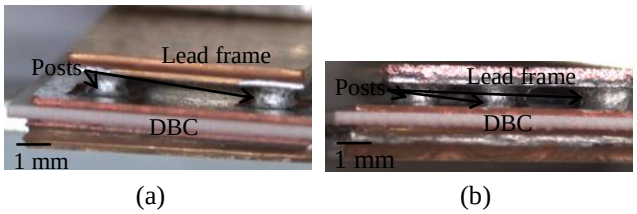

Fig. 14. Packaged samples for curvature measurement with four posts (a) and six posts (b).

IV. Experimental Double-Sided Module

Wafer-bonded symmetrical dies (1.2 kV / 25 A) were packaged to demonstrate the concept in a realistic module. High-temperature solder balls and tin-lead solder were used to form the compressive post, and the diameter of the solder ball was chosen to be 80 µm smaller than the total height of die and interconnection layers. The solder balls expand more than silicon during the heating phase of reflow process and contact the lead frame to maximize compressive force. The specifications of the packaging materials are listed in TABLE II.

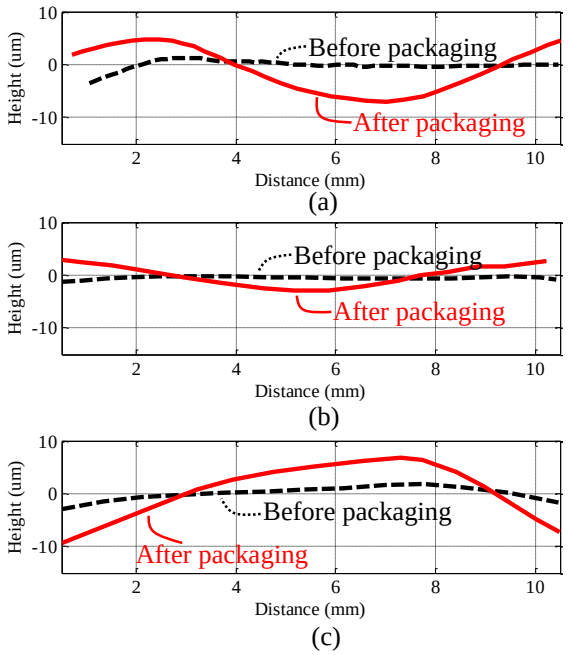

Fig. 15. Measured curvature of the test modules before and after packaging: (a) no post, (b) four posts, and (c) six posts.

TABLE II
Specifications of the Packaging Materials [16]

Layer	Material	Dimensions (mm^3)	CTE (ppm/°C)
DBC substrate	Al_2O_3	24 x 14 x 0.32	8.1
	Copper	23 x 13 x 0.127	16.4 to
Die attach	$Sn_{63}Pb_{37}$	5 x 5 x 0.2	18.7 to
Chip	Silicon	6.6 x 6.6 x 0.4	2.25 to
Lead frame	Copper	23 x 13 x 0.5	16.4 to
Compressive	$Pb_{93.5}Sn_5Ag_{1.5}$	0.72 mm diameter	~23

Fig. 16(a) and Fig. 16 (b) show the packaged module before and after the encapsulation. The molding compound (E-60NC) was deposited by potting. Cirlex fixtures were used for aligning die, solder preform, lead frame, and the gate pads (1 mm x 1 mm) of the BD-IGBT.

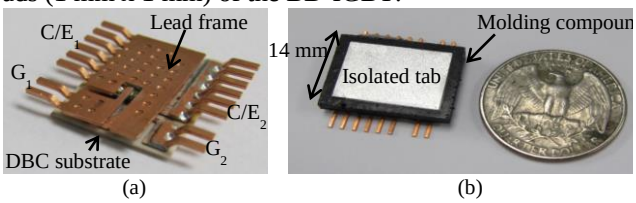

Fig. 16. Developed double-sided module with compressive posts before (a) and after (b) encapsulation.

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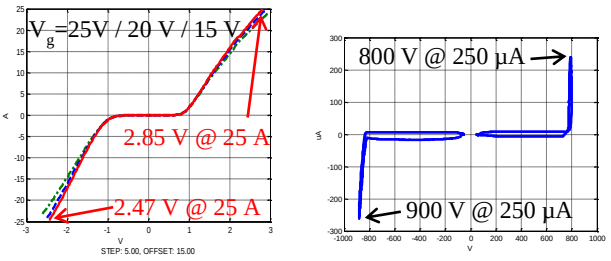
To verify the functionality of the packaged module, I-V characteristic and breakdown voltage were measured for both forward and reverse conductions. The I-V curve for forward conduction in Fig. 17(a) was measured by shorting back gate to drain, and applying 15 V to 25 V gate signal to the top gate. The reverse condition was measured in the same way.



(a) (b)

Fig. 17. Measured on-state voltage drop (a) and breakdown voltage of the developed module (b).

V. Conclusion

Compressive post has been investigated as a means to reduce residual thermo-mechanical stress in a power-electronic module. Because the mismatch among CTE's result in asymmetrical shrinkage during cooling phase, especially in double-sided packaging process, a chip could warp or crack due to residual stress.

For the 6.6 mm x 6.6 mm die studied, the optimal arrangement would place four posts symmetrically around the chip, each post at a distance between 0.75 mm and 1 mm from the chip's edges. The bonded chips no longer detached and the module fully functioned after being sandwiched between a DBC substrate and a copper lead frame. The Von-Mises plastic strain at the die-attach layer was reduced to 87.69% of the strain without compressive posts, implying enhanced fatigue lifetime of the joint.

To verify the compressive force by the posts, curvature change of the lead frame was measured as an indicator of the thermo-mechanical stress at the chip. As the number of posts increased, the curvature at the edge changed from upward to downward as tensile stress became compressive stress.

Both simulation and experimental results prove that the compressive posts alleviate the tensile stress in a package and enhance the reliability of the module.

Acknowledgment

This work was supported by Advanced Research Projects Agency – Energy (ARPA-E) under award DE-AR0000213.

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