# Cost Analysis of TSV Process and Scaling Options

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## Abstract

SEMATECH evaluated the impact of various process options on the overall manufacturing cost of a TSV module, from TSV lithography and etch through post-plate CMP. The purpose of this work was to understand the cost differences of these options in order to identify opportunities to significantly reduce cost. Included in this study were multiple process and materials options for TSV etch, liner, and barrier/seed (B/S). For each of these options, recipes were adjusted for post-etch clean, ECD Cu fill and CMP overburden, and the resulting cost impacts were evaluated. The TSV dimensions used in this study are 5x50 µm and 2x40 µm.

These cost comparisons included a sensitivity analysis, highlighting the main factors responsible for the differences. Cost of materials, tool cost, and throughput were the primary factors affecting cost differences, especially in barrier/seed deposition. In some cases the contributions from both these sources were comparable.

We explain the assumptions used and some of the uncertainties inherent in this work. For example, where materials costs were significant, we extrapolated the cost of new materials from research quantities to those needed to support high volume manufacturing. We had to estimate throughputs and materials costs using our best engineering judgment, because the recipes have not yet been optimized. We also considered that the tools used on some non-critical steps might be fully depreciated, or a lower cost tool such as is used in wafer level packaging. Despite these uncertainties and assumptions, we were able to extract some fairly clear conclusions.

The process options include the following B/S variations: For 5x50 µm TSVs, the B/S film structure is TaN/Ta/Ru/Cu, and the options are with and without the Ru and/or Cu layers. For 2x40 µm TSVs, the B/S structure is TaN/Ru/Cu, with different thicknesses of Ru, and the Cu is an optional seed layer for the field. We also discuss the impact of scaling the TSV dimensions on manufacturing costs. This work is continuing to look at different process options and to apply this methodology to MEOL modules such as temporary bond and debond, wafer thinning, and TSV reveal.

## Key words

Cost model, cost of ownership, through-silicon via, 3D, electrochemical deposition, barrier-seed, ruthenium, CMP, wet cleans

## I. Introduction

In this paper, SEMATECH evaluates how various process options impact the overall cost of the TSV module for both 5x50 µm (diameter x depth) and 2x40 µm processes. These process options include multiple options for etch, liner, and barrier/seed deposition (E/L/B/S), cleans, electrochemical deposition, copper (Cu) fill, and chemical mechanical polishing (CMP), with overburden recipes adjusted for E/L/B/S options. The goal is to understand cost impacts of various options including tool cost, throughput/throughput-limiting steps, materials cost, and the impacts of these factors on downstream processing. More importantly, understanding these impacts helps to identify opportunities to significantly reduce cost. The model is useful when down-selecting technology options by cost and identifying high cost-of-ownership (CoO) steps or modules.

There have been other recently published studies of TSV (through-silicon via) manufacturing costs [1]. This work has been done independently, reaches some different (and some similar) conclusions, and will therefore serve as useful point of comparison to help the 3D-IC community better interpret these cost projections.

### *A. TSV Via-Mid Process Flow*

The process steps that comprise the TSV via-mid flow are show in Table 1. These steps do not represent the full CMOS integration flow and do not include MEOL (mid-end-of-line) processes such as temporary bond/debond (TBDB), wafer thinning, or backside processing including redistribution layer (RDL) and bump formation.

Table 1—TSV via-mid flow and options

| | |
|---|---|
| 1 | TSV lithography (5x50 µm and 2x40 µm) |
| 2 | TSV etch (non-Bosch) |
| 3 | Wet clean |
| 4 | TSV metrology |
| 5 | Liner (oxide or polymer) |
| 6 | Barrier/Seed (multiple options: PVD/CVD/ALD) |
| 7 | ECD (with/without pretreatment) |
| 8 | Anneal |
| 9 | CMP (varies according to B/S material and thickness) |
| 10 | Inspection |

## II. Cost Analysis Methodology

Costs are estimated based on a tool set that is configured to run a single process step in HVM, or 25,000 wafer starts per month (wspm). SEMATECH's process flow, in collaboration with our associate members and partners at CNSE, was the starting point for tools and processes in the cost analysis. Contributors to the cost analysis were requested to provide the tool configuration based on the assumptions used in the model. Some material costs, e.g. chemical vapor deposition (CVD) precursors, electrochemical deposition (ECD) chemistry, and CMP slurries, were cost-adjusted from current research quantity cost to projected HVM quantity cost, by reducing their costs up to 30%.

Cost inputs requested from contributors include the budgetary purchase price (list price, not a negotiated price), tool footprint, chamber configuration, throughput in wafers per hour (wph), and if applicable, a throughput limiting step, and material usage and/or costs.

Cost estimates for the TSV etch are based on data provided by the supplier of a pre-production, non-Bosch etch tool. While a Bosch-etch process is predominantly used in the 3D-IC community, similar data were not available for this analysis. Cost differences between the Bosch and non-Bosch process would predominantly be dependent on throughput. Material costs are based on etch gas consumption, with quotes provided by the gas supplier.

The wet clean tool was configured with 12 chambers, was fully depreciated, and material costs were negligible. Cost inputs were obtained for 5x50 µm non-Bosch processes, and extended to other cleans processes, pending further modification.

In the cost modeling of barrier/seed deposition, inputs were obtained from the supplier, with the tool configured for 4 or 6 deposition chambers (PVD, CVD, and ALD). Throughput is limited by Ru deposition (either 3 or 6 nm). The cost of Ta precursors is estimated to be reduced by 25% when the process reaches HVM. In the case of the B/S process, the PVD tool that deposits field Cu is fully depreciated.

In the assumptions for ECD, inputs were obtained from the supplier for multi-cell tool plating up to 30 wafers simultaneously. Plating times depended on TSV dimensions, but are independent of the of B/S option. Plating times assume that field copper is used, which allows

uniform Cu fill with the current chemistry, tool, and process.

Inputs for the ECD chemistry were obtained from the tool supplier based on the current tool configuration and projected bath lifetimes. Chemistry costs are independent of TSV dimension and B/S option. Material costs are considered an estimate for HVM.

Throughput inputs and material costs for CMP were based on engineering estimates of the impact of varying Cu overburden, B/S composition and thicknesses. The tool has 4 platens (typically, 2 are used for Cu and 2 for B/S polish), with 4 additional cleaning stations. Material costs include slurries, pads, conditioners, and other consumables. Material costs are reduced to reflect likely HVM cost scenarios.

*A. Cost Model Background*

The cost model uses the Excel version of SEMATECH's "Cost Resource Model" (CRM), which was originally developed in 1991 using VisualWorks 2.0/2.5 from ParcPlace Systems. It was re-cast as an Excel workbook in 2007 in order to make it easier to use for assessing the incremental cost of process modules and for sensitivity analyses, rather than total factory costs. During the early 1990s, the software was licensed to Wright Williams and Kelly (WWK) so that it could be adequately supported as a commercial product.

*B. Tool Availability*

Regarding tool availability, all costs except materials (i.e. depreciation, maintenance, labor, and space) are inversely proportional to throughput and tool availability. The model assumes a "high volume limit," where all tools are fully utilized or shared, so costs are independent of wspm. This is appropriate for throughput A/throughput B comparisons, but this underestimates costs. Shown in Figure 1 are possible allocations of tool time. E10_Down corresponds to the fraction of time a tool is unavailable due to maintenance and/or repair while E10_Eng corresponds to the fraction of time a tool is unavailable due to engineering activity according to SEMI E10. In the cost model, 72% productive time was used.

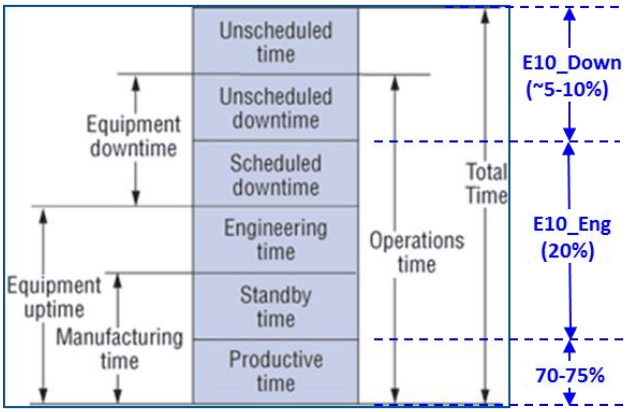


Figure 1: Depiction of tool time allocation segments.

*C. Material Costs*

Although not a detailed cost-of-ownership, material costs are estimated per wafer, assuming high volume (25,000 wspm). The model focuses on significant consumable (e.g. etch gases, precursors, plating chemistry, CMP slurry and pads, etc.), not including replacement parts, electricity, and DI water. Some materials are projected for high-volume manufacturing.

*D. Depreciation and Maintenance*

Capital cost is defined as purchase price plus installation cost (10% of purchase price) with 5 year straight line depreciation (20% for the first 5 years, 0% thereafter). Annual maintenance costs are 7% of capital costs. Fully depreciated tools have depreciation and maintenance costs reduced by a factor of 4, or (20+7)/7.

*E. Space*

The model calculates the space cost as construction costs amortized over 25 years for cleanroom, non-cleanroom, and non-manufacturing spaces. Also included are occupancy rates for cleanroom, non-cleanroom, and non-manufacturing spaces. There are also multiplier rates for cleanroom and non-cleanroom spaces for supporting equipment.

*F. Labor (Direct and Indirect)*

The model defines the personnel cost as the labor rates for engineers, maintenance support, and operators. The model does not include "product personnel" and "facility personnel" options.

*G. Yield*

Yield loss costs are not included in analyses. We did not include yield loss costs because we cannot make a meaningful estimate of the difference in yield of the different process options. However, it is important to point

out that any significant yield differences would dominate the cost comparisons [3].

## III. Cost Modeling Results

### *A. Lowest Cost 5x50 μm TSV Process*

For a 5x50 μm TSV non-Bosch process, with 500 nm SACVD oxide liner and an all PVD B/S process (30 nm TaN/30 nm Ta/0 nm Ru/300 nm Cu seed), B/S deposition and CMP are the two highest cost steps (Figure 2). CMP cost is dominated by material costs; B/S cost is dominated by both materials as well as tool cost and throughput limitations. Ta precursor cost was estimated as 75% of today's cost in HVM. CMP slurry and pads are also estimated at 75% of today's costs. Similar calculations are used to estimate the ECD chemistry cost. Thus, the greatest opportunities for cost improvement are associated with reducing B/S and CMP cost.

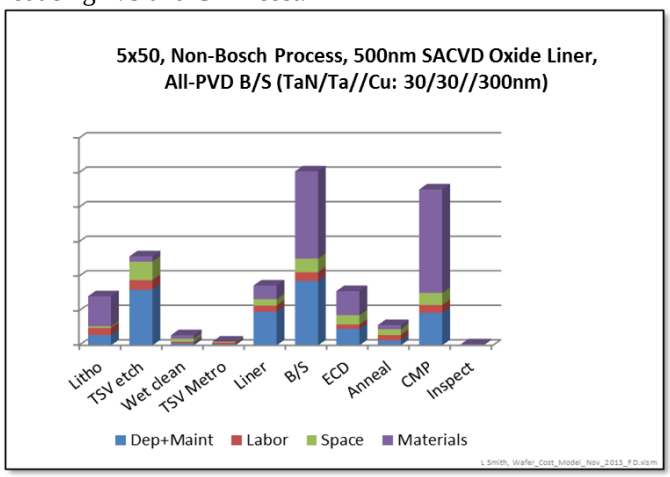


Figure 2: The relative 5x50 μm TSV via-mid non-Bosch process flow cost per wafer by manufacturing step.

The breakdown of the total cost per wafer by process step for the 5x50 μm, non-Bosch process is shown in Figure 3, with B/S and CMP comprising over 50% of the total cost.

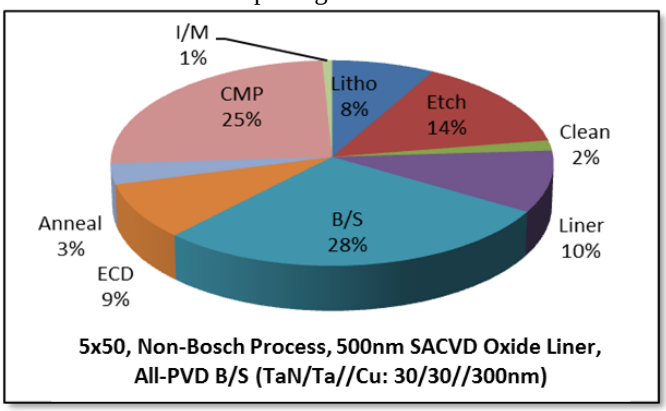


Figure 3: The percentage of the total 5x50 μm TSV via-mid flow cost per wafer by process step.

The cost per 5x50 μm TSV via-mid wafer by component is shown in Figure 4. Material costs are predominantly from B/S and CMP steps. Depreciation and maintenance, and materials costs account for 80% of the total cost per wafer. Throughput improvement would reduce all cost components except material costs.

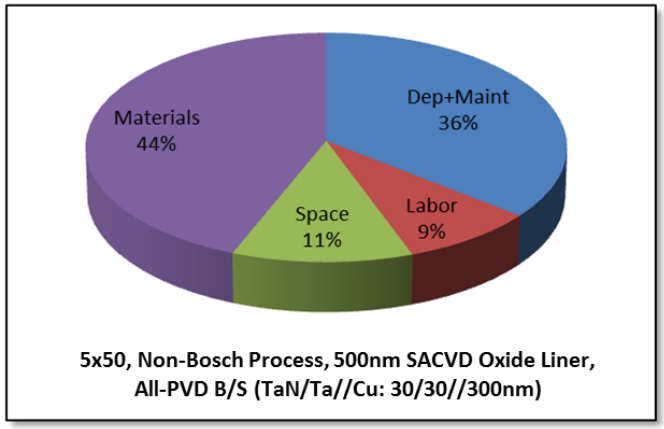


Figure 4: The total 5x50 μm TSV via-mid flow process cost by component.

#### *1) 5x50μm TSV Process Variations*

*a) Effect of Ru Seed Layer Addition to 5x50 Baseline*

Barrier/seed layer deposition costs increased 50% when a 3 nm Ru seed layer was added to the baseline process (30 nm PVD TaN / 30 nm PVD Ta / / 300 nm field Cu, or 30/30//300) to form 30/30/3/300) as shown in Figure 5. This is mostly due to the additional Ru deposition tool cost and the effect on throughput. In addition, CMP costs increased ~7%, mostly due to materials. The ECD cost remained unchanged.

*b) Effect of Replacing 300 nm Cu with 3 nm Ru*

The 300 nm field Cu (30/30/ /300) can be replaced with a 3 nm Ru layer (30/30/3) with a 5% effect on cost. The reduced B/S throughput (B/S wph) of the Ru process is partially offset by lower B/S material (B/S mat) cost (Figure 5). In addition, the ECD throughput cost (ECD wph) increases by 4% due to the addition of a pre-treatment step in one cell whereby surface native oxides are reduced prior to plating.

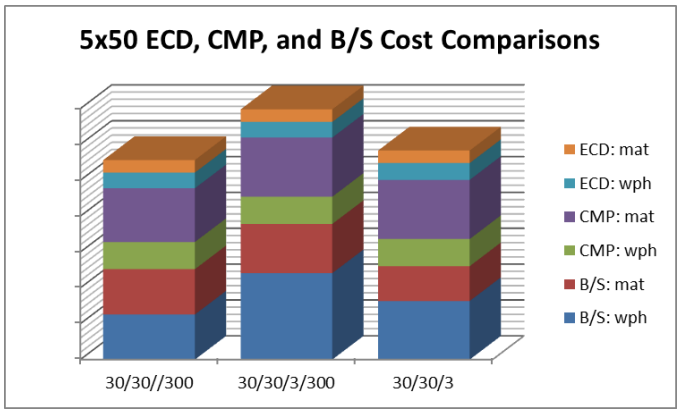


Figure 5: Cost comparison when including addition of 3 nm Ru seed layer (TaN/Ta/Ru/Cu).

*B. Lowest Cost 2x40 μm TSV Process*

For a 2x40 μm TSV non-Bosch process with a novel 100 nm vapor deposited polyimide (VDP) oxide liner and a 6 nm TaN ALD/3 nm CVD Ru process, B/S deposition and CMP were the two highest cost steps (Figure 6). VDP was included in the cost model because of its excellent sidewall step coverage in high aspect ratio TSVs and low temperature deposition process. B/S deposition cost was dominated by materials as well as tool cost and throughput. CMP was dominated by increased material costs. The etch cost per wafer increases slightly for the 2x40 μm TSV, mainly due to material cost increase and an appreciable drop in throughput. Cleans costs are based on 5x50 μm inputs.

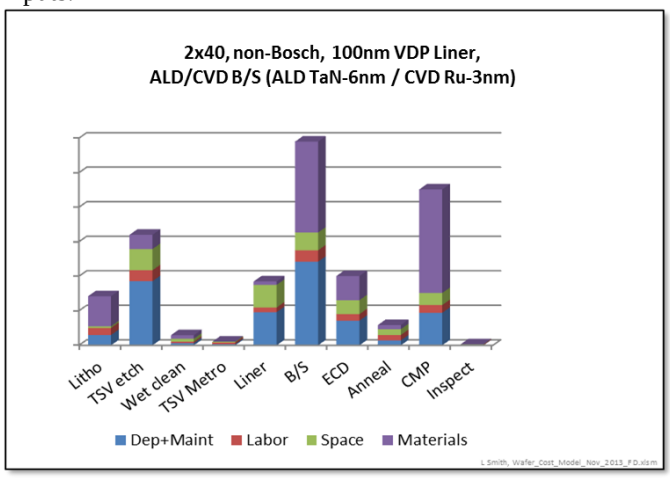


Figure 6: The relative 2x40 μm TSV via-mid non-Bosch process flow cost per wafer by manufacturing step.

The breakdown of the total cost per wafer by process step for the 2x40 μm, non-Bosch process is shown in Figure 7, with B/S and CMP comprising over 50% of the total cost, similar to the 5x50 μm TSV case. The B/S cost per wafer increases compared to the 5x50 μm TSV, mainly due to a significant reduction in throughput for the 2x40 μm TSV wafer process.

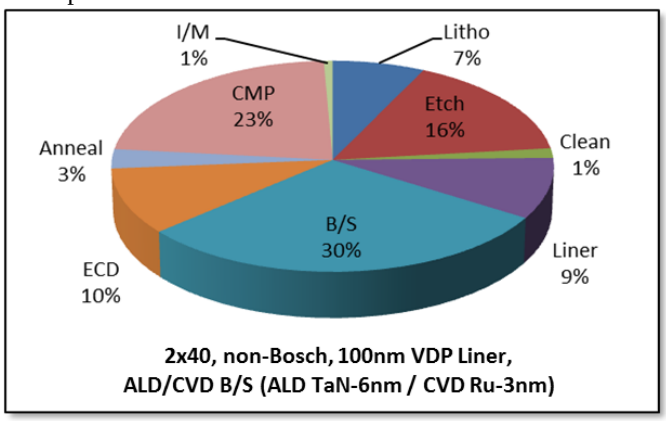


Figure 7: The percentage of the total 2x40 μm TSV via-mid flow cost per wafer by process step.

The cost per 2x40 μm TSV wafer breakdown by component is shown in Figure 8, and is similar to the costs associated with the 5x50 μm TSV process shown in Figure 4. Material costs are predominantly from B/S and CMP steps.

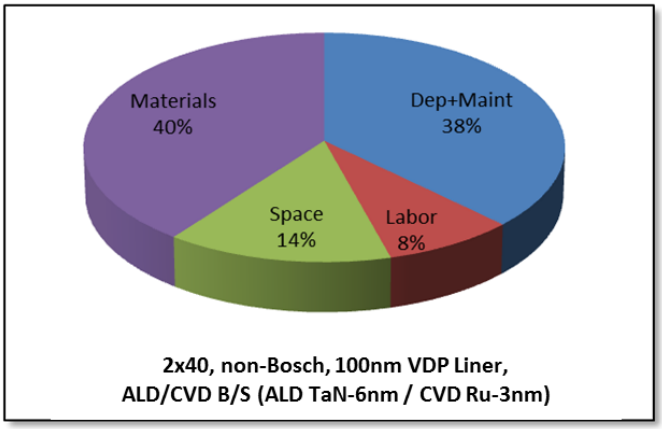


Figure 8: The total 2x40 μm TSV via-mid flow process cost by component.

*1) 2x40μm TSV Process Variations*

*a)Thinning Ru from 6 nm to 3 nm*

There are several cost effects of thinning Ru from 6 (B/S:6/6) to 3 nm (B/S:6/3) in Figure 9, including reducing B/S deposition costs by ~30%, mostly due to the increase in throughput. CMP costs are reduced by ~13%, mostly due to a reduction in material costs; ECD cost is unchanged.

*b) Addition of Cu Flash in BEOL tool*

The addition of 100 nm PVD Cu flash to the B/S module (B/S:6/6/100) to reduce the terminal effect (voltage drop across the wafer from edge to center resulting in non-uniform Cu deposition) during TSV Cu fill, also shown in

Figure 9, increases B/S processing cost by ~35% compared to B/S:6/6, mostly due to increased tool cost and size of the two additional chambers. Adding Cu flash to a fully depreciated BEOL tool (B/S:6/6+S:100) increases B/S cost only by ~8% compared to B/S:6/6.

*c) Cost Impact of Pretreatment in ECD Tool*

Pretreatment in an ECD tool requires an additional cell, with an additional cost of about 2-3%. The 4 B/S options shown in Figure 9 include pretreatment in one ECD cell.

*d) Cu Flash vs. Thicker Ru*

The relative cost effects of a thicker Ru seed layer (B/S:6/6) vs. 100 nm Cu flash (B/S:6/6/100) to reduce the terminal effect shown in Figure 9 results in comparable cost using a B/S tool. It is very cost effective when using a fully depreciated BEOL tool (B/S:6/6+S:100).

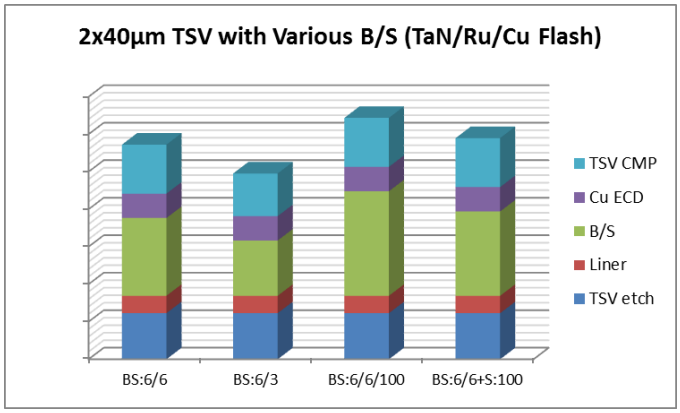


Figure 9: Relative cost effects of B/S changes to reduce ECD terminal effect on 2x40 µm TSV modules (Ta/TaN/Ru/Cu)

*C. 5x50µm (30/30/3) – 2x40µm (6/3) Cost Comparison*

A comparison of the 5x50 µm (30/30/3) and 2x40 µm (6/3) TSV module in Figure 10 indicates that the relative cost differences are negligible, as the increased cost of the Ta precursor is offset by reduced liner and CMP costs. The processing costs that show the most variation are B/S mat and B/S wph CMP costs are not affected much by varying the seed layer thickness. The difference between a 6/6 2x40 mm process and a 6/6/100* in a fully depreciated tool is only 5%.

It may be worthwhile to evaluate the 6/3 B/S for the 5x50 µm TSV, since the cost is comparable to either the 30/30//300 or the 30/30/3 B/S, and the use of same barrier would facilitate scaling.

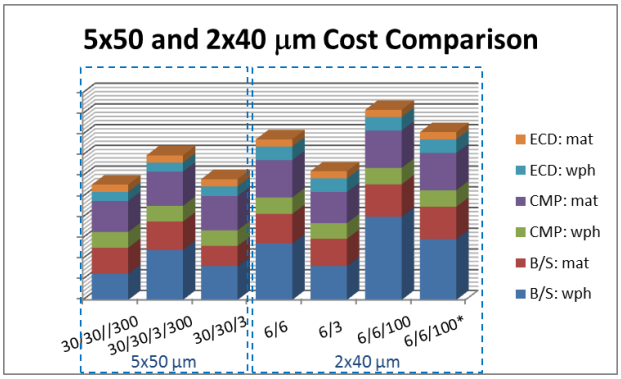


Figure 10: Relative cost effects of process changes on 5x50 µm and 2x40 µm TSV modules (5x50: TaN/Ta/Ru/Cu; 2x40: TaN/Ru/Cu flash); 6/6/100* refers to Cu flash in a fully-depreciated tool.

## III. Conclusion

Based on the SEMATECH model, there are several opportunities for cost reduction, provided there are no reductions in performance, yield, and reliability:

1) 5x50—thinner barrier:

Reduced material cost, improved B/S throughput, reduced CMP cost and improved CMP throughput

2) 2x40—thinner barrier:

Reduced material cost, improves B/S throughput, reduces CMP cost and improves CMP throughput

3) 2x40—thinner Ru-seed:

B/S throughput (representing a 1.67x improvement in wph).

4) VDP oxide liner:

Novel dielectric materials could also function as a barrier. Initial work with VDP suggests this may be possible.

Based on this work, significant cost reduction can be realized by minimizing the B/S and Cu overburden thickness. Reducing this thickness not only lowers the process cost for deposition, but also for CMP. Optimization must consider ECD throughput, yield and reliability.

In addition, TSV scaling only has a minor impact on TSV process cost. TSV scaling may be desirable to minimize keep-out zones and facilitate circuit layout, not just to support higher TSV density.

Similar to previous work [1], our findings indicate that B/S deposition, CMP, and etch are the highest cost process modules. Our conclusions also agree with IMEC's, that B/S and Cu overburden thicknesses should be reduced. However, in contrast to the IMEC work, the cost of the SEMATECH ECD module is lower relative to the other modules.

For the overall 3D-IC cost structure, the FEOL TSV process

costs represent just a piece of the bigger cost structure; for example, MEOL processing (TBDB, thinning, backside processing), assembly and test costs, process and assembly yield loss costs must be considered.

## Acknowledgments

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