Fine Pitch Copper Interconnects for Next Generation Package-on-Package (PoP)

Ilyas Mohammed
Invensas, Inc.
2702 Orchard Parkway, San Jose, CA 95134

Abstract

For low power processors, stacking memory on top offers many advantages such as high performance due to memory-processor interface within package, small footprint and standard assembly. Package-on-package (PoP) is preferred method of stacking as it offers two discrete packages that are tested separately and can be sourced independently. However, current PoP interconnect technologies do not efficiently scale to meet the memory bandwidth requirements for new generations of multi-core applications processors. The current interconnect technologies such as stacking with smaller sized solder balls, using solder filled laser drilled vias in the mold cap, or using organic interposers are not practically achieving the high IO requirements, since the aspect ratios of these interconnects are limited. To address the gap in PoP interconnect density, a wire bond based package stacking interconnect technology called Bond Via Array (BVA^{TM}) is presented that enables reduced pitch and a higher number of interconnects in the PoP perimeter stacking arrangement. The main technological challenges are identified and the research results explained. The three main challenges were forming free standing wire-bonds, molding the package while exposing the tips of the wire-bonds, and package stacking. The assembly results showed that the wire tips were within the desired positional accuracy and height, and the packages were stacked without any loss of yield. These results indicate that the BVA interconnect technology is promising for the very high density and fine pitch required for upcoming mobile computing systems.

Introduction

The mobile computing platforms are moving towards multiple core processors with integrated graphics processors, thereby significantly increasing the processor-memory bandwidth requirements for optimal performance. The bandwidth is typically increased by increasing the memory speed or the number of IO or both. With the power limitations for mobile systems, high speed signaling may not be the preferred method.

One approach to scaling mobile memory bandwidth has been to increase the number of memory I/O by an order of magnitude. This was implemented using Through Silicon Vias (TSV) by Samsung [1]. 512 I/O were used to obtain 12.8 Gb/s memory bandwidth using eight 2 Gb chips stacked and connected through TSV. To allow for about 1200 interconnects between the memory stack and processor, a TSV approach was suggested as shown in Figure 1.

Since the TSV technology is considerably more expensive than PoP due to its relative immaturity, the above approach is not expected as a 3D computing solution for mobile systems over the next few years. In this paper, an alternative interconnect system between the memory and processor is presented that offers the wide I/O capability utilizing widely used and low cost wire-bond technology.

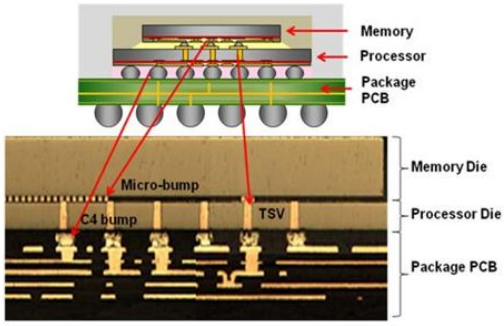


Figure 1: Wide I/O TSV solution [1]

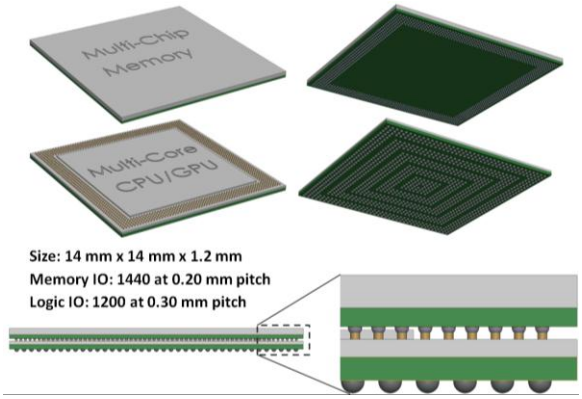


Figure 2: BVA PoP Design Features

Figure 2 illustrates the Bond Via Array (BVA) wire-bond array interconnect concept that will be detailed in this paper. The main features are that the wire-bond extends from the substrate to the top surface of the bottom package to be connected to a

package mounted on top. The BVA interconnects are free-standing wire-bonds formed on the periphery of the top surface of the logic substrate in multiple rows.

The mature wire-bonding technology offers very fine pitch, and free-standing wires are formed using proprietary processes utilizing conventional wire-bond equipment. As the wire-bonds can be done at a pitch as small as 50 µm, and can extend in length to any desired value, the benefits are immediately seen. This interconnect technology lends itself to a wide variety of 3D packaging, including multiple-rows and area array, fan-in and fan-out, flat or step mold, bond wires present on bottom or top package, bottom package face up or down, etc. This does not include other applications besides PoP such as wafer level packaging, embedded packaging, multi-chip packaging, etc., which will not be discussed in this paper. Preliminary and exploratory work done for BVA technology has already been reported [2].

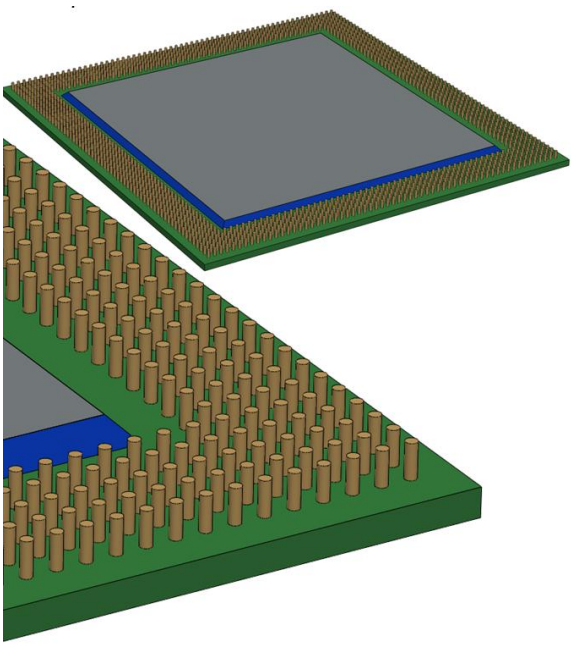
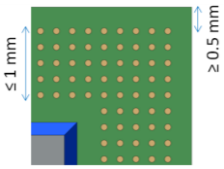


Figure 3: Free-standing wire-bonds around the bottom package

Assumptions:
- Package size: 14 mm x 14 mm
- IO edge to package edge: ≥ 0.5 mm
- IO area width: ≤ 1 mm



Pitch (mm)	No. of IO rows				
	2	3	4	5	6
0.50	200	288	-	-	-
0.40	248	360	-	-	-
0.30	336	492	640	-	-
0.25	408	600	784	960	-
0.20	512	756	992	1220	1440

Figure 4: Maximum possible IO as a function of pitch

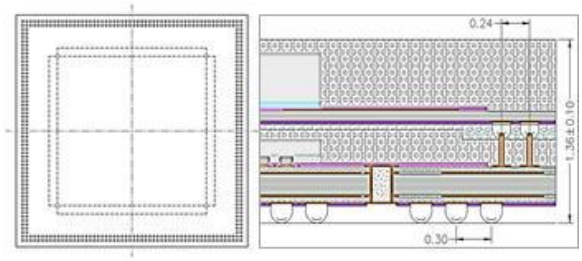
The interconnect scaling capabilities are shown in Figures 3-4. For a given 14 mm x 14 mm package and assuming a 1 mm peripheral width for IO, up to 1440 interconnects can be formed at 0.2 mm pitch. These numbers of IO are enough to meet future wide IO memory requirements.

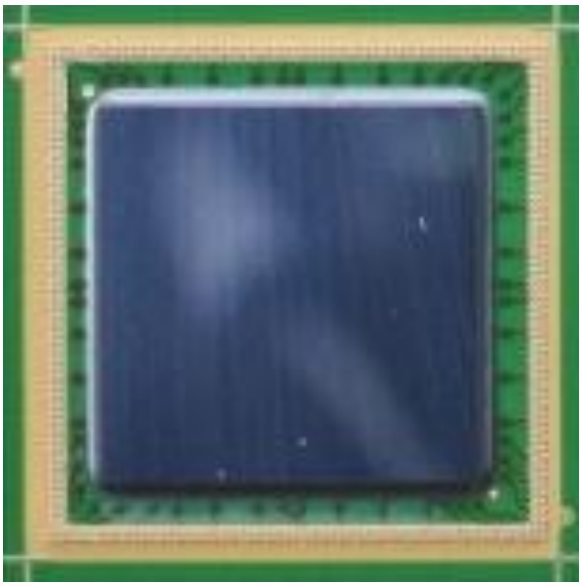
Challenges

The primary challenges related to this technology as applied to PoP are: 1.) how to terminate the wire tip at a prescribed height and X-Y position repeatedly with acceptable tolerances; 2.) how to expose a solderable wire tip above the mold cap, and; 3.) how to connect the top package solder balls to the exposed tip with good yield and reliability. The approach and experimental results for process development addressing each of these challenges are discussed below.

Forming the BVA Copper Interconnect

A BVA PoP daisy chain test vehicle was designed and fabricated that featured bottom package to top package IO pitch at 0.24 mm, which is smaller than any other known PoP interconnect pitch. The test vehicle design and the bottom substrate with processor chip are shown in Figure 5.





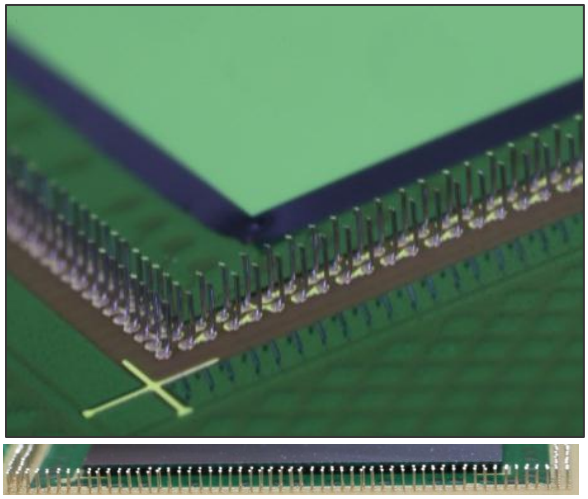


Figure 5: BVA interconnects (free standing wire-bonds) at 0.24 mm pitch around the periphery of the bottom (processor) chip

Copper wire bonding was selected as the method for forming the PoP interconnects as copper provides advantages over gold in cost, stiffness and electrical conductivity. The bonding equipment used was capable of processing copper wire with a maximum diameter of 50µm and hence 50µm diameter wire was chosen to maximize structural strength, electrical and thermal performance.

The free ended wire bonding was further developed to improve wire tip positioning which would be critical to alignment and soldering of the top PoP package. Figure 5 shows 0.4mm high free ended wires produced with these improvements. This implies a PoP interconnect with an aspect ratio (height/diameter) of 8, and pitch ratio (height/pitch) of 1.7, which is not possible using any other PoP interconnect technology.

The free-standing wire-bonds are the most important feature of BVA PoP. Forming the wire-bonds with the tips having good positional accuracy (x and y) and uniform height (z) are important in enabling very fine pitch and high yield package assembly. Wire tip final height measurement data is shown in Figures 6-8 and demonstrates control to within 10%. The data was measured and recorded using an OGP Flash 200. Bonding vertical wires was accomplished using Cu wire bonding equipment. Process conditions were developed and optimized to achieve these results.

The results given in these graphs depict data from 43 packages with each data point on the graph representing all the wire-bonds in one package. The average is the mean value for all the wire-bonds within a package and range is the maximum difference between any two wire-bonds within a package. This data includes the effect of package warpage, hence the reason for high range values. The average data is within 20 µm for all x, y and z positions, which translates to better than ± 10 µm.

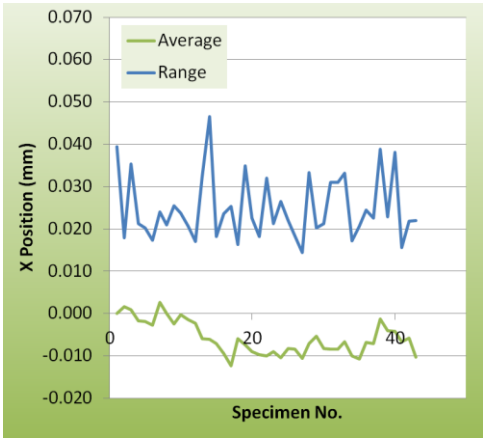


Figure 6: Wire-bond tip measured x-position data

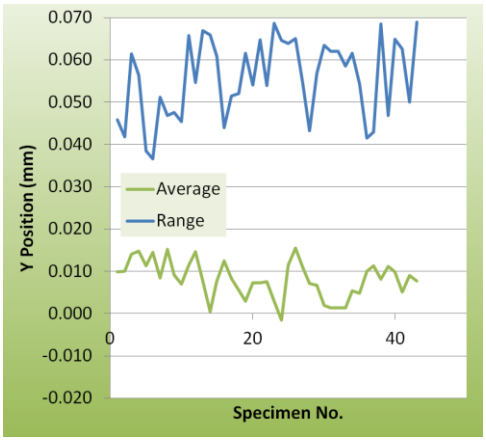


Figure 7: Wire-bond tip measured y-position data

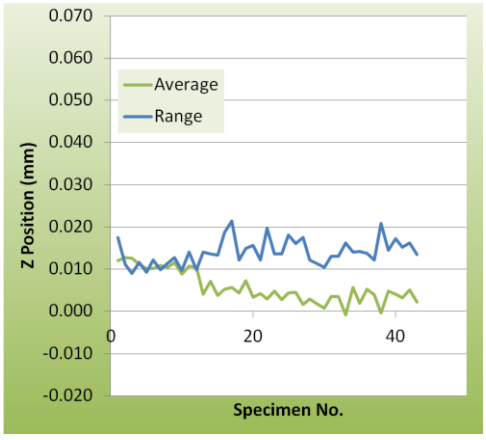


Figure 8: Wire-bond tip measured z-position data

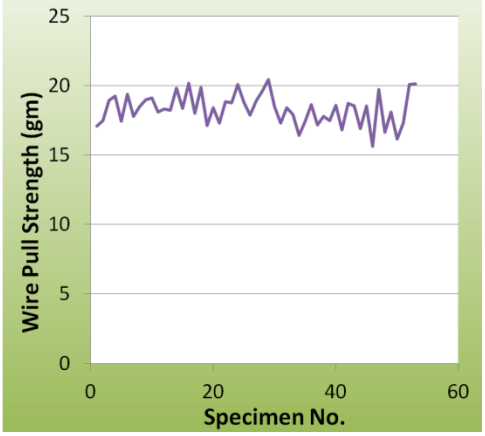


Figure 9: Wire bond pull strength

Bond strength process monitoring was accomplished by performing bond pull testing and by use of a tweezer jaw bond pull test fixture adapted for pulling the free ended wires. As shown in Figure 9, an average of greater than 15 grams was obtained. A cohesive wire break failure indicated that bonds were robust.

Molding and Exposing the Interconnect

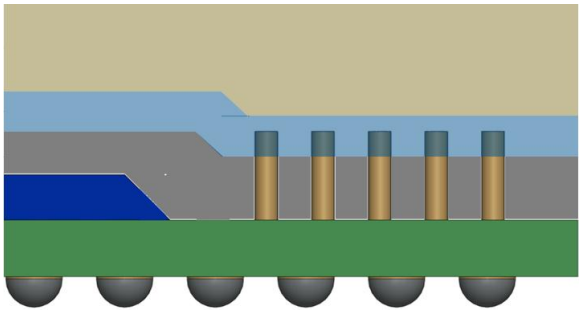


Figure 10: Film assist mold to expose the wire-tips

The next step is to mold the logic package while exposing the BVA tips with a consistent desired height. Film assisted mold technique as shown in Figure 10 was used to expose the tips. It is a mature technology commonly found in many packaging assembly operations and stable supplier support. The process uses a mold chase design with mold cavities only slightly deeper than the formed Cu wires. When the mold is clamped to the substrate, the Cu wires are pushed into the mold film. The mold cavity is filled with the molding compound, the molding compound is cured, the mold is opened and the mold film is pulled away from the package exposing the wire tips. The mold film thickness determines the wire tip exposure. Some process development was needed to optimize the wire tip exposure. No special molding parameters were needed to provide repeatable wire tip exposure results. Figure 11 shows the exposed wire tips. The target value was 0.12 mm and this height was obtained within ± 10 µm as shown in Figure 12.

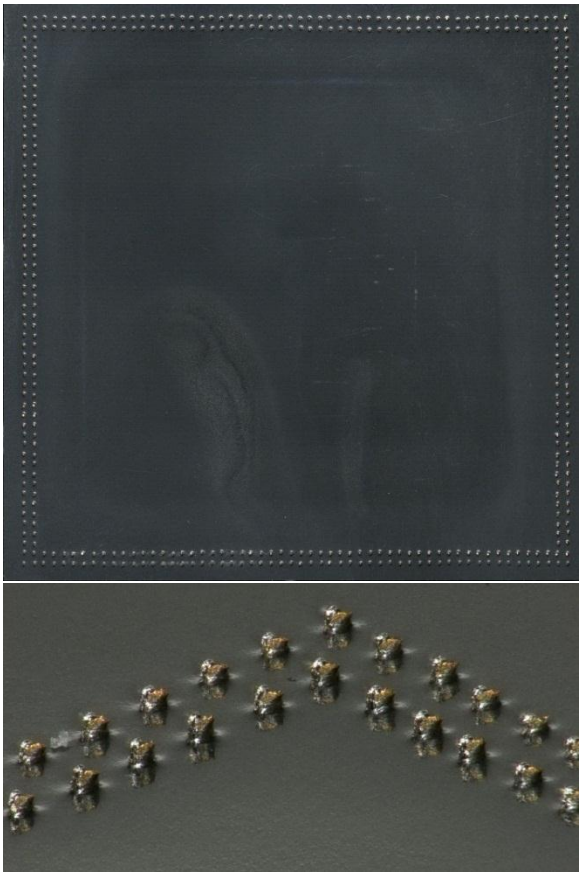


Figure 11: The BVA interconnects exposed on the top surface of the bottom package

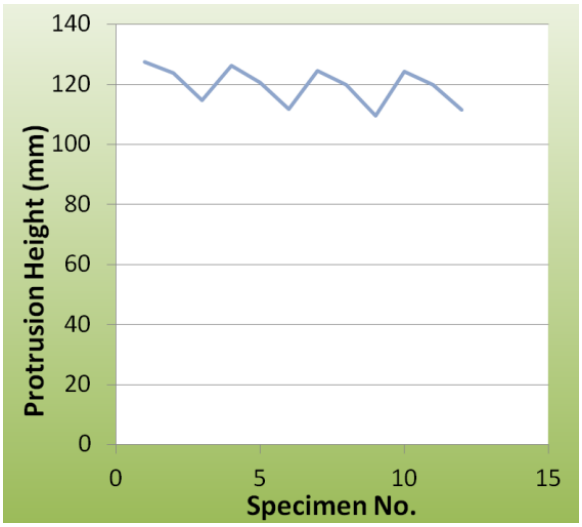


Figure 12: Exposed wire tip height over the mold surface

Connecting Top Package to Exposed Wire Tips

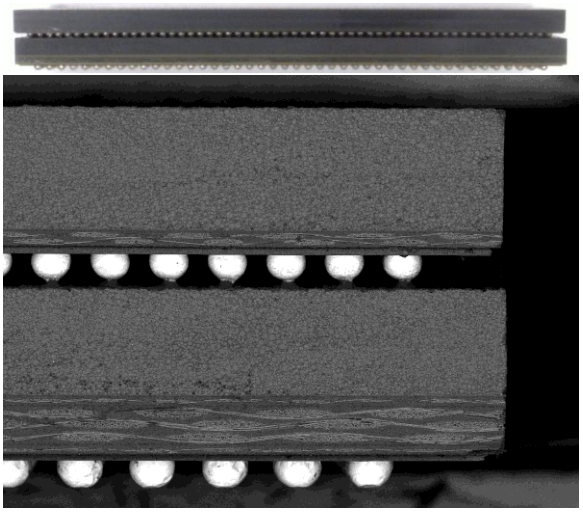


Figure 13: Assembled BVA PoP

The last step is to stack the memory package on top of the logic package, as shown in Figure 13. This process is very similar to conventional PoP assembly where solder paste is printed on the main board, the logic package is placed on the board, the memory package is dipped in solder flux and placed on top of logic package, and the stack is reflowed along with other components on the board. An underfill may be dispensed along the periphery of the stack for high reliability under dynamic loading. Good joints were obtained across all interconnects over the whole package, as shown in Figure 14 depicting 3D, X-ray and cross-section images.

Infrastructure and Reliability

The processes and equipment required to assemble and stack the packages are quite common to typical package assembly lines found throughout the industry. The assembly flow for the PoP bottom package is shown in Figure 15. The process steps highlighted in green are commonly found in packaging assembly factories but not typical to PoP package assembly today. Copper wire formation and film assisted molding if used must be adapted to PoP lines. Design specific tooling may be required for handling for solder ball attach and test to avoid contact with the exposed wire tips. A design specific pick-and-place tool for surface mount may also be needed. A modified flux or paste for stacking will be required if soldering to bare Cu but suitable formulations are available from major flux suppliers. The processes highlighted in blue require no changes at all.

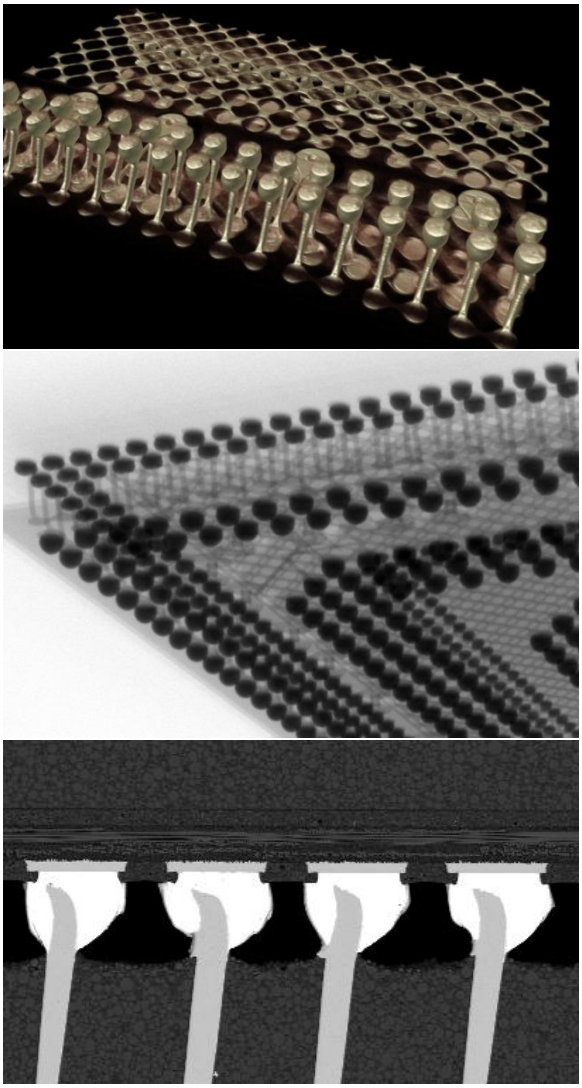


Figure 14: 3D, X-ray and cross-section images of the BVA interconnects to the top package

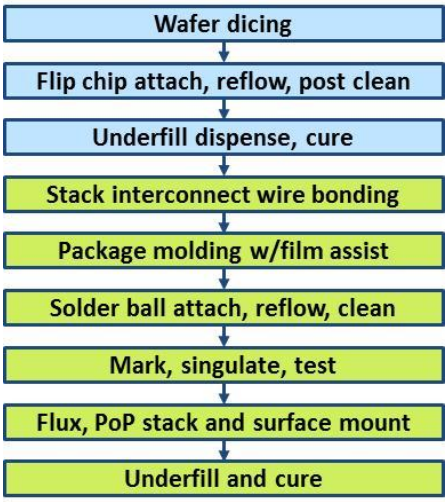


Figure 15: PoP bottom package assembly flow chart.

There was initial concern that the pin tips protruding above the mold cap would be exposed to potential damage in subsequent processes or handling. However, the pin tips proved to be very robust and resistant to harm from handling.

An EMS supplier using commonly found SMT package placement equipment is contracted to do the SMT assembly for the reliability evaluation. The top and bottom package are stacked in place on the test board and reflowed together at the same time the bottom package is reflowed to the test board as is common to PoP board mounting used today.

At the time of the writing of this paper technology qualification samples of the test vehicle design shown in Figure 5 are being assembled and tested. These qualification lots will be subjected to the reliability test plan shown in Figure 16. Results of the sample assembly and technology qualification will be presented at the conference.

Test	Standard	Test Condition	Sample Size
Moisture Sensitivity Level3	IPC / JEDEC J-STD-020C	125°C for 24hrs; 30°C/60%RH for 192 hrs, 3X Pb-free reflow	22
High Temperature Storage	JESD22-A103D Condition B	150°C, 1000 hrs	22
Unbiased Autoclave	JESD22-A102D Condition D	121°C / 100%RH / 2atm for 168hrs	22
Drop Test	JESD22-B111	>30drops, 1500Gs, 0.5mSec of half sine pulse	20
Temperature Cycling (Package Level)	JESD22-A104D Condition B	-55°C to 125°C, 1000 cycles	45
Temperature Cycling (Board Level)	JESD22-A104D Condition G	-40°C to 125°C, 1000 cycles	45

Figure 21: 240µm pitch stack interconnect PoP test vehicle technology qualification test plan.

Conclusions

A novel interconnect is presented that is based on wire-bonds and can be utilized in different applications such as 3D packaging, embedded packaging, wafer level packaging, etc. This technology offers very fine pitch and high IO to enable miniaturized 3D packaging for high end computing systems, including wide IO implementations in PoP. The key benefits of this technology are:

- *High performance:* Ultra-high IO (quad-channel+) between the bottom logic package and the top memory package offers greater than 12.8 Gb/s bandwidth. This is enables through >1000 logic to memory interconnects in a standard 14 mm x 14 mm package at 0.2 mm or smaller pitch.
- *PoP approach:* Independently sourced, packaged, and tested logic and memory for high yield and supply chain flexibility
- *Memory compatibility:* Utilizes current LPDDR2 and LPDDR3, while scalable to wide IO memory devices
- *High-level package reliability and low cost:* Utilizes established assembly equipment, processes and materials with completely molded top and bottom packages for low warpage and standard SMT for high yield.

Detailed research and development efforts were carried out addressing main features of this technology including wire-bond formation, wire tip exposure and solder interconnection. These experiments showed that the wire-tips positions were controlled to within ± 10 µm accuracy and the exposed tips after molding were found to have a consistent height. The stacking showed robust joints across all interconnects between the exposed wire-tips and top package solder balls. The processes were developed utilizing equipment commonly found in packaging assembly factories today thereby avoiding major changes to in-factory and supply chain infrastructure. Further testing is being performed to characterize the 240 µm pitch PoP assembly for high yield and reliability. Available results of further testing will be presented at the conference.

References

[1] Kang, Uksong, et al, "8 Gb DDR3 DRAM Using Through-Silicon-Via Technology", IEEE International Solid State Circuits Conference (ISSCC), February 2009.

[2] Damberg, Philip, et al, "Fine Pitch copper PoP for Mobile Applications", 2012 Electronic Components and Technology Conference (ECTC), June 2012.