Low Cost Glass Interposer Development

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Abstract

For high density interconnection IC packages of the future, the outlook is for thinner packages with higher routing densities. With that, managing the substrate warpage becomes critical. Traditional organic substrates may face several challenges for high density I/Os with very fine line interconnections. Glass is one of the candidates that can be used in substrate industry. The infrastructure of glass for LCD industry has already been developed for many years. Glass also has several superior properties than other substrate candidates, such as large panel size availability, adjustable CTE, high modulus, low dielectric constant, low dielectric loss and high insulating ability.

In this paper, we successfully demonstrate early manufacturing feasibility of glass substrate with 4 build-up layers starting with a thin glass panel of thickness of 200μm in 508mm × 508mm panel size format and under the IC substrate manufacturing environment. Fabrication and electrical results of a test vehicle are documented. The test vehicle includes daisy chains that are connected with 100μm diameter through glass via (TGV) in a 200μm thick glass. The laser via in via technology was adopted for double side electrical connection. The copper line width/space of 8/8μm was demonstrated. The total thickness of 4 layers test vehicle is about 390μm. The warpage of glass in comparison with an organic substrate (BT) with 200μm core thickness is 3X better. Further work is needed to develop, fine tune and assess the detailed manufacturability and reliability concerns.

Based on this work, it is clear that the potential of glass in IC packaging and integration is tremendous in diverse applications for substrate warpage enhancement.

Key words

Glass, Interposer, Panel Size, TGV, Warpage .

I. Introduction

Today's semiconductor packaging and assembly technologies are challenged by a variety of new product requirements. They include fine pitch and high density interconnection, very small and thin outlines, several GHz operating frequencies, high power dissipation, and low production cost. 3DIC integration has been well known as the next generation of semiconductor technology with the advantages of small form factor, high performance, low power consumption, high density integration, etc. However, 3DIC still needs some time to be developed. Current solution is to integrate on Silicon interposer as 2.5D integration. 2.5D Silicon integration can meet the requirements and also achieve heterogeneous integration as system in package (SiP). Silicon interposer can achieve the line width/space less than 1μm/1μm.

Although Silicon interposer has good performance, however high cost is still the major issue and limits its high volume adoption. Therefore to decrease the assembly cost or develop low cost, high density interconnect interposer technology is the keys to enable 2.5D-SiP integration. One possibility is to develop low cost interposer by adopting the alternative materials instead of Silicon. The glass, low CTE polymer material, ceramic, etc. may be included.

Glass represents an attractive choice with potential of tailorable properties dependent on specific glass composition. By targeting the coefficient of thermal expansion (CTE), the CTE of glass can be made to match perfectly with silicon dies and for reliable package. In addition, the advantages of using glass for interposer derive from process flexibility for size and thickness since the glass fusion process provides sheets with dimensions of more than three meters. It is straight forward to provide glass substrate of almost any size needed. Large glass panels are ideally suited for fabrication of interposer where the panel process is expected to provide large number of interposers in each run compared with wafer processing. Additionally, the two sided processing of the panel, the avoidance of CMP processes further enable lower unit cost for the interposer Consequently, glass is an ideal interposer material due to its insulating property, large panel size availability, high modulus and ability to tailor CTE [1-5].

This paper demonstrates the manufacturing feasibility of thin glass interposers with through glass vias (TGV) by Substrate HVM (high volume manufacture) line for 2.5D-SiP application.

II. Panel Level Glass Substrate & Design

Figure 1 shows the glass interposer schematic diagram. 4 build-up layers with TGV structure are on a thin glass panel with thickness of 200μm in 508 mm × 508 mm panel size. ABF dielectric is adopted in this development. The test vehicle includes daisy chains with a diameter of 100μm through glass via. The minimum copper line width/space is 8/8μm.

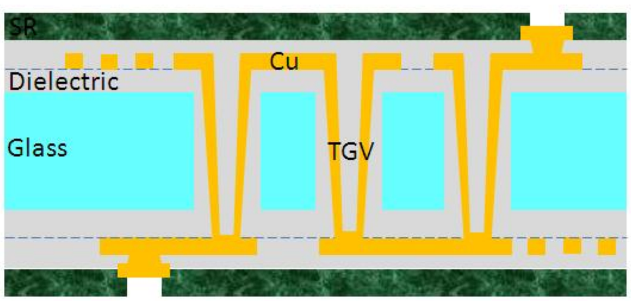


Figure 1: Glass interposer schematic diagram

The laser via in via technology [5] is adopted for double side electrical connection. Substrate SAP (semi additive plating) processes were used to build up this glass interposer, including dielectric lamination, seed layer, lithography, Cu plating and stripping/etching process.. KEYENCE VK-X200 3D Laser microscope measurement system was used for the glass interposer dimension, including line/space, layer thickness, TGV diameter and via in via diameter measurement. Panel warpage performance in SAP process was a key metric. Nikon NEXIV VMR-6555 was used to measure panel warpage data, and Akrometrix PS400 shadow moiré measurement system was used to measure the unit level warpage data.

A. Panel level Glass Interposer Process flow

A glass test vehicle was designed and fabricated to characterize the substrate and TGVs in glass. Figure 2 shows the process flow for fabricating the test vehicle.

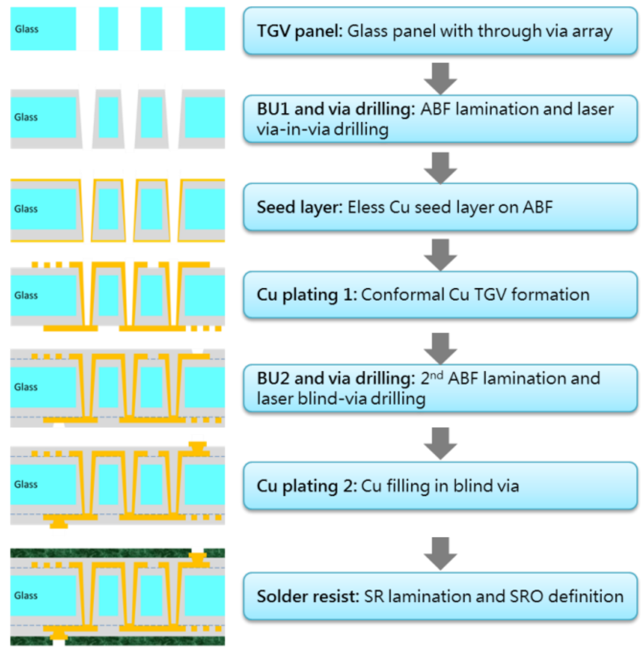
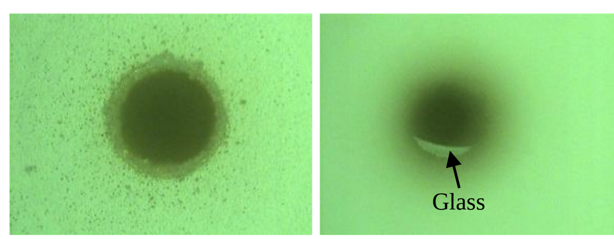


Figure 2: Process flow of fabricating the glass interposer

A 508 mm × 508 mm panel size Corning Willow® glass with a thickness of 200μm and array TGVs was used for the test vehicle fabrication. During the different stages of manufacturing processes, the handling of ultrathin glass substrates was a key challenge. The symmetric ABF lamination enhanced the handling of glass and provided mechanical support to the glass. Via in via of TGV was then formed by UV laser drilling. Accuracy of TGV collocated with via in via played an important role in the manufacturing. Figure 3 compares via in via with good and bad alignment of TGV.



(a) **(b)**

Figure 3: Through via with (a) good and (b) bad TGV alignment.

Metallization of through via and on the surface was carried out by using copper as metal and SAP approach in HVM manufacture line following by ABF desmear and electroless Cu seed layer processes. Early handling approaches led to glass breakage in metallization processes, as shown in Figure 4. However after improved handling techniques it has been shown that we can process 508mm × 508 mm glass panels without breakage, as shown in Figure 5.

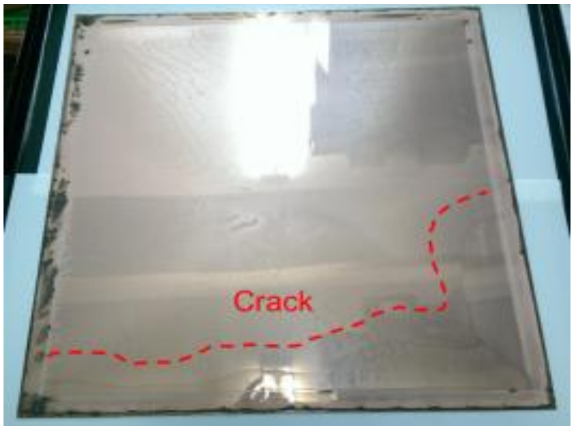


Figure 4: Glass crack occurred in copper plating process

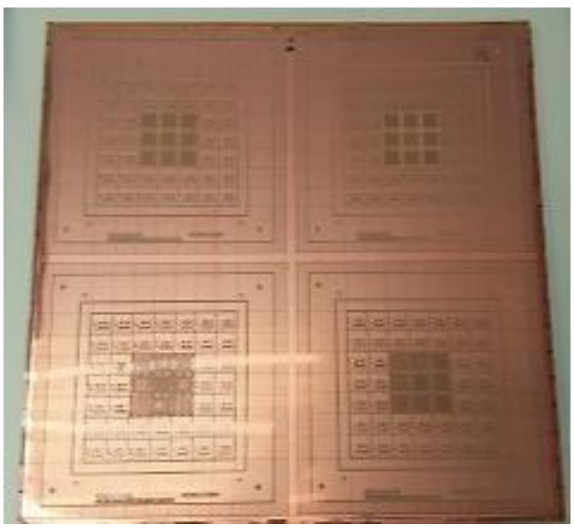


Figure 5: With proper handling and protection methods, no glass cracking seen after Cu plating process

After Cu metallization in the 2nd built-up layer, the process of solder resist and the following organic solderability preservative (OSP) were also carried out in HVM line.

B. *Fabrication Results of Glass Interposer*

The copper line width/space of 8/8µm was realized with 4 build-up layers on a thin glass panel with thickness of 200 µm in 508 mm × 508 mm panel size format as shown in Figure 6. Double side daisy chain with TGV between L2 and L3 metal layers through blind via connected to L1 and L4 layers as shown in Figure 7 (a) and (b).

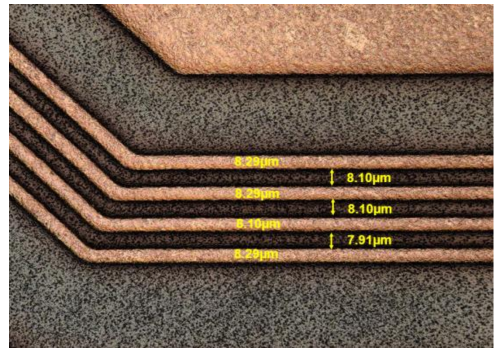
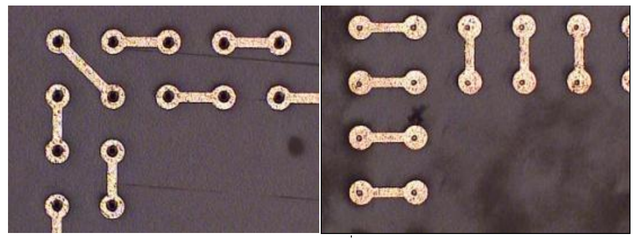


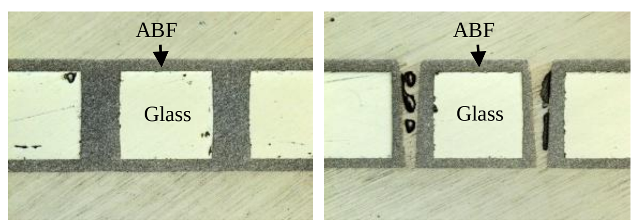
Figure 6: Top view of L/S 8/8µm fine line



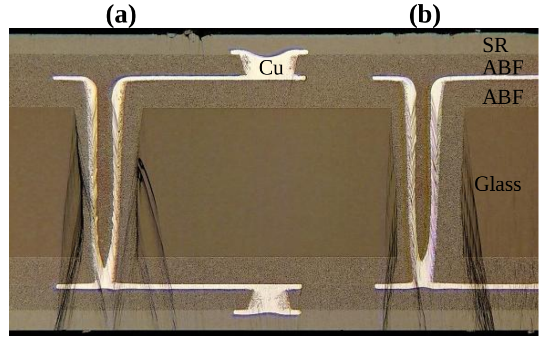
(a) (b)

Figure 7: (a) Top view of daisy chain after build-up layer one (b) Top view of daisy chain after build-up layer two

The glass substrate with diameter of 100µm through glass via (TGV) was laminated by double side ABF dielectric material. Void free filling was realized as shown in Figure 8 (a). The laser via in via drilling presented a 60µm through hole for double side electrical connection as shown in Figure 8 (b). Figure 8 (c) shows the test vehicle with 4 build-up layers through via in via which adopted conformal metallization and blind via connecting by Cu plating.



(a) (b)



(c)

Figure 8: (a) Cross-section after ABF lamination (b)Cross-section after laser via in via drilling (c)Cross-section view after solder resist process

C. Warpage Results

We also compared with the 508mm × 508mm panel size warpage history of 200µm thickness glass substrate and BT base organic substrate which owns similar CTE with glass, as shown in Figure 9. The results shows that the glass substrate has 3X better coplanarity performance than organic substrate after each thermal process including pre-cure and post-cure.

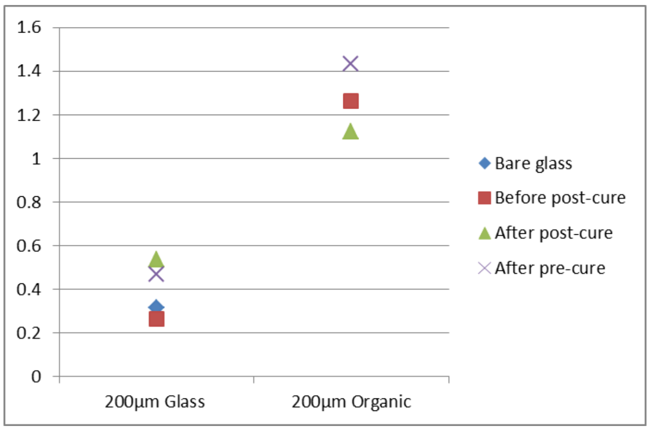
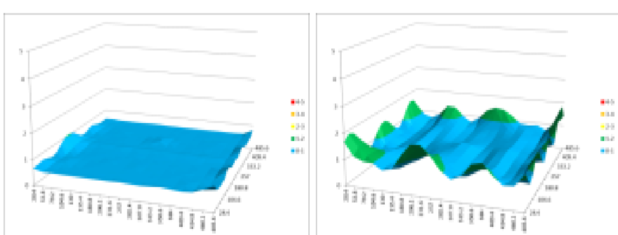


Figure 9: 508mm×508mm panel size warpage history comparison results

The profile of 508mm × 508mm panel size glass substrate of two layers build-up after pre-cure processes is showed in Figure 10 (a), and figure (b) shows the profile of organic substrate after the same processes. The warpage improvement was seen globally (across the large panel) and locally as shown in Figure 10. From lithography perspective, it's important and essential for fine line/space geometry for interposers.



(a) **(b)**

Figure 10: (a)Warpage measurement result of glass substrate after two layers build-up (b)Warpage measurement result of organic substrate after build-up layer 2

Figure 11 presents the shadow moiré measurement data of finished substrate 20mm × 20mm. This includes the complete structure including TGV metallization, metal circuit, dielectric layer, solder mask and surface finish.

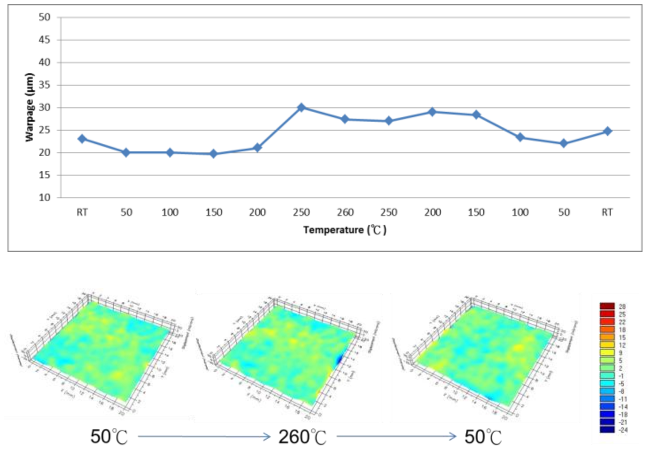


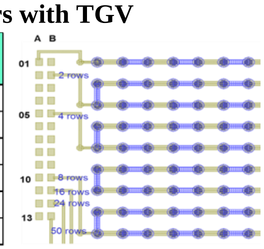
Figure 11: Profile and measurement result of shadow moiré (body size 20 mm×20 mm with 390µm thickness)

The measurement result shows that the maximum warpage was at the temperature 250℃. The average of three units shows around 30 µm. The warpage profile shows no significant variation in temperature ranging from RT to 260 ℃ to RT.

D. Electrical Test Results

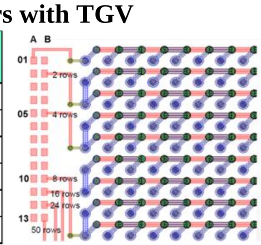
- **Table 1: 2 Build-up layers with TGV**

Port (+)	Port (-)	Chain Rows	Resistance (ohm)
A01	B02	2	2.57
	B05	4	4.87
	B10	8	9.58
	B11	16	19.31
	B12	24	28.93
	B13	50	61.09



- **Table 2: 4 Build-up layers with TGV**

Port (+)	Port (-)	Chain Rows	Resistance (ohm)
A01	B02	2	4.02
	B05	4	7.91
	B10	8	15.16
	B11	16	31.25
	B12	24	47.33
	B13	50	100.43



We adopted the 4 wire electrical test system to verify the stability of fabrication process including build-up layer metallization via in via technology

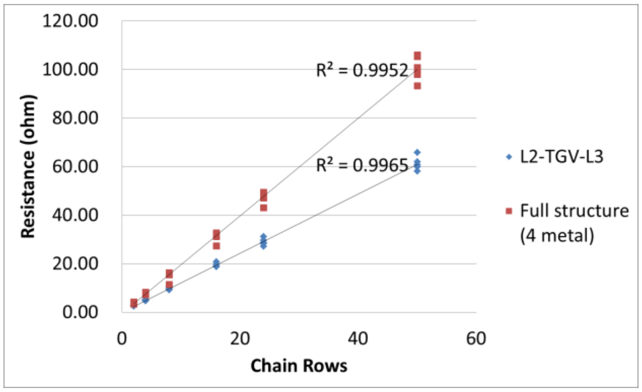


Figure 12: DC resistance measurement result

Based on electrical test results, both two types of build-up have good linearity observed by DC resistance measurement. One is L2 and L3 only (with TGV between) which is tested after L2/L3 formation with R square of 0.9965. The other one is four metal layers daisy chain substrate with R square of 0.9952, as shown in Figure 12.

III. Conclusion

A glass substrate daisy chain test vehicle was fabricated and characterized using a 508mm × 508mm panel size manufactured by IC substrate HVM line. Fine pitch of L/S=8/8μm on full glass panels was also developed and realized. The warpage of glass, ultra-thin glass, and organic panels were measured and compared. Daisy chain electrical measurement results of this glass substrate demonstrated good continuity and resistance. This study shows significant promise for continuing to explore and develop glass as a new substrate material. We urge and encourage more detailed studies to better understand and resolve yield and reliability issues.

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References

[1] Matt Nowak, "3-D Faces Cost Issues", http://scsong.wordpress.com/2009/10/14/qualcomms-nowak-3-d-faces-cost-issues-3/

[2] Matt Nowak, "2.5-D Interposers and 3D TSV DRAM Stacking-What's Next?", Global Interposer Technology Workshop, 2012

[3] Vijay Sukumaran, Qiao Chen, Fuhan Liu et al., "Through-package-via formation and metallization of glass interposers," in Proceedings of 61st Electronic Components and Technology Conference (ECTC), 2011, pp.557-pp.563.

[4] Aric Shorey, et al, "Advancements in Fabrication of Glass Interposers", Proc 64th ElectronicComponents and Technology Conf, 2014, pp. 20-25

[5] Chun-Hsien Chien, et al, "Process, Assembly and Electromigration Characteristics of Glass Interposer for 3D Integration", Proc 64th ElectronicComponents and Technology Conf, 2014, pp. 1891-1895

[6] Wei-Chung Lo, et al, " Development and Characterization of Low Cost Ultrathin 3D Interconnect ", Proc 55th ElectronicComponents and Technology Conf, 2005, pp.337-342