RF Device Integration on Glass Interposer toward 3D-IPAC Packages

Yoichiro Sato, Bruce Chou*, Vijay Sukumaran*, Junki Min*, Motoshi Ono, Choukri Karoui+, Franck Dosseul+, Christian Nopper+, Madhavan Swaminathan*, Venky Sundaram* and Rao Tummala*
+STMicroelectronics
*3D Systems Packaging Research Center, Georgia Institute of Technology
Asahi Glass Company
4375 NW 235th Avenue
Hillsboro, Oregon 97124, U.S.A.
Ph: 503-844-9689; Fax: 503-844-7207
Email: YSato@agcem.com

Abstract

3D Integrated Passive and Actives Component (IPAC) is a new concept of ultra-miniaturized and highly functional sub-systems, which enables one to achieve higher RF functionality in a single module. As the first step, this paper demonstrates the concept of integrating passive components using 100µm ultra-thin glass and small Through Package Vias (TPVs) by ArF excimer laser. Passive low pass filters (LPF) for WLAN in thin dielectrics on glass were designed using circuit simulator and EM solver. The LPFs were fabricated using low-cost panel based processes, and then assembled onto the Printed Wiring Board (PWB). The filters on either side of the glass interposer were measured at the board level, and the results corroborated well with EM simulations. The measurement results showed low insertion loss (about -1dB) and high rejection (<-20dB). The integration of passive components using double-side and ultra-thin glass interposers with small TPVs, enables one to shrink RF module size.

Key words

Glass interposer, RF component integration, through package via, low pass filters

I. Introduction

Majority of passive integration for RF modules still relies on surface-mounted discrete and bulky components to achieve the required performance. Integrated Passive Devices (IPDs) based on thin-film technology have emerged for size reduction of RF modules. However, current IPDs on silicon have difficulty in achieving high quality factor, due to the lossy material properties of silicon, and also the high cost associated with materials and processing of thin-film technology is one of the biggest barriers for the wide-spread use of silicon IPDs. On the other hand, IPDs on glass have been developed and produced by ST Microelectronics [1], since glass offers excellent electrical properties which enable us to design passive components with higher quality factor. However, because these glass IPDs use thick glass substrates and are based on single-side processing of components, there are limitations to size reduction. Moreover the added cost of thin-film processes is comparable to IPDs on silicon.

To address the above challenges, Georgia Tech Packaging Research Center (GT-PRC) has explored a new concept of ultra-miniaturized and highly functional sub-systems, called 3D IPAC [2]. As shown in Fig. 1, the concept involves the use of ultra-thin glass interposers with small TPVs to interconnect either passives or a combination of active and passive components on both sides. 3D IPAC can be assembled onto interposers, packages or printed wiring board (PWB), and provide a complete functional module for not only RF applications, but also for power or digital sub-systems. Moreover, 3D IPAC can be fabricated using low-cost panel-based process which has been explored by GT-PRC's industry program [3][4].

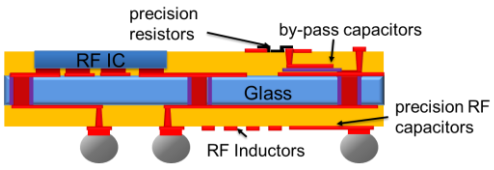

Fig. 1: 3D IPAC RF module concept [2].

The purpose of this study is to demonstrate ultra-miniaturized glass based 3D IPAC RF module as discussed above. As an initial demonstrator, we have fabricated a surface mountable RF module which includes RF low-pass filters on both sides

of 100µm ultra-thin glass using the low-cost and double-side process. This paper presents design, fabrication and characterization of the initial 3D IPAC RF demonstrator.

II. Key Technologies for Miniaturization

A. Ultra-thin glass

Asahi Glass Company (AGC) has developed manufacturing techniques to produce ultra-thin glass using the float process. Fig. 2 shows 100µm thin glass, rolled into a coil. Such ultra-thin glass enables one to achieve small TPVs at higher through-put, and also minimizes electrical parasitic loss of TPVs.

Fig. 2: Ultra-thin glass rolled into a coil [5].

To be able to tailor the material properties like thermo-mechanical or electrical properties is one of the biggest advantages of glass over silicon. EN-A1, borosilicate glass has been developed by AGC, has a low CTE (CTE=3.8ppm/℃) matched to silicon die and has excellent electrical characteristics for RF applications. Table 1 shows the material properties of EN-A1 glass.

Table 1: Material properties of EN-A1 glass.

Glass type	Alkaline Earth Boro-Aluminosilicate
T_g	720 ℃
CTE	3.8×10^{-6}
Bulk resistive	4.0×10^{13} Ω·cm
Dielectric constant	5.3 at 2.4GHz
Dissipation factor	0.004 at 2.4GHz

B. TPV formation technique by ArF excimer laser ablation

To form small TPVs in glass with high throughput is one of the greatest challenges for use of glass as core material, and there are many methods that have been proposed and explored [6]. AGC has also been developing several TPV formation methods, including ArF based excimer laser ablation. The short pulse width and high absorption of glass at the excimer wavelength enables one to form small and precise TPVs with less thermal stress in glass. In addition, the formation of multiple TPVs over a large sample area is possible by using the mask projection technique. To illustrate high throughput excimer laser ablation on glass, Fig. 3(a) and (b) shows the simultaneous formation of TPV array (with 20µm diameter at 30µm via pitch) in 55µm thin EN-A1 glass, and the cross section image of TPVs in 55µm thickness glass respectively.

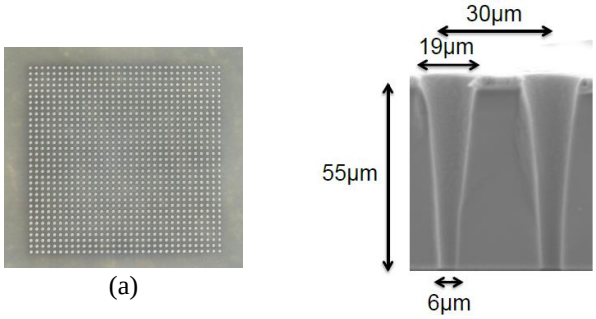

Fig. 3: (a) TPV array formation at 30µm pitch in 55µm thin glass, (b) cross-section image of TPVs [4].

C. Substrate stack-up and design rules

Design rules for the initial 3D IPAC RF demonstrator with four-metal-layers (1/2/1) was defined assuming the use of 100µm ultra-thin glass and small TPVs formed by ArF excimer laser discussed above. A schematic cross-section of the four layer stack-up with TPVs is shown in Fig. 4.

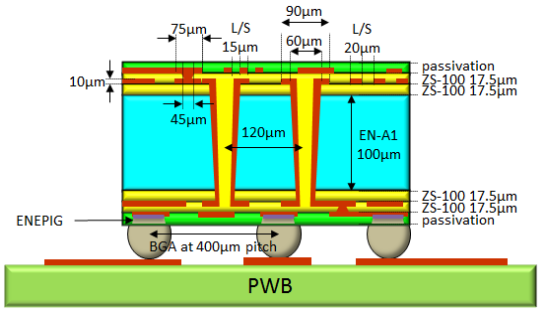

Fig. 4: Substrate stack-up and design rules.

III. Design of Low Pass Filters on Glass

A. High Density Inductor and Capacitor Designs

Inductor and capacitors (LC) are fundamental building blocks for RF filters. Using the four-metal-layer glass interposer design rule, various capacitor and inductor geometries were studied to optimize the capacitance and inductance densities and to minimize the parasitic effects. All of the geometries were laid out using SONNET and placed in the same ground ring to allow consistent de-embedding of parasitic [7].

Two types of inductors were considered: planar spiral inductors and core inductors. Core spiral inductors have the potential to exhibit high inductance in true 3D form; however, due to design rule constraints on TPV diameter and pitch, the achievable inductance density was observed to be

lower compared to spiral planar inductors. Both single layer and two layer spiral planar inductors were studied. A 3D schematic of the different inductor configurations is shown in Fig. 5. The inductance and series resistance of planar spiral inductor can be simply calculated using the expressions derived in [8]. The use of glass substrate effectively eliminates the parasitic RC associated with silicon substrate; therefore resulting in a design with higher quality factor.

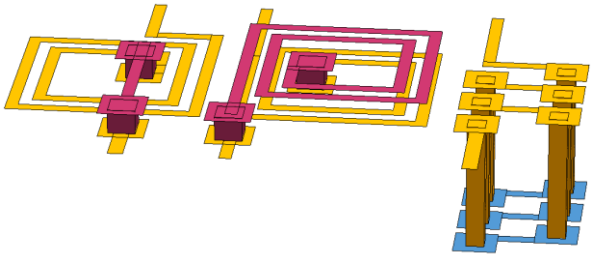

Fig. 5: 3D side-by-side comparison of spiral inductors and a core inductor.

Capacitors were all designed on the build-up layers to fully utilize the thin dielectric spacing between the metal layers. Three different configurations were considered: parallel plate, stitched, and inter-digitated, as shown in Fig. 6. The capacitance density was highest for parallel plate, as expected. Since the low-loss glass substrate is immune to substrate capacitance, parallel plate capacitors is both the simplest and the most suitable solution. Inductance and capacitance density of the different geometries considered are listed in Table 2.

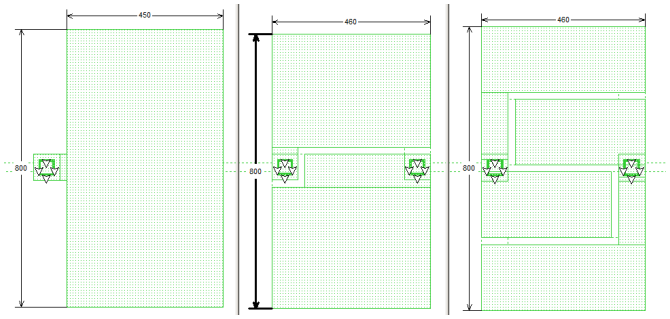

Fig. 6: 2D side-by-side comparison of planar capacitors.

Table 2: Inductance and capacitance density of passive building blocks.

Inductor	Density (nH/mm^2)		Capacitor	Density (pF/mm^2)
Core	16		Parallel plate	3.67
1 layer spiral	19		Stitched	3.48
2 layer spiral	66		Inter-digitated	3.59

B. RF Filter Modeling and Design

Four passive RF filters for WLAN of the same architecture have been modeled and designed to demonstrate the high density integration capabilities of 3D IPAC. The four filters differ only in cutoff frequency f_c, which are at 0.87, 1.8, 2.5, and 5.2 GHz. The design specifications, listed in Table 3, are the same for all filters. All of the filters follow the same design process shown in Fig. 7.

Table 3: Filter design requirements.

Parameter	Specifications
Insertion Loss (IL) @ f_c	As low as possible
Return Loss (RL) @ f_c	>15 dB
$2f_c$ Attenuation	> 30 dB
$3f_c$ Attenuation	15 dB > $2f_c$

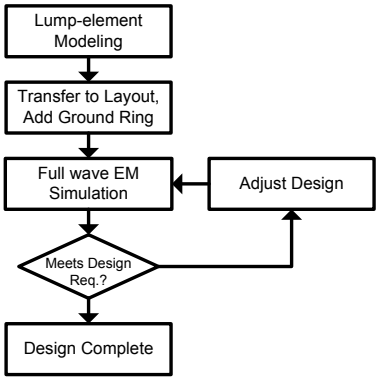

Fig. 7: RF Filter design flow.

This paper will describe the entire design process of the 2.5 GHz filter. Ideal lump-element schematic, constructed using Advance Design System (ADS) is shown in Fig. 8 [9].

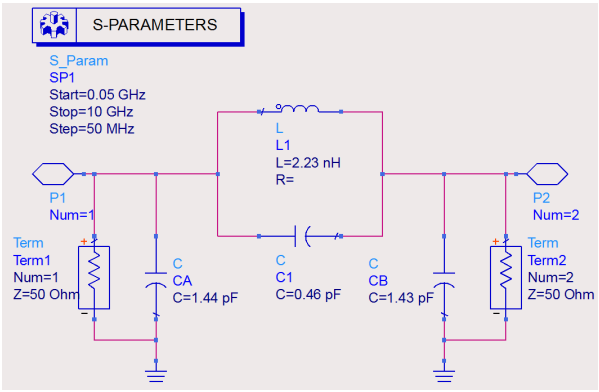

Fig. 8: Lump-element modeling of the 2.5 GHz filter.

After the lump element parameters have been defined, the corresponding capacitor and inductor areas can be estimated. Using the estimated values, the lump elements were translated to layout level and enclosed in a ground ring structure. SONNET was used as the full wave simulator, and the layout was adjusted iteratively to optimize the design requirements and to minimize the overall form factor of the filter device. The final 3D view of the layout is shown in Fig.

9. Noticeable differences in loss can be observed between the S-parameter plots of the lump-element model and the actual layout as shown in Fig. 10. These differences are due to the series resistance of the inductor and the slight variation in LC values. The series resistance adds to insertion loss and reduces return loss, while the slight LC variation changes the location of $2f_c$ resonance frequency.

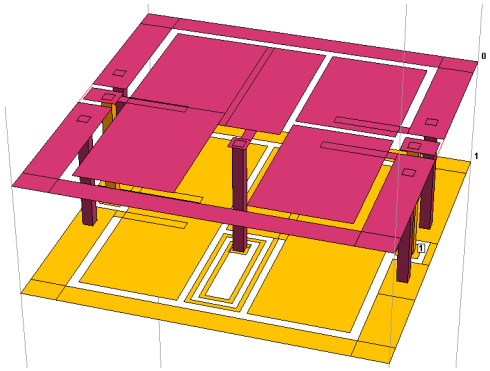

Fig. 9: 3D view of completed layout of the 2.5 GHz filter.

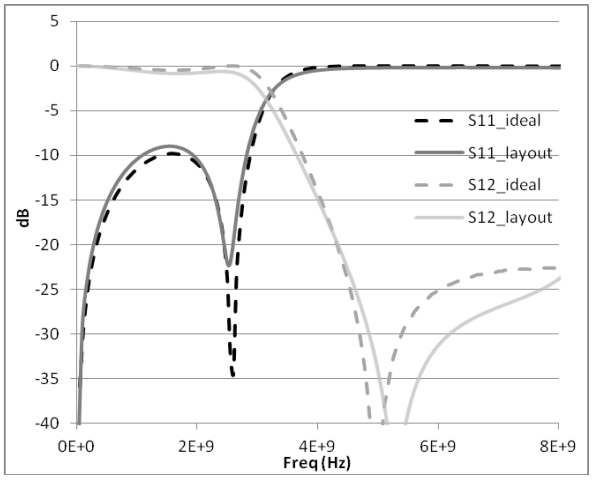

Fig. 10: Comparison between pre (ideal) and post layout design, for the 2.5 GHz filter.

The completed filter design parameters after iterative full wave simulation and area optimization are listed in Table 4. All of the design parameters were met except for the $3f_c$ attenuation of the 2.5GHz filter, which fell short by 5 dB. In addition, sub 1mm^2 filter designs are achievable for the 5.2 GHz filter.

Table 4: Optimized Design Parameters of the Filters.

f_c (GHz)	IL @ f_c	RL @ f_c	$2f_c$ Atten.	$3f_c$ Atten.	Area (mm^2)
0.85	0.5	25	>40	22	2.55
1.79	0.45	23	38	23	1.39
2.5	0.85	20	35	25	1.21
5.3	0.55	28	32	15	0.46

IV. Fabrication of RF Demonstrator

A panel based double-side process was used to fabricate the four-metal layer demonstrator. Fig. 11 depicts the fabrication process flow.

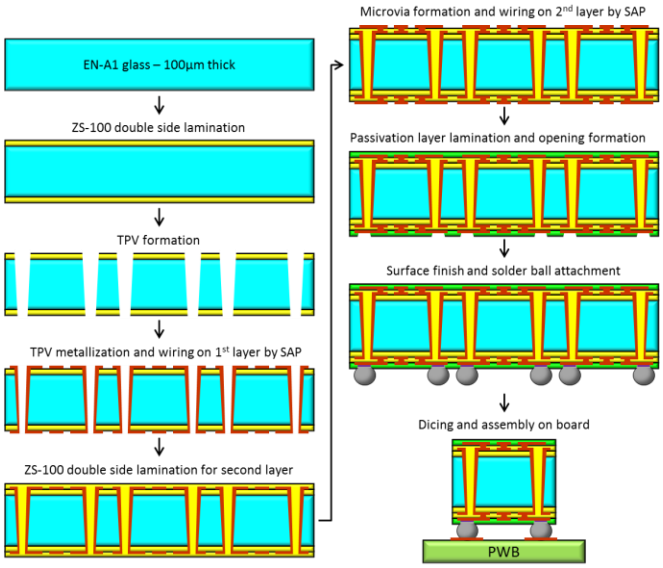

Fig. 11: Fabrication process flow.

In the first step, a 17.5µm thin polymer based insulation build up film, ZEONIF ZS-100 from Zeon Corporation, was laminated on both sides of a 100µm thin EN-A1 glass. Then, TPVs were fabricated using ArF excimer laser, with TPV entrance diameter of 60µm. Metallization of TPVs and surface wiring were carried out using Semi-Additive Process (SAP). For this demonstrator, conformal TPV plating was adopted in view of through-put of TPV plating and TPV reliability. To build up next dielectric layer, ZS-100 was laminated again on both sides of the substrates. At the same time, the conformal TPVs were filled with the polymer due to low viscosity of the polymer prior to thermosetting. Subsequently, micro-vias were formed using UV laser ablation, followed by SAP for metallization of the micro-vias and surface wiring on the outermost layers. Fig. 12 illustrates the double-side low-pass filters which were fabricated in the dielectric layers on the top side and bottom side respectively. The low-pass filter on the top side has TPVs to interconnect the bottom side.

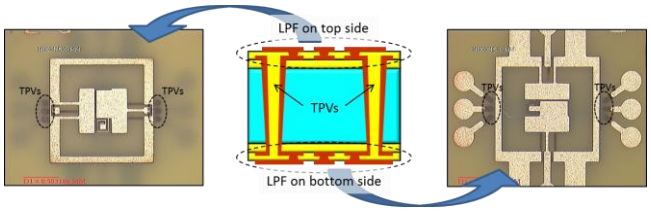

Fig. 12: Fabricated double-side low-pass filters.

After the four-metal layer substrate fabrication, passivation layer was laminated, and the openings in the passivation were formed to expose the BGA pads. After ENEPIG surface finish process, BGA balling was conducted, and finally assembly of the interposer onto PWB was carried out. Fig. 13 and Fig. 14 show the snapshot and cross-section image of the demonstrator after assembly onto PWB.

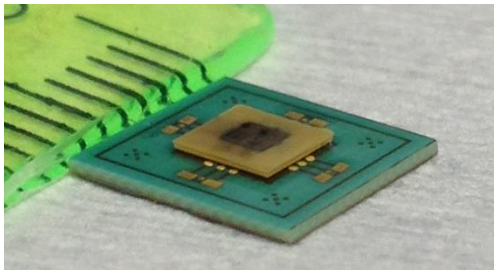

Fig. 13: Snapshot of the fabricated demonstrator.

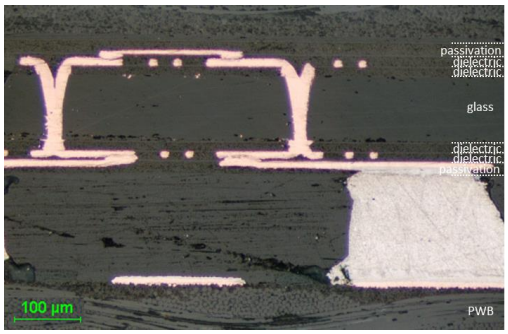

Fig. 14: cross-section image of the fabricated demonstrator.

V. Characterization of RF Demonstrator

The frequency responses of the fabricated RF filters were measured using an Agilent Network Analyzer. Consistent increase in frequency on all filters can be observed. To study the consistency, 30 filters on either sides of the interposer were characterized using the same setup, and their responses were averaged and reported below, in Table 5. As shown in the table, the cutoff frequency is consistently shifted by 8 ~ 15 % for all filters. The insertion loss increases with the introduction of TPVs and pads, which is expected. The return loss values are on average on par with the simulated values, but with a wider variation.

Table 5: Fabricated Filter Parameters Verses Simulation.

Sim f_c	0.85	1.79	2.5	5.3
Measured	0.98	2.03	2.82	5.72
Δf_c (%)	15.3	13.1	12.9	7.9
IL @ f_c	0.91	0.77	1.1	0.93
ΔIL (%)	82.5	70.9	29.1	69.5
RL @ f_c	17.4	35.8	21.4	32.3
ΔRL (%)	-30	55.7	7.07	15.5

To demonstrate the consistency of filter fabrication on either sides of the interposer, and to compare the effects of TPV, identical filters were placed on either sides of the interposer and characterized. The differences in cutoff frequency were less than 5%, while the design parameters were consistently above design requirements. Therefore, the presence of TPVs did not degrade the performance of the filters. Furthermore, filters can be constructed on the same area of the interposer to double the planar density. As an example, the measured s-parameter responses of the 0.87 GHz filter is shown in Fig. 15.

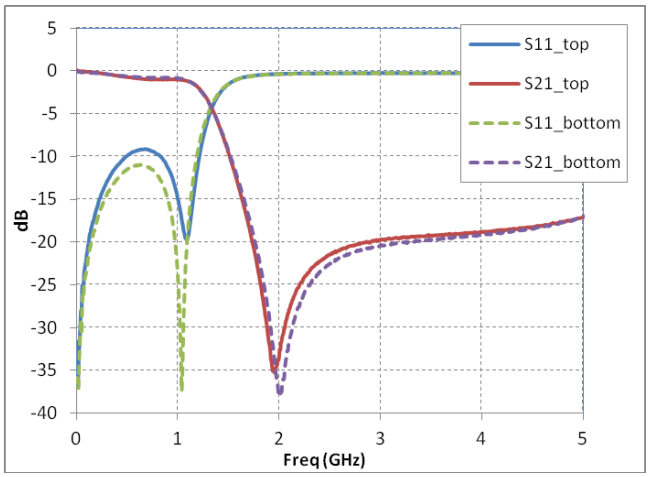

Fig. 15: Comparison between top and bottom filters, for the 0.87 GHz filter.

To comprehend the effects of assembly, the filters were measured before and after assembly onto PWB. The measured s-parameter responses for the pre-assembly and post-assembly 2.5 GHz filter have been plotted against the simulated responses in Fig. 16.

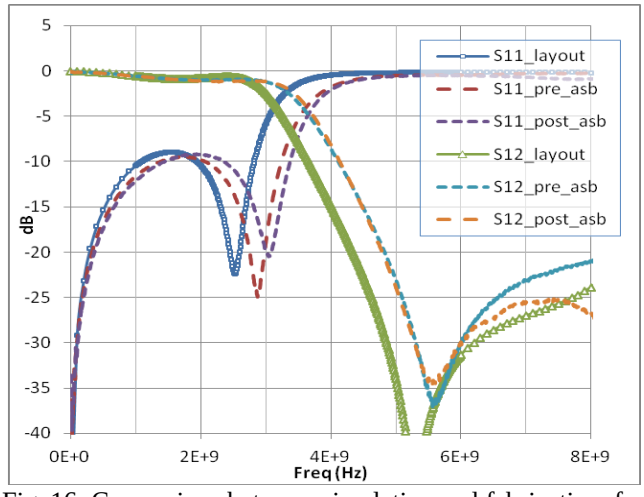

Fig. 16: Comparison between simulation and fabrication, for the 2.5 GHz filter.

A scalable increase in cutoff frequency is measured to be around 15%, as reported earlier. A 15 % shift in cutoff frequency for the fabricated samples is consistent with the 10 % thicker dielectric layer and 10% thinner copper traces due to over etching. The slight variation between the pre-assembled and assembled filters is due primarily to the series inductance and resistance of the solder joint. To comprehend the effects of the solder joints, a simple RLC model is adopted, as shown in Fig. [10]. The modeling result shows the series inductance to be around 0.2 nH, which is consistent with reported values. Similar measurement results were also observed on different filters and the same filter on different locations on the panel.

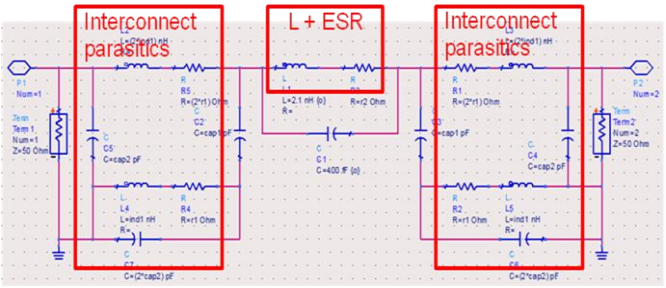

Fig. 17: Lump-element modeling of interconnect parasitics from solder joint.

VI. Conclusion

Toward ultra-miniaturization of RF modules, the concept of 3D IPAC was demonstrated using 100µm thin glass and small TPVs. The low pass filters for WLAN in thin dielectrics on glass were designed using circuit simulator and EM solver, and fabricated using low-cost panel based process, and finally assembled onto PWB. The measurement results showed low insertion loss (about -1dB) in the pass-band, with high rejection (<-20dB) in the stop-band. The measurement results further demonstrated the capability of double-sided filter placement, and showed negligible performance degradation between the top and the bottom side of the interposer. On the other hand, a 20% shift in cutoff frequency was observed, which are understood as variability in processing and parasitics from solder balls.

Acknowledgment

The authors would like to thank Hilal Ezzeddine from STMicroelectronics for providing valuable design guidelines. The authors would also like to acknowledge Tobias Materne, Steve Bigalke and Sven Johannsen from Technical University of Dresden, Germany, Toshitake Seki from NGK/NTK, Yuya Suzuki from Zeon Corporation, Makoto Kobayashi from NAMICS Corporation, Akira Mieno from Atotech Japan, and Vanessa Smet from GT-PRC for their fabrication support. This research is a part of the Low-cost Glass Interposers and Packages Consortium at GT-PRC.

References

[1] C. Calvez, et al., “New millimeter Wave Packaged Antenna Array on IPD technology,” SiRF 2010, pp. 96-99
[2] P. M. Raj, et al., “3D IPAC – A New Passives and Actives Concept for Ultra-miniaturized Electronic and Bioelectronic Functional Modules,” ECTC 2013 63rd, pp. 517-522.
[3] V. Sukumaran, et al., “Through-Package-Via Formation and Metallization of Glass Interposers,” ECTC 2010 60th, pp. 557-563.
[4] V. Sukumaran, et al., “Design, Fabrication and Characterization of Low-Cost Glass Interposers with Fine-Pitch Through-Package Vias,” ECTC 2011,61st, pp. 583-588
[5] S. Takahashi, et al., “Development of Through Glass Via (TGV) Formation Technology Using Electrical Discharging for 2.5/3D Integrated Packaging,” ECTC 2013,63rd, pp. 348-352
[6] M. Töpper, et al., “3-D Thin Film Interposer Based on TGV (Through Glass Vias): An Alternative to Si-Interposer,” ECTC 2010 60th, pp. 66-73
[7] "Sonnet Suites," Sonnet Software Inc., 2011.
[8] S. Mohan, M. Hershenson, S. Boyd, and T. Lee, “Simple Accurate Expressions for Planar Spiral Inductors,” *IEEE J. Solid-State Circuits*, vol. 34, Oct. 1999, pp. 1419–1424.
[9] "Advanced Design System (ADS) ", Agilent Technologies, 2012.
[10] J. Laskar, et al, “Review of RF Packaging Research at Georgia Tech’s PRC,” International Symposium on Advanced Packaging Materials, 1998, pp. 139-150.