

ULTRA THIN CHIPS STACKING ON TSV SILICON INTERPOSER USING BACK-TO-FACE TECHNOLOGY

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Abstract

Chip-to-wafer stacking is a key enabling technology for 2.5D as well as for 3D with technological challenges driven by on one hand the increase of the die surface and the number of I/Os and on the other hand by the reduction of the vertical dimensions.

In our integration, the chips are reported on a silicon interposer containing copper via-middle TSVs. Two different approaches have been considered to realize chip-to-wafer stacking with respectively 35 and 20 μm ultra-thin dies. The first one is the conventional flip chip (or Face-to-Face, F2F) integration based on Cu/SAC μ -pillar connections while the second is a less classical Back-to-Face (B2F) way based on the realization of a high topology RDL after bonding the chips face up on the silicon interposer using a polymer. This last architecture becomes more and more attractive with the reduction of the chip thickness to ultra-thin dimension and can offer substantial advantages in terms of design flexibility and technology cost.

Chip bonding is one of the first tasks to address: several bonding materials have been tested either on die side using die attach film (DAF) or on bottom interposer side using wafer level spin coated polymers. Then a novel brick consisting of high topology encapsulation and metallization has been fully developed to connect the dies to the bottom wafer enabled by the development of a specific lithography process.

Thermo-mechanical FEM simulation and first reliability assessment have been carried out and support the good mechanical behavior of this integration.

Electrical tests have been also completed that allows comparing the performances of F2F and B2F interconnections in terms of resistances and yield at front side level but also at back side level after TSV exposure.

Back to Face integration can be very attractive in terms of process complexity and cost for ultra-thin chips with limited I/Os counts.

Keywords: 3D, Chip-to-wafer stacking, Back-to-Face, Copper TSV.

Introduction

As miniaturization of CMOS devices is becoming more and more difficult and costly, new fields for improving ICs performances are actively developed. One of the most promising ways is certainly the 3D integration of stacked chips [1-3]. Different solutions of vertical stacking have been proposed and demonstrated during the last period. Essentially, this can be done at the package level (Package on Package, PoP) or by integrating all the chips of a system in the same package (System in package, SiP) [4, 5]. This last approach offers the best solution in

terms of resulting form factor as well as reduction of the interconnection lengths at system level enabling larger signal bandwidth and lower power consumption.

The individual chips can be either assembled horizontally side by side [6] or vertically one on top of the other on an interposer substrate. In this integration scheme, wires will no longer be the best solution and new electrical connection means are preferred. Through Silicon Vias (TSV), μ bumps or copper pillars associated with Redistribution Layer (RDL) all together are likely to form a complete and

most efficient path for the signal to be transmitted between the dies at an unprecedented density of channels.

Reducing the vertical dimension of the dies is also a key feature in this quest not only because it will have a direct effect on the final form factor of the product but also because it has a strong impact on the TSV geometry. When the die thickness becomes really thin, typically much lower than 50 μm , other approaches than using flip chip and TSV can be envisioned with a benefit in the integration complexity [7]. In this work we have developed an interconnection scheme where ultra-thin dies are not flipped on the interposer but stacked on its back side and with a metallization passing over the die topology to connect the chip to the interposer (Back to Face). The different processes used in this approach are detailed henceforth and mechanical and electrical results are presented accordingly.

Design

In this section Face-to-Face (F2F) and Back-to-Face (B2F) design are presented and compared. Figure 1 illustrates the two different schemes used to report a thin die on an interposer. The first is the flip chip classical way where the die is stacked upside down and connected by means of microbumps or copper pillars that are most likely based on Cu/Sn intermetallic soldering technology [8]. It is a Fan-In like layout and the interconnection area depends essentially on the smaller die, practically the top one. Top and bottom chips need to be co-designed necessarily and for both ICs real estate areas are directly impacted by the μbumps placement. μbumps can be placed either only in the periphery of the die with one or few rows or in a full array depending on the pitch and on the number of IOs required for the function.

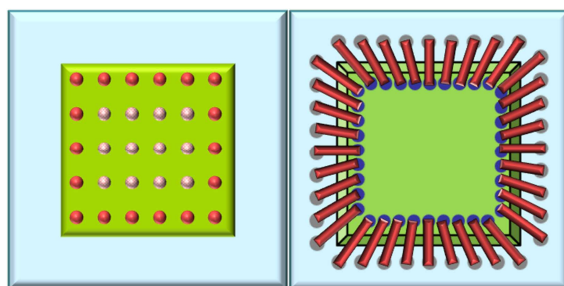


Figure 1: Face-to-Face (left) and Back-to-Face (right) die to wafer stacking.

The second scheme is the so called Back-to-Face stacking where the die is bonded active face up on the interposer. The interconnection between the top and

bottom chips is ensured by the formation of a redistribution layer on top of the stacked die. In this case it is a fan-out like layout where the limitation of the interconnection area is dictated by the bottom chip size, the pitch of the bottom die contacts can eventually be relaxed.

The top RDL adds a degree of freedom for the design and already existing functional chips can be directly integrated in this approach. With actual equivalent or finer pitch, same or even higher interconnection density than F2F stacking can be achieved assuming that only peripheral arrays is used which is the case for most of low and medium I/O count products.

Test vehicle

Electrical test vehicles have been designed with both B2F and F2F die to wafer stacking approaches as illustrated in Figure 2. Die thickness is respectively 20 μm and 35 μm and the pitch of the inter-chip connection is 200 μm . Electrical test can be performed on front side directly after stacking but also on the backside through TSV and RDL routing. Finally the chip can be mounted on board by solder balling and tested at this level including reliability.

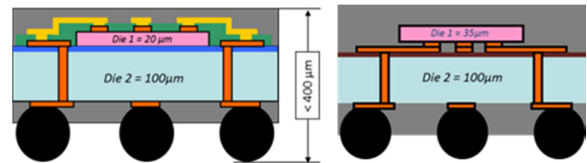


Figure 2: Face-to-Face (left) and Back-to-Face (right) die to wafer stacking.

This way a straight comparison can be made between the two approaches regarding mechanical and electrical performances. Only wafer level results will be presented in this work.

Technology

The overall process flow for the realization of the demonstrator is depicted in Figure 3. Top dies and bottom interposer are fabricated in a parallel way from bare silicon wafers with no active device. Then the same top dies are thinned, singulated and stacked either in F2F or in B2F configuration on the interposer having a differentiated design. For B2F stacking, two approaches have been also investigated, either by applying the bonding layer at the top die level using Die Attach Film (DAF) or at the bottom wafer level using spin coated polymers.

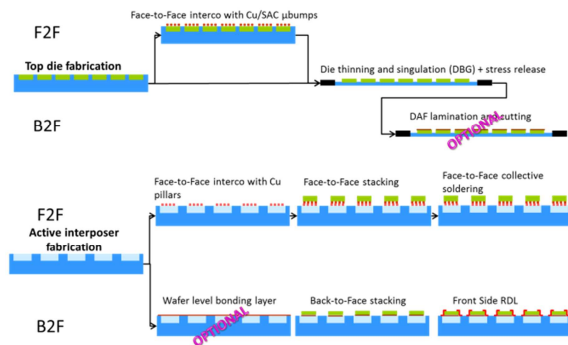
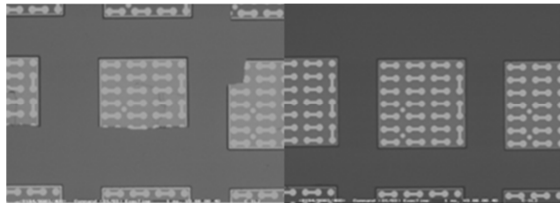


Figure 3: General process flow for chip-to-wafer stacking.

Results and discussions

A. Thin die preparation

Ultra-thin dies have been prepared using state of the art techniques provided by DISCO consisting of Dicing Before Grinding (DBG) [10]. For B2F, in order to facilitate the step coverage of both the dielectric encapsulation and the metallization, the dicing angle has been adapted to obtain beveled die edges. The slope of the edges has been set to 45°. After DBG a plasma stress release process is applied to the backside and to the edges of the singulated chips mounted on tape by SF6/O2 plasma using PVA Tepla technology [11]. This step has been proven to be mandatory particularly in case of ultra-thin dies as shown in Figure 4.

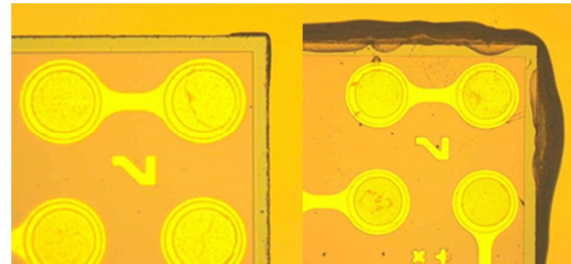


Left: without plasma; Right: with plasma
Figure 4: effect of plasma stress release on die fragility.

When plasma stress release is not applied 100% of the dies are broken during pick and place, inversely none are broken with this treatment.

B. Chip Bonding

DAF material has been first studied and characterized using Lintec LE product provided with 2 thicknesses, 10 and 7 μm . In principle, the thinner the DAF the better it will be for the final topology as well as for thermo-mechanical behavior perspective.



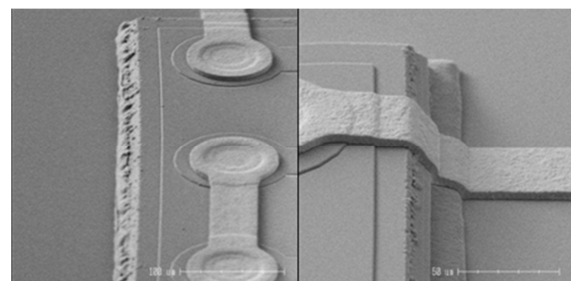
a) DAF 7 μm b) DAF 10 μm
Figure 5: chip bonded with DAF.

Figure 5 depicts the aspect of bonded die with respectively 7 and 10 μm of DAF. Fillet around the die is much more limited and uniform with DAF at 7 μm (20 μm max) than with DAF at 10 μm (80 μm max). Large fillet will be detrimental for the realization of the interconnections between the top and the bottom dies. In addition, the top die profile measured by profilometer is much flatter with 7 μm than with 10 μm (respectively 5 μm and 25 μm). However bonding strength needs also to be compared.

Shear test has been performed on a representative number of bonded dies with both DAF thicknesses. For DAF 10 μm we found that the edge of the silicon chip was broken under the nail while the rest of the die stayed bonded to the base substrate. For the DAF 7 μm the breaking mechanism is different since a part of the die is pulled off from the base substrate at about 4 KgF. These shear test results were confirmed by pull tests with respectively 3 N and 1.5 N for pulling out the chips from the base substrate. The adhesion strength of the DAF 10 μm is then higher than the one of the DAF 7 μm , although this last remains acceptable.

Taking into account all these factors, DAF @7 μm has been considered to be the best compromise and was selected for the integration.

Another important feature is to have a clear-cut delineation of the DAF along the die edge. For that, different cutting techniques like laser or expansion cut have been tried (Figure 6).



Left: Laser cut Right: DDS cut
Figure 6: DAF cutting techniques.

Laser cut technique leads to shallow DAF edges but at the same time to a lot of residues from the laser ablation around the die edges which can eventually rise over the top of the die. A proprietary cleaning technique from DISCO using protective water soluble material called HogoMax allows suppressing these residues when using laser cutting method.

Conversely, expansion cut leads to large fillet (30 μm) but with very clean cutting edges.

Pick and place parameters were also optimized varying the force and time for bonding each individual die with minimum DAF squeezing effect in particular with beveled slope where DAF can flow up more easily along the side of the die.

Another issue encountered for the die placement is that the presence of the DAF around the die edges is detrimental for the accuracy of positioning due to edge recognition issue. As well, cumulative clogging effect of the P&P head due to DAF overflow has been observed which degrade in turn the placement accuracy.

In summary, DAF bonding has been proven to be an acceptable solution for B2F stacking with a good bonding strength and P&P yield, however some limitations have been encountered on several aspects:

- Residual DAF outside the die before pick and place related to DAF cutting technique limitations.
- Presence of DAF residues on the die bevel due to squeezing effect during P&P.
- Placement accuracy degraded due to the presence of the DAF underneath the dies together with tool clogging by DAF.

For these reasons as well as for simplification of the bonding process, an alternative solution has been pursued consisting in the replacement of the DAF by a wafer level permanent bonding polymer coated on the bottom wafer before die placement.

Two different options can be proposed using this approach, the first consists in keeping the bonding layer on the full sheet bottom wafer and opening the bottom contacts through it; in this case it can be used as a bottom wafer passivation layer; the second is to pattern the layer outside the top die location either before or after bonding leaving the bottom wafer uncovered.

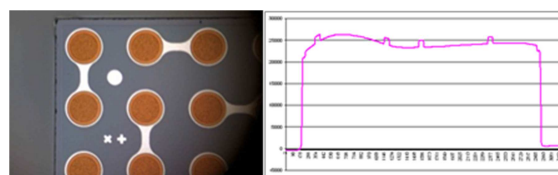
Then, to obtain the appropriate characteristics for D2W bonding, two main criteria need to be considered:

- Good tackiness during die placement at a relatively low temperature in order to maintain the dies in place without curing the polymer during the whole P&P sequence.

- Good adhesion and shear strength after curing of the polymer to allow subsequent process steps to be done with no delamination or displacement of the dies.

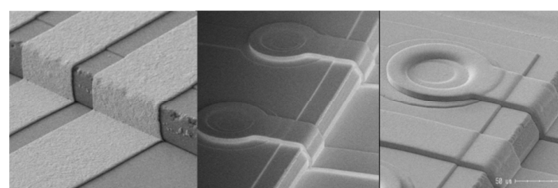
The principle is to place the dies in a range of temperatures where the material has a low viscosity but low enough to prevent polymerization from beginning. This process window as well as the intrinsic tackiness of the material is the key features for this application.

Three materials have been selected for this purpose: BCB (Dow Chemical), AL-X (Asahi Glass) and PI (HD microsystem). In the case of BCB, the best set point for bonding was obtained at a temperature of 160°C in very good agreement with the viscosity behavior with temperature of this material, the die placement force and the delay being not critical. A complete curing of the BCB is then achieved at the standard set up of 250°C, 1H under nitrogen. The shear strength is measured in the range of 1-2 KgF/mm² after placement and 4-5 KgF/mm² after BCB curing. These last values are well higher in comparison with DAF data (around 2 KgF/mm²). An illustration of a bonded die with BCB is shown in Figure 7.



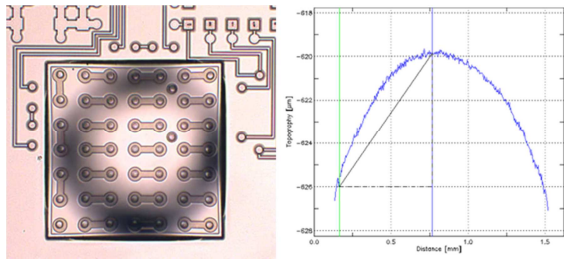
Left: top view Right: top die profile
Figure 7: chip bonded on full sheet BCB layer.

Using wafer level bonding layers leads to very clean die edges and extremely low bead effect as shown by SEM pictures of Figure 8.



Left: BCB center: AL-X right: PI
Figure 8: Wafer level bonding SEM pictures.

In case of PI bonding, higher temperatures are required to be in the tackiness regime. Optimum set point was found at 275°C. After final curing at 350°C shear strength was equally high (over 4KgF/mm²) but die profiles were not evenly flat on the wafer exhibiting some concave shapes (Figure 9). It is assumed that PI outgases water during imidization [12] causing the deformation of the thin die membrane.



Left: optical top view Right: optical profile.
Figure 9: die bonded with PI.

In the case of ALX we tried to use the same method to find the best tackiness regime by targeting the low viscosity temperature window before reticulation corresponding to a range between 120°C and 160°C. Unfortunately tackiness remained very low whatever the temperature set point prohibiting the use of this material for D2W bonding application.

In summary, for wafer level bonding, BCB give the best results among the 3 tested polymers. Wafer level bonding solution offers noticeable advantages over DAF for placement accuracy since the die edge detection is not affected by the presence of the bonding material assuming that the bonding layer is transparent for wafer mark localization. Also no clogging effect of the P&P head is observed, ensuring consistent placements over large volume of die population.

Finally main performances for the different bonding materials are summarized in table 2.

Table 2: Performances of selected bonding materials

	Chip Level	Wafer Level (spin coated)		
Material	DAF	BCB	PI	AL-X
Accuracy [μm @ 3s]	13.5	5.95	5.95	5.95
Shear values after P&P [kgF/mm²]	> 2	>1.5	> 1.0	Not consistent
Shear values after curing [kgF/mm²]	>4	>4	>4	na

C. High topology encapsulation

After the dies have been stacked an insulation layer needs to be added on top of the populated interposer before metallization. Main complying properties for this layer are listed below:

- Good step coverage over top die topology.
- Wafer level capability (good across-wafer uniformity).
- Low stress/low CTE.

- Low temperature budget (compatible with DAF or other bonding material, typically <270°C).
- Patternability on 2 levels topography.
- Transparency for lithography alignment.
- Good adhesion on underneath layers (SiO2/Si) and good adhesion of subsequent metallization layer.

Like for die bonding several solutions have been investigated to achieve this step illustrated in Figure 10, Figure 11 and Figure 12 corresponding respectively to different techniques of deposition:

- Option 1: thin conformal encapsulation using CVD deposited dielectric layers like Low Temperature Oxide (LTO) or parylen.
- Option 2: pseudo conformal encapsulation using spin coated or spray coated films.
- Option 3: thick planar encapsulation using spin coated or laminated viscous polymers.

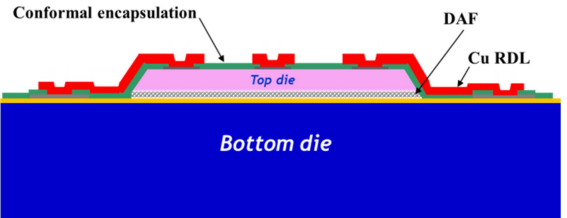


Figure 10: Thin conformal encapsulation.

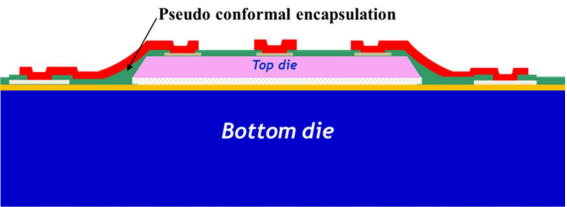


Figure 11: Pseudo conformal encapsulation.

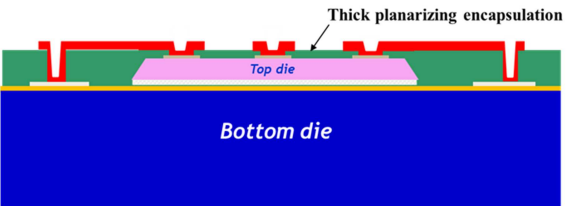


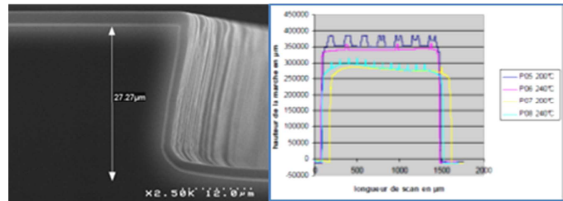
Figure 12: Thick planar encapsulation.

Each solution presents some advantages and some inconveniences that are discussed hereafter.

Option 1: thin conformal encapsulation with CVD oxide.

This option is interesting since CVD deposition technology is widely used in the fabrication lines and is already qualified in BEOL process flow including

contact openings and metallization. Low temperature oxides with good conformity behavior in the range of 150 to 250°C were evaluated. Figure 13 illustrates the behavior of this film on die topology showing very good conformity even with negative profile step. Additionally, LTO deposition at 200 °C or 240°C, either with BCB bonding (P05&P06) and DAF bonding (P07&P08) keep the die profile unaffected and flat.



Left: LTO step coverage Right: die profile with LTO
Figure 13: Encapsulation with conformal LTO.

Integrity of the encapsulation has been also carefully inspected and no crack or delamination of the film was observed.

Conversely to option 2 and 3, this integration requires the availability of an additional lithography step capable of defining the contacts on bottom and top levels. A specific development has been carried out regarding this lithography process also needed for defining the front side RDL which is described later (§ D).

Option 2: pseudo-conformal encapsulation

This option has been evaluated using EVG® 150 spray coater system and positive UV patternable polymer WPR 5100 from JSR.

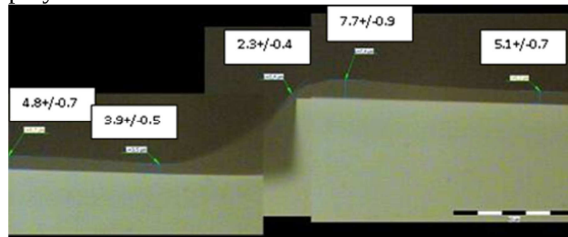


Figure 14 shows a cross section of a die step covered by this encapsulation with thicknesses varying between 8 μm to 2 μm from the center to the corner of the die. Contact openings were achieved with mask aligner lithography direct exposure through hard mask with acceptable resolution. Appropriate curing process of this material is critical to achieve a good adhesion of the above metallization.

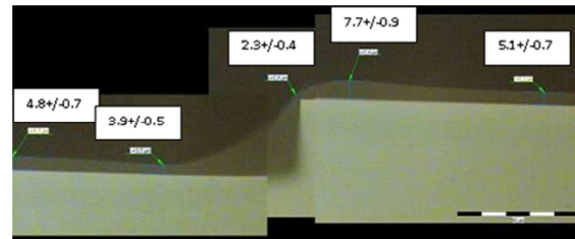


Figure 14: spray coated WPR on 30 μm step.

For option 2, ALX2010 polymer from Asahi Glass has also been evaluated using spin coating technique. A specific coating process has been set up to achieve a good coverage of the high topology surface with in particular a very low RPM speed. Figure 15 shows the result obtained on a wafer with a 25 μm step topology.

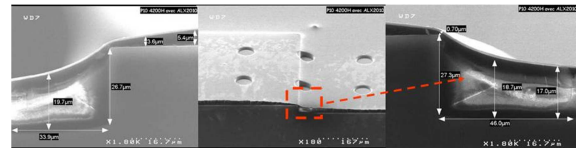


Figure 15: ALX2010 step coverage on high topology step.

A full coverage is obtained, however the minimum thickness at the upper corner of the die is only 0.7 μm with a nominal thickness of 12 μm on flat surface. Yet, the use of 45° beveled dies is likely to improve significantly the coverage making this solution pertinent. Regarding the patterning capability it was well in the CD specifications.

Option 3: thick planar encapsulation.

In this approach a thick planar polymer is coated on the wafer after die stacking. This polymer is preferably UV patternable to form directly the contacts on bottom and top die levels. Smooth positive slope profile for the high AR contact on the bottom dies (1:1) are preferable to allow the metallization to get over. Unfortunately most of the thick patternable polymers are currently negative tone with straight or even negative profiles as shown in Figure 16 (case for SiNR product from Shin Etsu). However optimized curing conditions may help to smooth the profiles.

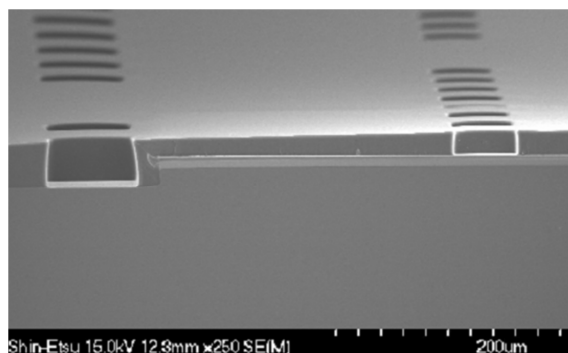


Figure 16: thick planar encapsulation with polymer.

In summary, different ways for thin die encapsulation have been investigated successfully. Option 1 with LTO thin deposition and option 2 with WPR spray coating were finally selected for the test vehicle integration. Option 3 was not kept for the integration since robust metallization process appeared to be more difficult to achieve on top of this layer.

In order to confirm these options for the integration, thermo-mechanical modeling and reliability assessment study will be discussed later in this paper.

D. High topology lithography

This lithography will be used either to open contacts in the passivation (in case of non UV patternable encapsulation layer like LTO) or for the realization of the top RDL. The aim is to use a thick resist that will be conformal enough and that will allow defining the desired patterns across the steps in one exposure shot. A specific development has been necessary to achieve this task using a thick negative tone product THB151N from JSR. The thickness of the resist needed to be adapted to the topology height to ensure a sufficient coverage but not too thick for maximizing CD resolution. The thickness has been set up to 30 μm nominally (on blanket substrate) and the soft bake has been adapted to help reflowing the resist over the topology. The coverage of the resist on the top corner is then at 15 μm and the maximum thickness at about 40 μm just after the step as shown in Figure 17. The minimum achievable CD is around 20 μm with little barrel-shaped profiles of the contacts and with acceptable bias between top level and bottom level contacts (<3 μm at the bottom of the contacts).

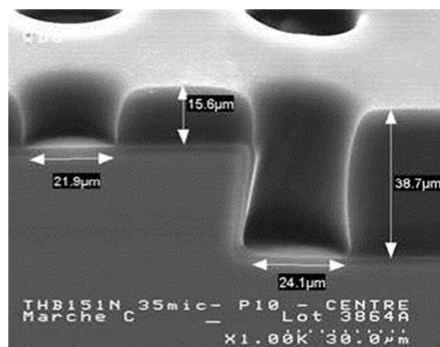


Figure 17: Thick negative resist contact lithography on 30 μm step.

For RDL line patterning, the same recipe is used with good compatibility with electroplating deposition process.

E. High topology RDL

Metallization level to connect the top to the bottom dies is achieved above the encapsulation layer with corresponding topology. The worst case corresponding to the conformal option and straight die profile has been first considered to check the coverage and definition of the metal routing as illustrated in Figure 18 and Figure 19. Semi-additive process consisting in Ti/Cu seed layers, high topology lithography and Cu electroplating deposition is used. Process window for copper seed layer thickness was verified in the range of 100 to 400 nm.

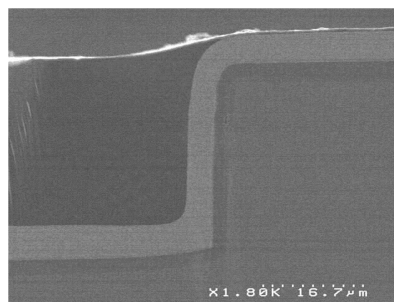
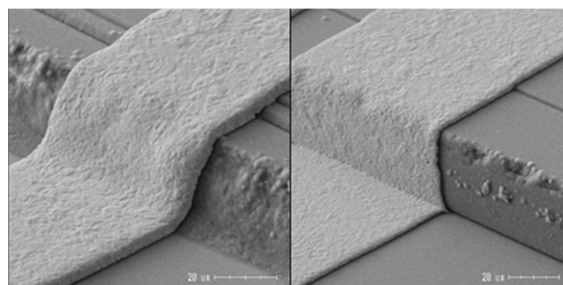
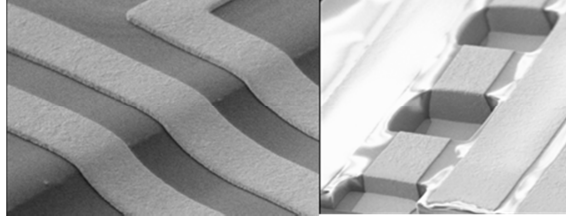


Figure 18: Copper RDL step coverage on silicon step.



a) Bevel die/DAF b) straight cut/full sheet BCB
Figure 19: RDL over die corner.

Also metal patterning has been performed over spray coated and thick planar encapsulations as illustrated in Figure 20.



Left: spray coated Right: planar
Figure 20: RDL over die topology with option 2 and 3 encapsulation stack.

In all configurations good step coverage and patterning definition down to 20 μm were obtained. Meanwhile, metal adhesion on polymer encapsulation necessitates careful surface preparation.

F. Final passivation

Thick polymer encapsulations either by spin coating or spray coating already developed for die encapsulation were used to cover the top RDL to complete the front side process flow. There is no need for patterning this layer since electrical connections are ultimately taken from the back side through the TSVs. Front side intermediate electrical tests are then carried out before coating this protective layer.

G. FEM simulation

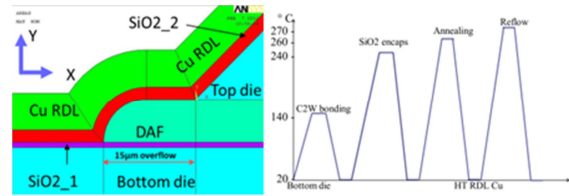
For the B2F stacking, bonding material may have a strong influence in integration integrity since the thickness of this film is quite comparable to the silicon die thickness. In particular, when using PECVD silicon dioxide layer for die encapsulation, thermo-mechanical mismatch between organic bonding material and thin glass layer may be detrimental and can lead to cracks and reliability issues for the high topology interconnects. In table 1 we have summarized the principal thermo-mechanical data of the films integrated in the structure.

Table 1: Main data of selected bonding polymers.

Materials	CTE (ppm)	Modulus (GPa @20 °C)	Tg/Stress free (°C)	Curing Temp. (°C)
Silicon	2.7	202	na	na
LTO	0,4	85	240	na
Copper	17	110	140	na
DAF	$\alpha 1$: 90 $\alpha 2$: 40	2.1	169	140
BCB	42	2.9	350	250
PI	50	2.6	325	350

Materials	CTE (ppm)	Modulus (GPa @20 °C)	Tg/Stress free (°C)	Curing Temp. (°C)
ALX2010	60	2.4	230	200

Thermo-mechanical simulation has been carried out on B2F stack assuming that all material behaviors are elastic in the considered range of temperatures. 2D model has been constructed using ANSYS software with adapted meshing to the structure topology (Figure 21), assuming that the DAF is forming a bead outside the die. Thermal history corresponding to the process integration is then loaded in the calculator to extract the stress in the x, y, z directions as well as Von Mises averaging component.



Left: FEM of B2F structure Right: thermal cycle
Figure 21: Thermo-mechanical simulation with DAF, LTO encapsulation and RDL.

Figure 22 illustrates the constraints after completion of the whole process cycle with the DAF bonding /LTO encapsulation case. Maximum stress is localized in the SiO₂ at the bottom corner on top of the DAF with values in the range of 600 MPa.

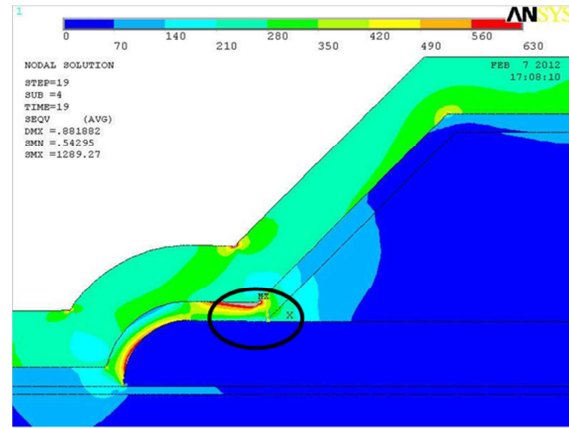
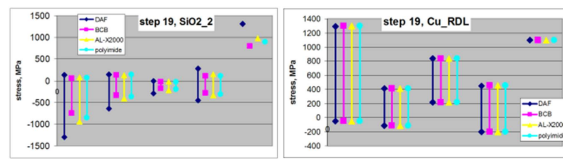


Figure 22: stress at ambient temperature after HT RDL fabrication.

Same studies were applied to other bonding materials and comparative results are given in Figure 23 corresponding to maximum stress values. Absolute data are not directly representative of the real case due to single point effect but comparative study is

valid. There are very little differences between the bonding materials.



Left: in SiO₂ encapsulation Right: in RDL
Figure 23: Maximum stress with different bonding materials.

H. Thermal cycling

First reliability assessment has been carried out on B2F integration with DAF bonding, SiO₂ conformal encapsulation, HT RDL and final thick passivation for passivation.

5 cycles at 200 °C, 225 °C, 250 °C and 275 °C with heat up ramp of 10 °C/min and neutral cool down were applied on a wafer. After each temperature cycle the wafers were inspected and die bow was measured. No significant variation was found and no crack or delamination was observable by microscope inspection. Electrical test was performed after all thermal cycles and passivation opening to access the test pads, very little increase of the resistance (about 1%) was found with no failure as shown in Figure 24.

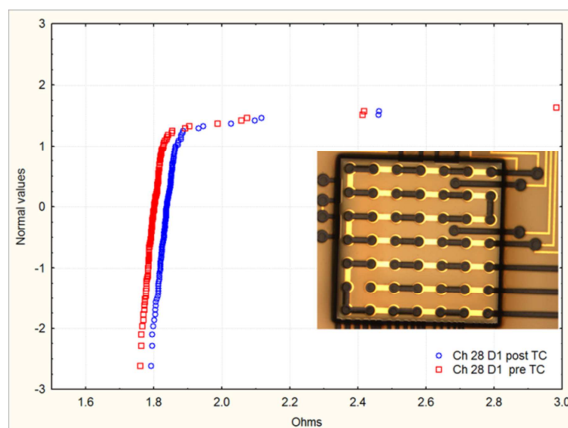


Figure 24: Resistance distribution of B2F daisy chain after thermal cycling.

These preliminary results are very encouraging for the integration of this brick; more reliability tests using JEDEC standards are going to be realized to consolidate these first data.

I. Electrical results

Resistances of daisy chains are measured on front side after high topology metallization and on backside through TSV and back side RDL on 147 sites with 4

points automatic probing on daisy chains of 14 links of HT metal and top die metal. 4 full wafers were first tested in the B2F chip stacking configuration using DAF/SiO₂ encapsulation/HT RDL/ALX passivation as reported in Figure 25. Resistance measurements are in perfect agreement with expected values with negligible contact resistances between chip metallization and HT RDL.

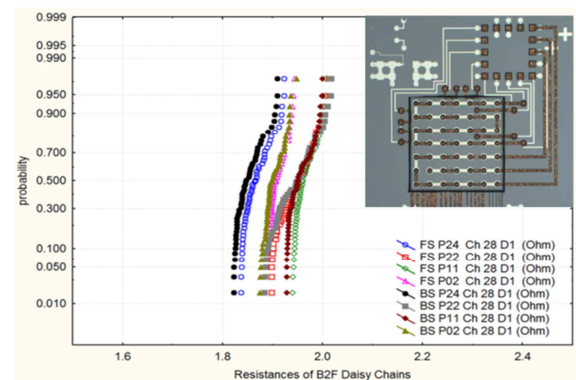


Figure 25: Normal plot resistances of 4 full populated wafers with B2F stacked die measured on front side (FS) and back side (BS).

These results are neither impacted by the thinning of the interposer nor by the back side process and wafer yield loss was about 5% from 98% at front side level to 93% at back side level.

Finally, in our design, B2F stacking daisy chain resistances give lower values than F2F equivalent structures due to the beneficial contribution of the thick copper top RDL lines.

Conclusions

Ultra-thin die stacking on silicon wafer interposer using back to face architecture was presented. This way of stacking very low profile chips presents some compelling advantages both in terms of design and process over conventional flip chip method. First we have demonstrated that chips as thin as 20 µm can be prepared using Dicing Before Grinding and plasma stress relief process with good control and good mechanical yield. For die-to-wafer bonding, Die Attach Film as well as wafer level polymer bonding has been successfully assessed supporting some substantial advantages for the latter solution.

Die encapsulation and interconnection issues have been analyzed and several solutions were evaluated with a focus made on a thin conformal dielectric layer followed by a high topology RDL.

This scheme exhibits high mechanical and electrical yield and good electrical performances. First reliability assessments are also conclusive and will be further complemented with JEDEC protocol

tests. Also functional products are being completed using this route.

References

- [1] J. U. Knickerbocker, et al., "3D silicon integration," in Electronic Components and Technology Conference, 2008. ECTC 2008. 58th, 2008, pp. 538-543.
- [2] S. Pozder, et al., "Progress of 3D integration technologies and 3D interconnects," in IEEE 2007 International Interconnect Technology Conference, IITC, Burlingame, CA, 2007, pp. 213-215.
- [3] K. Takahashi, et al., "Process integration of 3D chip stack with vertical interconnection," in 2004 Proceedings - 54th Electronic Components and Technology Conference, Las Vegas, NV, 2004, pp. 601-609.
- [4] Kuroda T., Miura N., Perspective of low-power and high-speed wireless inter-chip communications for SiP integration, 2007, ESSDERC 2006 - Proceedings of the 36th European Solid-State Device Research Conference, P3-6.
- [5] Glass & Silicon Interposers Market Report – September 2010, <http://www.i-micronews.com/reports>.
- [6] Patrick Dorsey, "Xilinx Stacked Silicon Interconnect, Technology Delivers Breakthrough FPGA Capacity, Bandwidth, and Power Efficiency", White Paper, www.xilinx.com
- [7] Michael Töpper, Tobias Baumgartner, Matthias Klein, Thomas Fritzsche, Julia Roeder, Mario Lutz, Maria von Suchodoletz, Hermann Oppermann, Herbert Reichl, "Low Cost Wafer-Level 3-D Integration without TSV", Proceedings of Electronic Components and Technology Conference, 2009, pp 339-344.
- [9] Wei Koh; Lin, B.; Tai, J.; , "Copper pillar bump technology progress overview," Electronic Packaging Technology and High Density Packaging (ICEPT-HDP), 2011 12th International Conference on , vol., no., pp.1-5, 8-11 Aug. 2011.
- [10] <http://www.disco.co.jp/eg/solution/library/dbg.html>
- [11] J. Burkhart, "Ultra Thin Chip Technology and Applications", Springer 2011, Chapter 3, page 28
- [12] Nicklaus F, Enoksson P, Kälvesten E and Stemme G 2001 Low-temperature full wafer adhesive bonding J. Micromech. Microeng. 11 100-7.