A Novel Back-side Via Process For Low-cost TSV.

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Abstract
Recently, mobile devices, such as smart phone or tablet PC have spread widely, and data traffic is increasing rapidly. Data servers for them are required high-speed data processing and low power consumption. Devices for those equipments are required high-speed processing, high-density packaging and low power consumption. Most powerful way to achieve these goals are three-dimensional (3D) integration using TSV (Through Silicon Via) and 2.5D integration using silicon interposer. However, cost and reliability issues are pointed out. The radical problem about the long-term reliability of TSV production is not still solved. In particular, the management of barrier metal film deposition on the smooth surface is most important technology for Cu diffuse protection [1]. To solve these problems, we have been developing via last process. One of the major challenges to via last back-side via is high capacitor. For this problem, scallop-free high rate Si etching and low dielectric constant liner is effective. We have been developing scallop-free etching by direct etching method. [2,3,4] Direct etching method use mixture gas of SF6 and O2, forming a thin SiOx film on the sidewall, and achieves an anisotropic etching. Advantage of direct etching is smooth sidewall without scallop. Simultaneous etching and side wall protection do not generate periodic unevenness. The issue of the leakage current, which could be caused by sidewall roughness, has been studied. [5, 6] Moreover, since a thick fluorocarbon film does not adhered, reduce the load of cleaning step and the risk of peeling the insulating film. Direct etching method is superior to the taper angle controllability. Taper and scallop-free etch improve the deposition coverage and contribute cost reduction. On the other hand, Bosch etching also has some advantage. We have developed etching module which is capable of both direct etching and Bosch etching. As a result, we have developed new process which is combined direct etching and Bosch etching. It has a new value and potential.

Key words
Via-last, low-cost TSV, Scallop-free

I. Introduction
Currently, via middle process is major attempt for 3D integration. However, cost and reliability issues are pointed out. At via middle process, TSV are formed between CMOS process and BEOL. Therefore, particle and contamination must be strictly managed. Equipments for FEOL are used, and then cost is high. Table 1.(a) shows standard via middle process. At the case of via middle process, CMP processes are required several times and they are high cost. On the other hand, at via last process, TSV are formed after BEOL. Particle and contamination are not so strict. Low cost equipments for assembly and testing process can be use. Table 1.(b) shows standard via last back-side via process. Process cost is lower than that of via middle. One of the major challenges to via last back-side via is high capacitor. For this problem, scallop-free high rate Si etching and low dielectric constant liner is effective. We have been developing “scallop-free” etching method by direct etching method. Direct etching method use mixture gas of SF6 and O2, forming a thin SiOx film on the sidewall, and achieves an anisotropic etching. Advantage of direct etching is smooth sidewall without scallop. Simultaneous etching and side wall protection do not generate periodic unevenness. Moreover, since a thick fluorocarbon film does not adhered, reduce the load of washing step and the risk of peeling the insulating film. Direct etching method is superior to the taper angle controllability. Taper and scallop-free etch improve the deposition coverage and contribute cost reduction. On the other hand, Bosch etching also has some advantage. We have developed etching module which is capable of both

direct etching and Bosch etching. As a result, we have developed new process which is combined direct etching and Bosch etching. It has a new value and potential.

Table 1. Comparison of via middle and backside via TSV process.

(a)	(b)
< Via Middle > 1. TSV Etch 2. Oxide Liner CVD/ ALD 3. Barrier/Seed PVD/CVD/ALD 4. Cu Plating 5. Annealing 6. Cu CMP 7. Edge Trim 8. Temporary Bond Via Reveal Process 9. Grind & CMP Si 10. Recess Etch (Dry, Wet) 11. CVD Nitride/Oxide 12. Oxide CMP	< Back-side via > 1. Edge Trim 2. Temporary Bond 3. Grind & CMP Si 4. Lithography 5. TSV Etch 6. Oxide Liner CVD 7. Oxide Contact Etch 8. Barrier/Seed PVD 9. Cu Plating 10. RDL

Table 2. Comparison of conventional method and countermeasure technology.

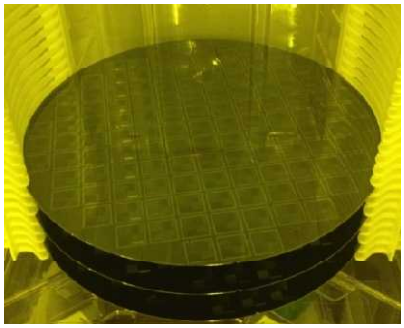
(a)	(b)
< Conventional > 1. Edge Trim 2. Temporary Bond 3. Grind & CMP Si 4. Lithography 5. TSV Etch: Bosch Etch 6. Oxide Liner CVD 7. Oxide Contact Etch 8. Barrier/Seed PVD 9. Cu Plating 10. RDL	**< ULVAC >** 1. Edge Trim 2. Temporary Bond 3. Grind & CMP Si 4. Lithography: Large lens & High resolution. 5. TSV Etch: Non-Bosh*/Bosch 6. Polymer Liner VDP** (Photo-imageable dielectric) 7. Polymer Contact Etch 8. Barrier/Seed PVD 9. Cu Plating 10. RDL

*Non-Bosch Etching: ULVAC's Scallop-free Etching
**VDP: Vapor Deposition Polymerization

II. Results and Discussion

Low-cost Lithography

High throughput in the lithography is also one of the important technologies. Compared with conventional litho process, higher throughput and low COO are expected. Large area and high resolution exposure technique is extremely effective technical means. An example of 300mm wafer after lithography process using this technology (USHIO Inc. UX-74101SC) is shown in Figure 1. Via diameter of under 3-10um were exactly exposed.



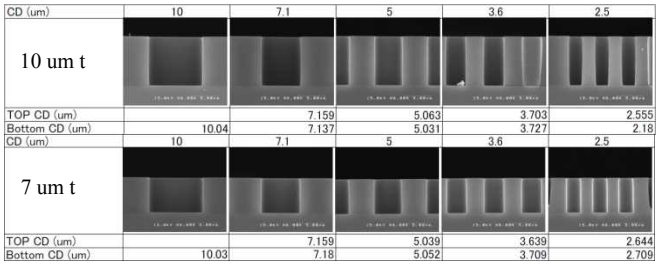


Figure 1. Low cost lithography

"Scallop-free" Etching

Bosch etching is popular among Si deep etching, but scallops are generated by repetition of etching and deposition. ULVAC's scallop-free etching (Non-Bosch etching) is non-cyclic process and scallops are not generated in principle. (Figure 2.)

Scallop-free etching uses mixture gas of SF6 and O2. Silicon etching by fluorine radical is originally isotropic. Anisotropic etching is realized because the sidewall is passivated by oxygen. Figure 2. is the comparison of Bosch etching and Scallop-free etching.

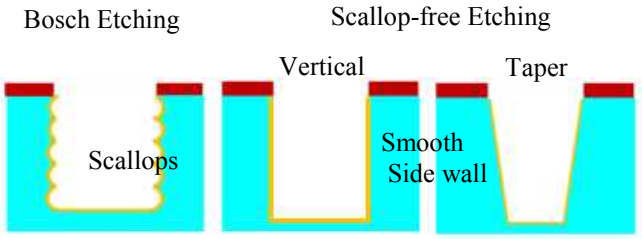


Figure 2. Comparison of Bosch etching and scallop-free etching.

"Scallop-free" etching process has developed for TSV fabrication. And, the smooth-sidewall had proved shorten PVD process time. A novel ICP plasma for Si etching is high electron density (10^{12} / cm^3), and very uniform on the Si wafer. This plasma characteristic of ICP source above 5Pa process operated with dual rf antenna coils for TSV and bottom-SiO2 etching. Improved plasma characteristics such as higher plasma density and very uniform and high aspect ratio anisotropy TSV etching process were realized in 300mm wafer. Which plasma source is kind of planar type ICP. 13.56MHz or 2MHz of rf for dual antenna coils and low frequency rf bias can operate in independently. (Figure 3.) Mechanism of Si etching is mainly fluorine radical reaction. High fluorine radical density plasma is need to get high etch rate. On the other hand, management of radical diffusion from around rf antenna is important for very uniform process of high aspect ratio TSV as well. Center gas injection on the rf window is induced instead of side gas injection to avoid of the rf electric field effect. Therefore, when Si was etched using dual rf antenna coil with SF6 / O2 / additional gases mixture injection from center of rf window, the high etch rate and selectivity of Si over the photo-resist and very uniform process were observed. And, the Si wafers used in this work are 200/300 mm in diameter with TSV holes patterned. The diameter of TSV is 10 to 50 um with photo-resist / SSS or GSS substrate structure. When the pressure increased about 20 Pa, the Si etch-rate is increased. On the other hand, Taper-angle can get positive at high-pressure process in 300mm wafer (Figure 4.), and when another parameter changed, taper-angle going vertical or negative profile. These results demonstrate that taper angle is able to controllable by scallop-free etching process. And, which method found that it was better continuous growth of Cu-ECP than the vertical profile (Figure 5.). Figure 6. shows relationship of electro deposition time and etched shape. Electro deposition time of vertical shape is 25 min. On the other hand, tapered shape is 4 min. A reduction in the electro deposition time of 80% is obtained by changing from vertical to tapered shape. [7] This result suggests the possibility that can reduce a burden of Cu-ECP process in the future (lead to low-cost).

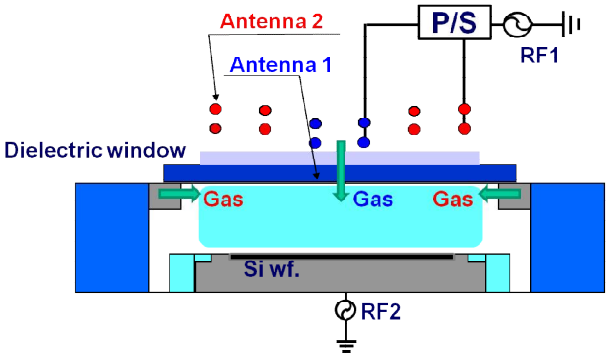


Figure 3. Schematic view of the TSV etcher apparatus.

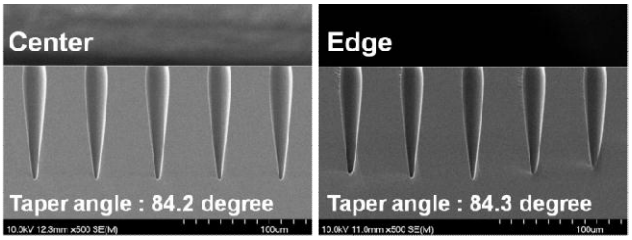


Figure 4. Tapered control with scallop-free etching in 300mm wafer.

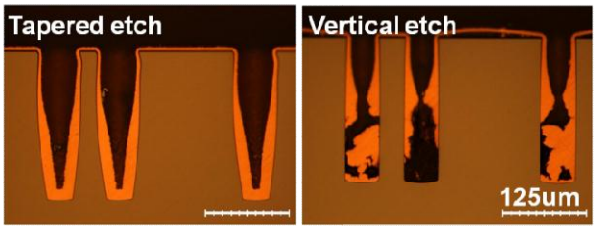


Figure 5. Etched profiles and Cu ECP.

Figure 6. Electro deposition time reduced by tapered shape [7]

Notch free process for back side via

We have mainly developed Non-Bosch (scallop-free) etching. But our new plasma source is also able to Bosch etching. (Figure 7.) We propose a new etching process combining Bosch etching and Non-Bosch etching. Figure 8 is an example. At first step, silicon was etched to 130 um by Non-Bosch process. Non-Bosch process uses mixture gas of SF6 and O2. In the next step, remaining 30 um was etched by Bosch process. Etching step uses SF6 based gas and deposition step uses C4F8 based gas. Etching was stopped at SiO2 layer and notching did not occurred at the interface of Si and SiO2. Etch rate of Non-Bosch etching is faster than that of Bosch etching, then process time of combination etching is shorter than that of all Bosch etching.

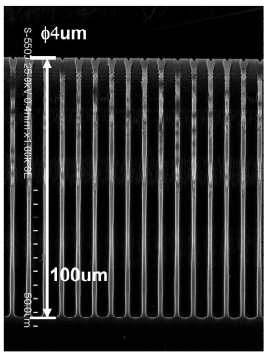


Figure 7. Bosch etching

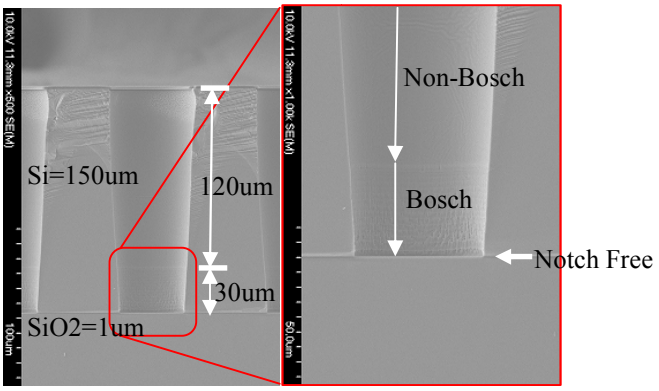
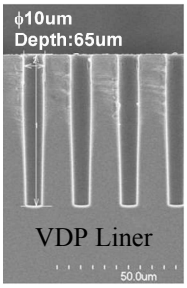


Figure 8. Notch free etching by combination etching

VDP (Vapor Deposition Polymerization)

We are trying to apply VDP as TSV liner. Step coverage of VDP is higher than that of conventional CVD TEOS. VDP has a great potential to realize the low-cost TSV.



	VDP		CVD TEOS	
Position	Thickness	Coverage	Thickness	Coverage
Top	873 nm	-	1906nm	-
Side (top)	754 nm	86 %	1290nm	68%
Side (middle)	555 nm	63 %	417nm	22%
Side (bottom)	437 nm	50 %	397nm	21%
Bottom	417 nm	48 %	417nm	22%

Table 3. Step coverage of VDP and PE-CVD.

III. Conclusion

1. A novel ICP plasma realize both Bosch etching and Non-Bosch etching by same system, which enables new low-cost TSV fabrication.
2. Scallop-free etch improve the deposition coverage and reduce the deposition cost.
3. Tapered shape improves the deposition coverage and enhances the electro deposition rate thereby reducing the TSV fabrication cost.
4. Because VDP is good step coverage, it has the potential as a new insulating material for TSV.

Acknowledgment

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