Control of 3D IC process steps by optical metrologies

G. Fresquet *Fogale Nanotech*, D. Le Cunff and *STMicroelectronics*, Th. Raymond and D. K. de Vries *Qualtera*

delphine.le-cunff@st.com,

g.fresquet@fogale.com,

dirk.de.vries@qualtera.com

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2015/1/000479/2256146/isom-2015-wp53.pdf by guest on 23 November 2022

Abstract

This paper evaluates various optical metrology techniques for in-line control of the uniformity of 3D stacked structures.

Advanced packaging technologies are rapidly evolving and 3D architectures require very well controlled process steps. Optical metrology techniques are now used for TSV but also for interconnect processing. In engineering mode, at the process implementation step, these techniques must be evaluated and then used to get uniform and repeatable processes.

Among the 3D TSV Via middle process flow, the temporary bonding, wafer thinning and TSV reveal are key 3D process steps to get a uniform backside copper nail signature. High aspect ratio TSV are etched in Front End of the line and deep reactive ion etching systems generates radial non uniformities signatures. The wafer backside processing challenge consists in compensating this issue among the entire wafer surface.

In this paper, all these process steps were characterized in order to quantify their specific intra-wafer dispersion signature .of the related key parameters. Cross correlation between the various intra-wafer process step signatures was then analyzed to verify the data set consistency and several process parameters analyzed to get a simple model. This model was then used to get a very uniform copper nail signature.

For small diameter TSV and corresponding copper nails, a comparison has been done between full field OCT and confocal chromatic techniques.

Key words

TSV, 3D IC, metrology, process control, copper pillars.

I. Introduction

The use of Through-silicon via (TSV) to conquer the third dimension enables to keep a very small form factor and opens up the way to stack far more than two dies.

Among the 3D process integration flow, key 3D process steps were identified and characterized in order to quantify their specific intra-wafer dispersion signature.

One of the key success factors for this technology is maintaining the wafer uniformity across the whole process flow. Several of the major 3D integration process steps are known to create strong non-uniformity across the wafer, namely:

- Through Silicon Via (TSV) etching
- Wafer/carrier bonding and thinning
- TSV reveal etching

Each of these 3D process steps generates a specific non-uniformity signature, and these add up to a cumulative dispersion on the final wafer.

The development of non-destructive optical metrology techniques is therefore critical in order to provide information on the dispersion of the related key parameters TSV depth, carrier and glue thickness, Remaining Silicon Thickness (RST) – the thickness of the silicon on top of the

TSV after thinning – and the copper nails dimension, i.e. the height of the TSV extrusion after the TSV reveal process

In this paper, we evaluated several optical metrology techniques for the intra-wafer uniformity control of the specific process steps mentioned previously. The metrology capability was evaluated through repeatability test. The accuracy was verified, where possible, with reference techniques or at least double-checked with comparative techniques.

For the interconnect steps, full field optical metrology techniques have been studied to assess the impact of the environment on the Copper pillar height measurement.

II. Optical metrology techniques

In this section, we describe the optical metrology techniques used for the intra-wafer uniformity measurements of the key parameters associated with the 3D process steps

A. Optical head configuration

Fig. 1 shows an internal view of the patented FOGALE optical system developed and used for the experiments [1]. It includes a top optical head with microscope objectives designed to allow thickness, gap and etch depths measurements by Near-Infrared (NIR) Optical Coherence Tomography (OCT) combined with White light or infra-red microscopy, wafer shape profiling and nails/ pillar height by visible full field interferometry [2, 3, 4].

Fig.2 shows a bottom NIR OCT head can also be inserted for double side measurements. An infra red microscope is included to perform IR inspection of the wafer/carrier interface defect detection.

Mapping can be performed with a fast, motorized XY translation of the aperture 300mm wafer chuck.

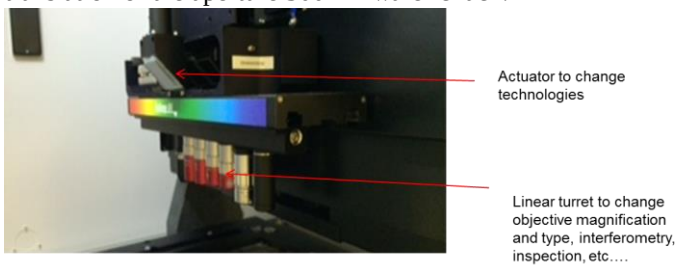


Fig. 1. Internal view of the top head optical system for 3D integration process control

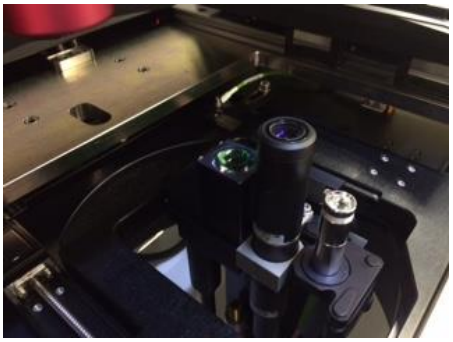


Fig. 2. Internal view of the bottom head optical system for 3D integration combining thickness metrology and IR inspection

By using the NIR OCT, a TSV depth patented method consists in using a beam spot size larger than the TSV diameter [3]. Two groups of waves are coming back from the top and bottom of the measured TSV and give directly the TSV depth without aspect ratio limitation. The combination of this technique with white-light microscopy in the same optical path allows the user to position the spot very precisely and also to obtain top CD.

For silicon, glue and carrier thickness measurements, a commercial system with a dual-probe IR low-coherent Michelson interferometer operating at a wavelength of 1.3µm was used. The specific dual probe configuration where two interferometers are located on different parts of the sample (top and bottom) allowed to obtain individual and total thickness measurements on the same location of the stacked structures.

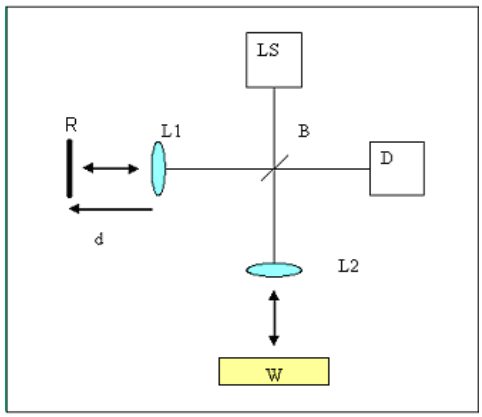


Fig. 3. Echo probe block diagram (Michelson interferometer).

The principle of the Michelson interferometer operating system is illustrated in Fig. 3. The sample is illuminated with a light beam, and a dependence of the reflected light intensity against the interferometer's reference arm length, is mathematically processed. The light is generated by a light source (LS), split by a beam splitter (B), directed, through lenses L1 and L2, to a moving reference arm

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2015/1/000479/2256146/isom-2015-wp53.pdf by guest on 23 November 2022

element (R) and to a sample (W), reflected back, collected together with the same beam splitter, and directed into a detector (D). When the optical path from a beam splitter to a reference arm element R is equal to a path to sample surface, an interference peak happens. For the case of multi-stacked structures, the resulting diagram will present several peaks corresponding to each interface. The thickness of the individual layers can be calculated from the distance between the two peaks divided by the layer's material refractive index [5].

B. Multi-Wavelength OCT in Spectral Mode

By using a 1.31µm Super Luminescent Diode (SLD) as a light source for the NIR OCT, the minimum measured thickness is limited to 20/n µm (n being the refractive index of the layer to be measured). To decrease this value, it is necessary to increase the source bandwidth in order to decrease the signal width. To reach silicon thickness measurement capability down to 1µm, the SLD is replaced by a halogen lamp and the signal is analyzed by a spectrometer. The Fourier transform of the signal gives the thickness value directly

C. White Light Chromatic Confocal

For surface profiling metrology, the White Light Chromatic Confocal technique can be applied [4]. As shown in Fig. 4, this technique uses a custom lens with very large axial chromatic aberration. Thus every wavelength of the large-spectrum source is imaged in a different plane. The one focused on the surface is more coupled with the detector than the others. As there is a unique correspondence between wavelength and distance, the spectrum returned allows extraction of the distance at which the surface is lying.

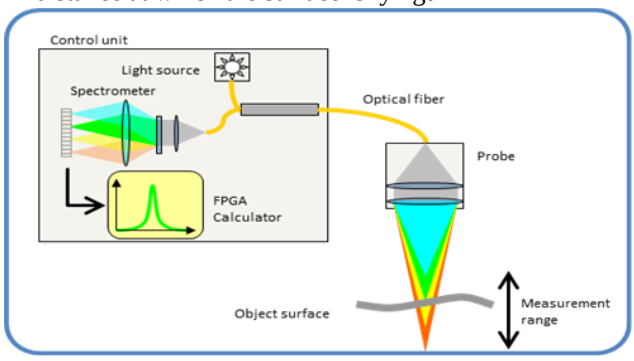


Fig. 4. White Light Chromatic Confocal metrology.

D. Full Field interferometry

As shown in fig.5, full field interferometry is using an interferometric objective for microscopy. The optical view of the sample is converted to an elevation map using interferogram processing techniques. The height of each pixel is determined independently one to each other with a nanometer level accuracy in a single scan. Lateral resolution depends on the objective magnification and camera pixel size.

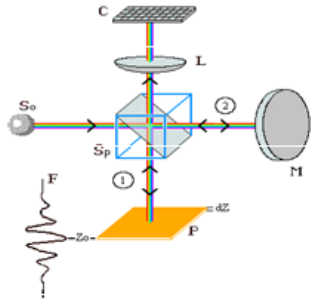


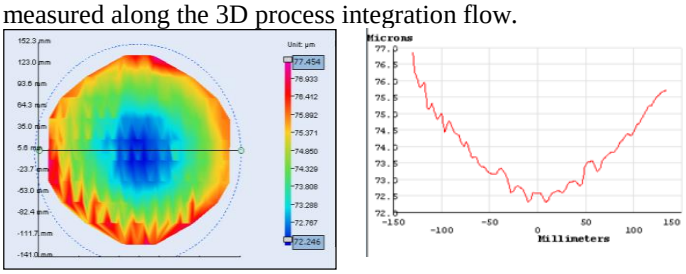
Fig.5: Full Field interferometry

Light is emitted by a selectable light source (So). A beam splitter (Sp) splits the light beam in two half beams marked as 1 and 2. This device is integrated inside the interferometric objective. One of the two beams is reflected by a reference mirror (M), the other is reflected at the sample surface (P) or at internal interface in the case of transparent layers. The cube (Sp) combine the two beams and sends the resulting image, through the tube lens (L), the camera (C).

The intensity I(d) which is measured on one pixel of the CCD camera, varies in function of the difference of length (d) between the two beams ways 1 et 2. This result in an image showing interference fringes following the equal-height lines on the sample.

E. Process steps characterization

For this study, we used an interposer product from a 65nm node technology with middle TSVs of 10µm diameter and 75µm depth. A production lot was run through all the process steps to the TSV reveal process where Copper extrusions are formed at the surface of the stacked wafers. For TSV depth measurement, some wafers were extracted from the production lot. For the bonding, thinning, and TSV reveal process steps, the same production wafers were measured along the 3D process integration flow.



(a) (b)

Fig. 6. (a) Typical TSV depth signature (b) Etch depth profile along X axis.

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2015/1/000479/2256146/isom-2015-wp53.pdf by guest on 23 November 2022

F. Through-Silicon Via Etching

The NIR OCT technique from Fogale was tested to characterize the TSV depth of the etching process. Four wafers from the same production lot were selected at different slot positions (1, 2, 7 and 15) to quantify the intra-lot etching process variability. One individual TSV was measured inside each lithography scanner field in order to perform full map measurement. This leads to 110 individual TSV measurements per wafer.

Repeatability tests were run through 30 static repetitive measurements on the same wafer using a specific 17-points mapping. The 1-sigma repeatability for single via measurement was calculated to be around 0.03µm, which is very low compared to the depth value (0.04%).

To check for the accuracy of this optical technique, comparative XSEM analysis was performed on one of the Middle TSV wafers. As presented in Fig. 7, the TSV depths obtained by XSEM at center, mid radius and edge of the wafer correlate very well with the optically measured values (R^2 = 0.9997). Nevertheless, an offset of about 3.5% was found between the two techniques, XSEM-measured depth values being systematically larger.

TABLE I. TSV DEPTH MEASUREMENTS ACROSS THE LOT

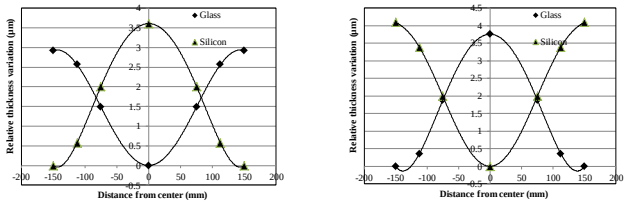
Depth (µm)	Wafer position in production lot			
	Slot1	*Slot2*	*Slot7*	*Slot15*
Maximum	76.89	77.45	77.08	77.82
Minimum	71.65	72.25	71.75	72.14
Range	5.23	5.20	5.31	5.68

Overall, the FOGALE metrology technique was therefore found reliable for the process control of TSV depth, as well as for characterization of the intra-wafer spatial signature.

G. Silicon Bonding and Thinning

Following the Middle TSV etch process, the production lot was run through multiple process steps to perform all the backend metallic connections. Wafers were then bonded on glass carriers with an adhesive layer consisting of 80µm thick resist. At the bonding and thinning steps, we focused on analyzing the Total Thickness Variation (TTV) of the individual layers and of the Remaining Silicon Thickness (RST).

Glass carriers are known to exhibit significant variation. The individual layers and the total stacked layers were measured with IR interferometry described previously. The glue thickness was found to be quite stable, with a small TTV of around 1µm, whereas the glass carriers TTV showed a range of up to 5µm. After the Si grinding process, the individual thickness measurements provide clear evidence that the TTV of the Si grinded layer is dominated by the initial glass carrier TTV. This is illustrated in Fig. 7, where two different glass carrier shapes (convex and concave) as well as the corresponding Si grinded signatures are presented. To generate those simplified graphs, we used the full map thickness data and averaged the values along the different radius from the center wafer in order to get an estimated average profile.



(a) (b)

Fig. 7. Glass and silicon thickness variation across wafer diameter for the case of (a) convex glass signature and (b) concave glass signature.

From Fig. 7, we observed clearly that the glass carrier and the thinned silicon signatures are reversed. This is actually fully predictable, as the grinding process tends to generate stacked Glass/Glue/Silicon wafers with very low TTV values. During the process, the thickness variability of the glass carrier is then simply reported on the grinded silicon layer.

At the grinding process step, we evaluate the combination of NIR microscopy, IR interferometry and IR multi-wavelength spectrometry from Fogale to measure the Remaining Silicon Thickness (RST) above the TSVs [1]. This configuration allows the equipment to position the NIR beam precisely at the bottom of the TSV. We tested the technique on several stacked wafers with different glass carrier TTV signatures to obtain full map data (Fig. 8).

Repeatability test was run through 30 static repetitive measurements on the same wafer using a specific 17pts mapping. The 1-sigma of repeatability for RST measurement was calculated to be around 0.03µm for typical RST values around 20µm. Assessing the accuracy of the results is difficult due to the fact that stacked silicon wafers on glass are very difficult to characterize by SEM cross section analysis. Nevertheless, the RST values found were consistent with the post-grinding silicon thickness measured at a TSV-free location on the wafer, and the TSV depth measured at the etching process step.

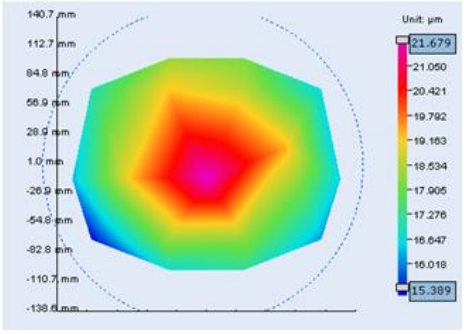
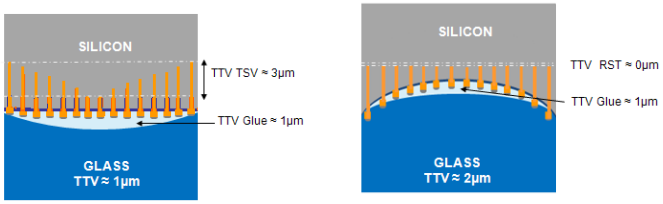


Fig. 8. Example of RST signature with higher values at the center.

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2015/1/000479/2256146/isom-2015-wp53.pdf by guest on 23 November 2022

Finally, we investigate the validity of the reported TTV for the various thicknesses. The TTV reported for the RST measurement were actually in coherence as our expectation. Fig. 9 shows a schematic representation of the intra-wafer signature for the two cases of glass shapes. For the case of Wafer A with concave glass shape, the glass and glue TTV were previously measured and found to be about the same amplitude of 1µm but reversed in sign. The RST TTV then simply results from the TSV depth signature, which was measured around 3µm (Table II). For the case of Wafer B where the glass carrier is convex in shape, the Glass and Resist TTV are cumulative leading to higher TTV values. For the specific case, the resulting TTV is of the same amplitude as the TSV depth TTV but in reverse sign. The very low value for TTV of the RST can be simply explained by a direct compensation effect between both contributions (Table II).



Wafer A Wafer B

Fig. 9. Schematic of the TTV for different cases of wafer shape.

TABLE II. TTV EVOLUTION ALONG PROCESS

Wafer	TTV (µm) within 120mm radius				
	Glass	*Glue*	*TSV*	*RST Predicted*	*RST Measured*
Wafer A	-1	1	-3	3	4
Wafer B	2	1	-3	0	1

We conclude that we can predict the TTV of the RST within 1µm based on the Glass, Glue and TSV etch pre-measured TTV signatures through (1):

$$TTV_{RST} = TTV_{Glass} + TTV_{Glue} + TTV_{TSV\,Etch} \quad (1)$$

Overall, we found that the RST measurements provided by the optical technique were stable and the resulting TTV consistent with the individual signatures.

H. Through-Silicon Via Reveal

The last step of the 3D integration flow studied here concerns the TSV reveal process, which consists in a back side process etching the RST layer in order to reveal the bottom of TSVs named Copper nails. The height of those extrusions is targeted to be about 5µm from the top of the silicon backside surface. The height of the copper nails was measured for the full map by White Light Chromatic Confocal from Fogale (Fig. 10).

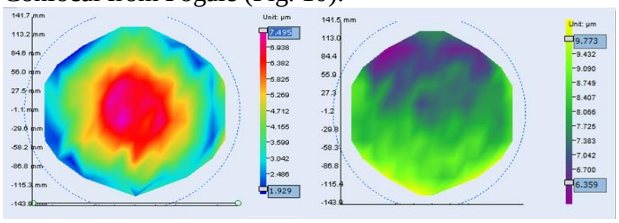
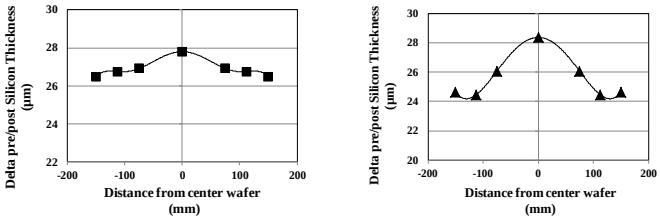


Fig. 10. Examples of copper nail signatures with higher and lower values at the center.

Not only the height values, but also the intra-wafer dispersion of the Copper nail height is critical for further process integration steps. We found that there are strong differences in behavior between wafers from the same production lot. To explain these differences, we studied, for the wafers A and B, the TSV reveal etching profile signature with delta of pre/post measurement of the silicon thickness layer at location on the wafer free of any TSVs and using the same average profile methodology as before (Fig. 11).



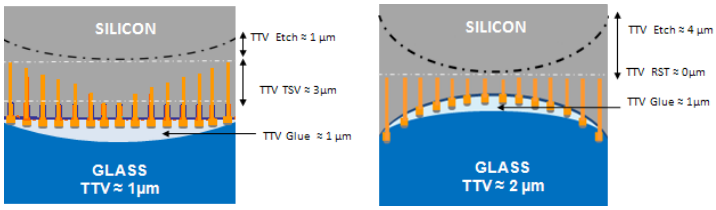
(a) (b)

Fig. 11. Examples of TSV reveal etch signature for (a) wafer A (b) wafer B.

We found that the plasma etching profiles vary significantly depending on the shape of the glass carrier. This is probably due to thermal or charging effects acting differently depending on the thickness of the insulating carrier. There is then a new intra-wafer signature of the final etching process that needs to be taken into account to understand the final copper nail height signature. In Fig. 13, we schematized the various signature contributions including this final TSV reveal step.

Table III reports the copper nail height measured for wafers A and B. The nail heights of the two wafers are found to differ strongly in terms of intra-wafer signature. This is the consequence of both the glass carrier shape leading to different RST TTV, and the TSV reveal etching process signature being strongly impacted by the glass shape (Fig. 12).

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2015/1/000479/2256146/isom-2015-wp53.pdf by guest on 23 November 2022



Wafer A Wafer B

Fig. 12. Schematics of the TTV contribution for different glass shapes.

TABLE III. TTV EVOLUTION ALONG PROCESS

Wafer	TTV (µm) within 120mm radius					
	Glass	*Glue*	*TSV Etch*	*RST*	*TSV Reveal*	*Nails*
Wafer A	-1	1	-3	4 (3)	1	-1 (-2)
Wafer B	2	1	-3	1 (0)	4	3 (4)

We found that the final copper nail height TTV signatures for Wafer A and Wafer B are in agreement within 1µm with the predicted values through:

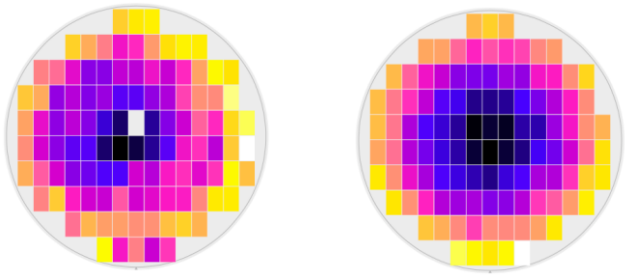
$$TTV_{Nail} = TTV_{Glass} + TTV_{Glue} + TTV_{TSV\ Etch} + TTV_{TSV\ Reveal} \quad (2)$$

Therefore, by knowing the Glass, Glue, TSV Etch TTV as well as the TSV reveal signature, we can predict the Copper Nails TTV. A benefit could be to adapt the TSV Reveal etching process to the RST signature in order to optimize the final Copper Nails signatures.

I. Statistical analysis of TSV process steps uniformity

To quantitatively analyze the model quality and measurement precision with respect to the spatial signature, the site level measurement data post TSV etch, bonding, thinning, and reveal have been aligned and loaded in a semiconductor data analysis system [6]. Here, "site" refers to a fixed position within the lithographic reticle field, of which there are 110 per wafer. The analysis is split in two parts: validation of the effects of the glass carrier shape and bonding on the pre-reveal remaining silicon thickness; and validation of the coherency of the measured copper nail height with the initial TSV etch depth and the remaining silicon thickness post-reveal.

The first analysis models the pre-reveal RST as a function of the thinning process, starting with the glass carrier and glue profile. Figures 13 and 14 show the measured RST *vs.* the modeled maps and site-level values. We observe good correspondence of the spatial wafer profiles as well as good linearity, with a Pearson R^2 = 0.672. The residual standard deviation of 0.68 µm is small compared to the median thickness of the (glass+glue) stack, which was measured at 833 µm.



RST (pre-reveal) model (a) RST (pre-reveal) actual (b)

Fig. 13. Site-level analysis of pre-reveal remaining silicon thickness: wafer maps

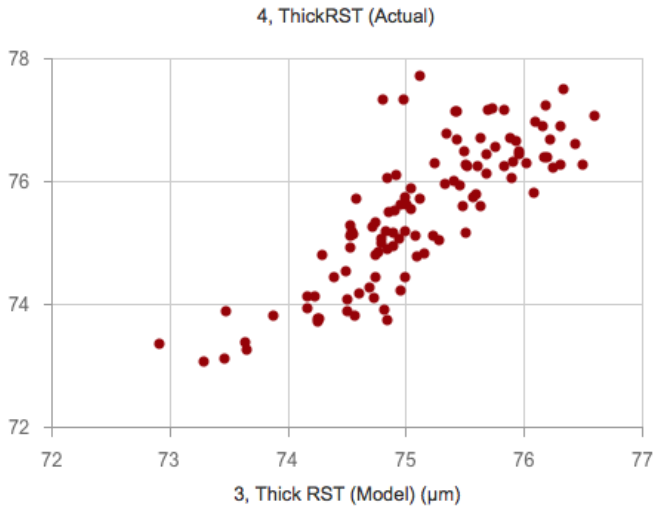


Fig. 14. Site-level correlation of pre-reveal RST *vs.* modeled RST, based on a median (glass+glue) stack thickness of 833.0 µm.

The second analysis validates the coherency between the TSV etch measurement (NIR OCT) and the post-reveal measurements (WLCC) for RST and copper nail height. Fig. 15 shows the measured copper nail height *vs.* the theoretical nail height, calculated as the difference between the TSV etch depth and the remaining silicon thickness post-reveal. A good linearity is observed, with a Pearson R^2 value of 0.713. A mean offset of 3.1 µm is present between actual and modeled heights. In view of the results of Sec. IIIA, the offset is probably dominated by the TSV etch measurement.

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2015/1/000479/2256146/isom-2015-wp53.pdf by guest on 23 November 2022

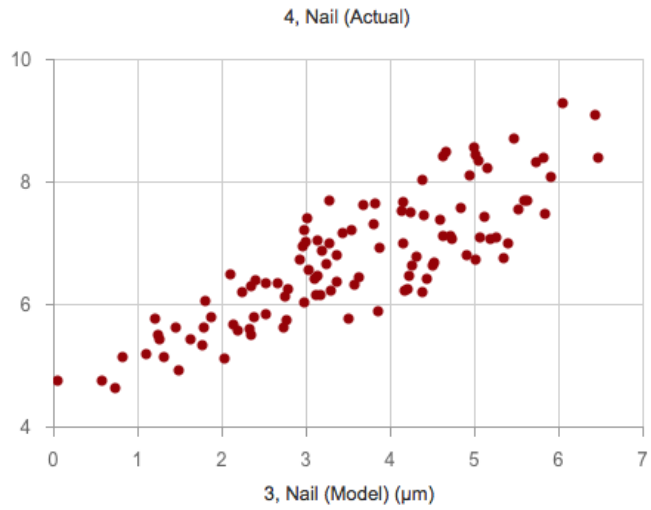


Fig. 15. Site-level analysis of measured copper nail height *vs.* expected height from TSV etch depth and post-reveal RST.

For smaller copper nails diameter, confocal chromatic and other line scanning techniques have lateral resolution limitations (Fig.16). Full field field interfometry is then the technology of choice for diameters below 3µm (Fig.17).

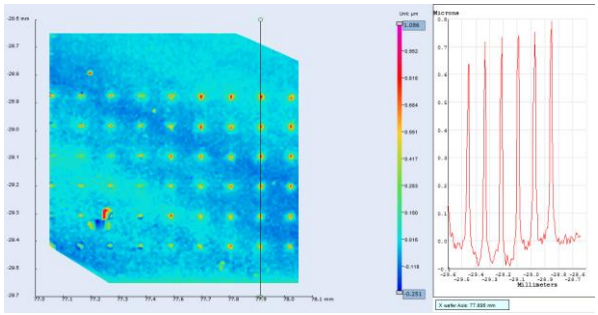


Fig. 16. 3µm diameter copper nail field with confocal chromatic technology: limitation due to lateral resolution.

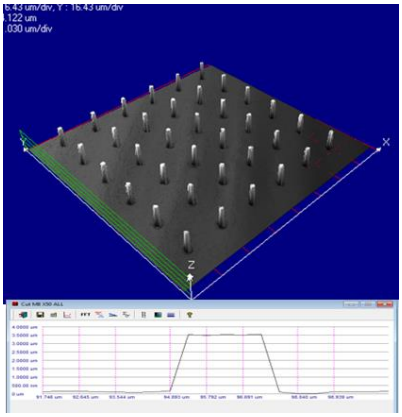


Fig. 17. 3µm diameter copper nail field with high lateral resolution full field interferometry.

II. CONCLUSION

We have studied the benefit of various optical metrology techniques for the in-line uniformity control of 3D stacked wafers. Multiple optical technique configurations were implemented and allowed the monitoring of all process steps related to 3D IC applications. Through analysis of the complete set of measurement data collected, we demonstrated the impact of the dispersion of each process step on the final copper nail height signature. The study raised the importance of the glass carrier TTV control and/or selection. The glass shape is demonstrated to have a high impact on the Silicon thinned TTV layer and the TSV reveal etching process leading to Copper nails TTV signature strongly dependent on the stacked wafer configuration.

(1) References

[1] G. Fresquet, "Optical device and method for inspecting structured objects" Patent WO 2011135231, FR 2959305.

[2] A. Courteville, R. Wilhem, and F. Garcia, "A novel low coherence fibre optic interferometer for position and thickness measurements with unattained accuracy," Proc. SPIE 6341 pp.63411Q , 2006.

[3] A. Courteville, "Method and device for measuring heights of patterns". US Patent 7,782,468.

[4] F. Quercioli, M. Trivi, G. Molesini, and M. Melozzi, "An optical probe based on spherical aberrations for surface figure testing"; Optics Communications, 71(1-2), pp. 11-14, 1989.

[5] D. Le Cunff, A. Pravdivtsev, K. Le Chao, S. Couvrat, C. Euvrard, E. Deloffre, and A. Cailean, "Use of optical metrology for wafer level packaging of CMOS image sensor" Proceedings 3DiC Conference Munich 2010.

[6] *Silicondash*. Qualtera SAS. [Online] Available: http://www.qualtera.com

Acknowledgment

Part of the work presented in this paper, was supported by the European EUREKA CATRENE program (MASTER 3D project).

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2015/1/000479/2256146/isom-2015-wp53.pdf by guest on 23 November 2022