Wafer Level Integration of MMIC and Microwave IPD with Metal/BCB Multilayer Interconnection Based on Low Resistance Silicon

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Abstract

A new high-density wafer-level integration of a GaAs based monolithic microwave integrated circuit (MMIC) chip and a microwave integrated passive device (IPD) is presented. This integration technology, an important and IC-compatible option for system-in-package (SiP), utilizes bulk Si fabrication and film deposition based multichip module (MCM-D) process. MMIC is entirely embedded into the silicon wafer while IPDs are integrated on the dielectric layers simultaneously with the metal/BCB multilayer interconnection. Key fabrication processes and crucial technologies are described in detail. Normal silicon wafer is selected as substrate because of its mature processing technology, low cost, good thermal dissipation as well as its thermal expansion matching with GaAs. To obtain excellent microwave performances and good planarization, thick photosensitive BCB of 25um/layer is adopted as dielectric and thus the use of tapered via that is hollow inside or filled by BCB is a cost-effective way to accomplish inter-layer connection instead of Au bump bonding or column used in dry-etch BCB process. Further promotions on microwave performances are achieved by the shielding effect through ground layer coverage on silicon surface and the application of microstrip lines. Several experiment results such as dc inter-layer connection resistance and thermal resistance measurements are complemented to investigate the characteristic of the whole package. The Microwave properties of the integration sample are measured by transmission performance test from 15GHz to 30GHz. The measurement results are analyzed and discussed comparing with the theoretical or simulation results.

Key words: wafer-level, integration, MCM-D, BCB, IPD, MMIC

Introduction

Miniaturization of electronic products becomes an overwhelming trend in driving revolutionary changes in the integration technology. Reductions in dimensions and costs as well as improvement in performance are the main challenges. Especially, the booming development in communications put forward the requirement of microwave compatibility requirements to the electronic system. Therefore, the integration of a functional system including multiple microwave monolithic integrated circuit (MMIC) chips and the microwave passive devices is inevitably the most basic and crucial issue since many important aspects like the integration intensity, the guarantee in high quality-value (Q-value) of the microwave passive devices and the RF matching between the microwave chips and the devices should be taken into consideration not only in theoretical design but also in fabrication process [1-2]. To adapt the progress in subsystem or system integration from single chip to multichip, from two-dimensional (2D) to three-dimensional (3D) fabrication and from single die to system integration, a lot of high-density integration technologies have been developed [3-5].

By applying these integration technologies, monolithic chips and passive devices can be integrated in the system mainly by three ways distinguished by the spatial location of the passive devices which is schematically shown in figure 1: integrated on chips, integrated on intermediate dielectric layers and mounted on surface. With respect to system-on-chip (SOC), on-chip integration suffers the bottleneck of lack of high quality passive devices owing to the high-loss characteristics of silicon substrate based on RF CMOS process. And the cost is also a limitation due to the large chip/board occupation of the passive devices. Surface mounted technology (SMT) is one of the most popular technologies for its high density, small size, high reliability, good high-frequency performance and automation. Discrete passive components, modules and even chips are mounted on the surface of the board. However, the integration density and the heat dissipation are barely satisfactory. Integrated on intermediate dielectric layers, for example, on low temperature co-fire ceramic (LTCC) [6], multichip

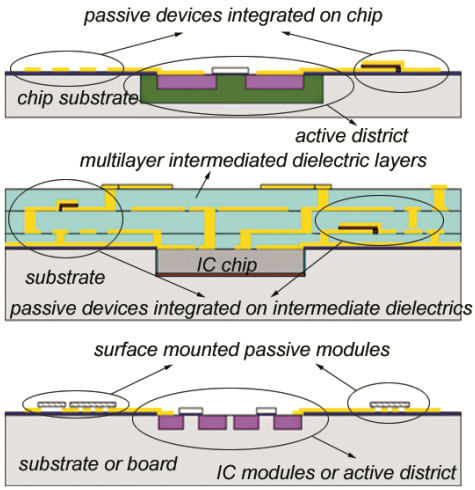


Figure 1: Passive devices integrated on chip, on intermediate dielectric layers and surface mounted.

modules (MCM) [7] and system-in-package (SiP) [8] technologies, passive devices can be fabricated with higher quality values (Q value) because of the reduction of stray capacitances and inductances. And higher integration density and efficiency can also be achieved. Compared to the former two ways, integration on dielectric is a more prospective method in microwave application in spite of the higher unit cost. However, the total cost may not be as high as what we thought after considering some other factors such as the increasing yield.

In this paper, a new high-density integration technology used to integrate MMIC chips and integrated passive devices (IPD) into one package at wafer level is presented. IPDs are fabricated on multilayer intermediate dielectric layers (BCB) under which the MMIC chips are embedded in the trench formed on Si substrate. Low-resistance silicon is adopted as substrate not only for its mature process but also for its good physical properties such as low cost, good heat dissipation and good thermal expansion matching with the material of MMIC chips (GaAs), etc. Furthermore, it can avoid the shifting induced by curing and difficulties in handing in wafer-level integration compared to other materials such as organic, ceramic and laminated layers [9]. This technology combines both bulk silicon process and thin-film technology, one of the most popular technologies in industry. To overcome the restrictions in microwave frequency range, the structure applies microstrip lines (MSL) to transmit high-frequency signals, and the loss that arises from the Si substrate can be shielded by ground plane. A thick layer of low dielectric permittivity material, BCB, is used to reduce the dielectric loss and further to improve the microwave performance. Moreover, in such package, varieties of functional chips and MEMS devices can also be integrated. In section II, a brief description of the integration structure and the fabrication process are presented. In section III, the key technologies of the process such as BCB deposition and embedding are described in details. Section IV presents some measured results of the parameters of the interconnection between MMIC and the IPD, e.g. *inter-layer connection resistance, via geometry parameters and thermal resistance.* In section V, microwave performances of a MMIC chip and a band-pass filter are measured at wafer level up to 30GHz.

Description of the Design and Fabrication

Structure and Material Selection

In this work, MMIC chips are arranged face-up and stuck on with conducting glue in the trenches on a low-resistivity silicon substrate (1-10ohm·cm). The trenches are fabricated in advance by KOH wet etching simultaneously with the etching of alignment marks. Photosensitive BCB (photo-BCB) is selected to form the intermediate dielectric layer due to its low permittivity, low cure temperature (<250^{o}C), photosensitive capability and excellent thermal and chemical characteristics. BCB with about 25μm thick of each layer and total thickness of 50μm are deposited for the purpose to reduce the dielectric loss in microwave band. Similar to the semiconductor process, tapered vias on photo-BCB are easily formed to connect the upper and bottom layers. The use of photo-BCB can omit the processes of electroplating for the inter-layer via filling and successive CMP, greatly reducing the process complexity and the process cycle, and accordingly is cost-effective compared to the non-photosensitive process [10]. The patterns and the metal parts of the microwave passive devices are made of gold thin film which possesses the advantages of the high conductivity, good ductility and good stability against oxidation in order to achieve low conductor loss. The signal transmission lines have a thickness of more than 3μm to avoid the skin effect. Three layers of metal layers and two layers of intermediate dielectric layers are fabricated in this integration structure.

Process Flow

The integration method of the MMIC chips and microwave IPDs are briefly described as the following:

i. A deposition of a 2μm silicon dioxide layer used as a mask of the etching of the trenches and the alignment marks;

ii. Lithography to form the etching windows of the silicon by buffered oxide etch;
iii. Formation of the trenches and the marks by wet etching;
iv. Ground shielding layer formation on the seed layer of TiW-Au;
v. Embedding and location adjustment of the chips;
vi. BCB deposition, lithography and development;
vii. BCB soft cure and polymer residue removal;
viii. Metal patterns and IPD fabrication;
ix. Material deposition of the IPD and metal redistribution line (RDL) (optional);
x. Repeating step vi to ix to complete multilayer fabrication
xi. BCB hard cure.

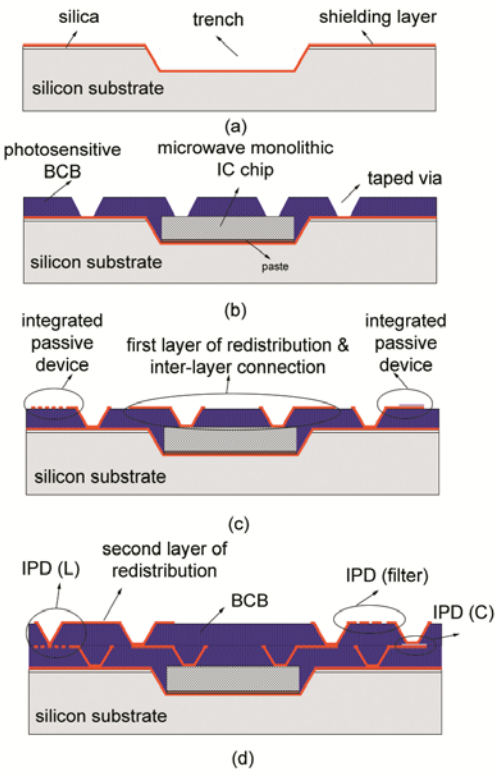


Figure 2: Process flow. (a) substrate preparation, i.e. step (i)~(iv); (b) chip embedding and BCB lithography, i.e. step (v)~(vii); (c) first layer of RDL and IPD fabrication, i.e. step (viii)~(ix); (d) multi-layer RDL and IPD fabrication

Some notices are necessary to be mentioned in the process. The electroplating is used to thicken the shielding layer to 3μm. The RDL and the metal parts of the IPDs are fabricated by seed layer evaporation and electroplating. Considering the adhesion of BCB, the seed layer is composed by Cr-Au, and some surface pretreatments should be done before metal deposition. Figure 2 illustrates the schematic diagram of the main process flow. Detailed process steps of the photo-BCB process can refer to our previous work [11].

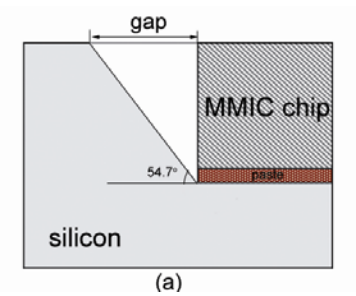
Key Issues related with the fabrication

Inter-layer Connection

The inter-layer connection is achieved by BCB lithography and metallization. After BCB exposure and development, the surface of the tapered vias are covered by some residual polymer which can be removed by a descum step [12]. The wafer is processed by O_2/SF_6 etching with a flow ratio of about 4:1 for a while, and thus the metal pads of the bottom patterns are exposed. To improve the adhesion between BCB and gold, a conversion of 60%~70% is appropriate in multilayer fabrication. A plasma pretreatment and adhesion promoter is also necessary. Since the height of the via is about 25um, a relatively thick seed layer of Cr-Au should be evaporated to form good inter-layer connection.

Planarization of the Wafer Surface

A gap between the embedded MMIC chip and the wafer is formed in this work because of the sidewall corrosion angle of 54.7° of the <100> silicon by wet etching, as shown in figure 3. The thickness of MMIC chip is approximately 100μm while the thickness of the paste is about 10um-15um. And the chip should be horizontally placed to make the top surface of the chip maximum 5μm higher than the wafer surface. Otherwise, parts of the MMIC chip tend to be exposed after BCB coating (figure 4). Therefore, gaps with a width of about 78μm at each edge of the trench are formed. The gap will lead to poor BCB coverage that may cause short or open circuit problems. To minimize the impact, accurate trench size and depth are carefully controlled not to broaden the gap. Furthermore, a short period of time is needed to make BCB spilled into the gap before spin-coating followed by a horizontal placement between coating and the pre-bake. The planarization can be greatly improved by dividing the coating of BCB into two steps with half thickness each. Figure 5 reveals the top view of the improved gap coverage.



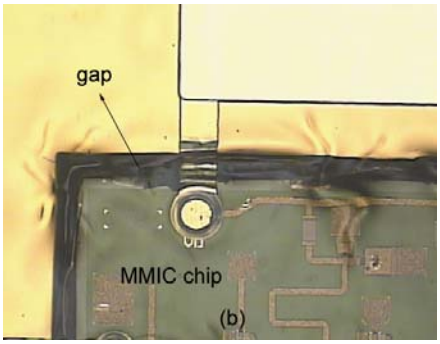


Figure 3: The gap between embedded MMIC chip and the substrate. (a) schematic sectional view; (b) photograph of the top view.

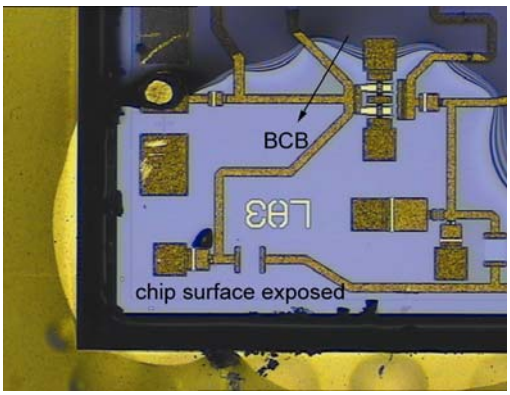


Figure 4: Chip surface exposed after BCB coating due to the slanting or excessive high placement of the chip

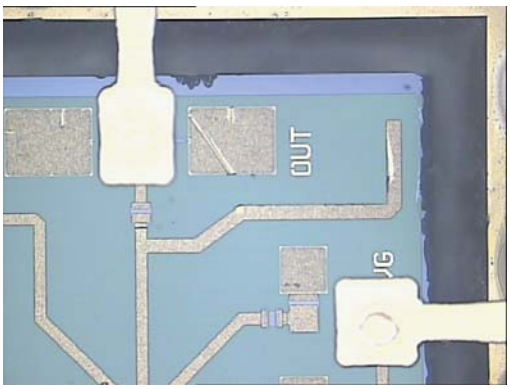


Figure 5: the improved planarization of the gap after twice BCB coating.

Results

Interconnection Characteristics

Maximum three layers of BCB and three layers of metal patterns are fabricated in addition to the ground plane. Since a wall angle of about 60^{o} appears after the BCB lithography, the inter-layer via is tapered and inter-layer conductor line climbs along the profile of the tapered via. Figure 6 is the top view of the metal/BCB interlayer connection through via. To investigate the direct circuit (DC) electrical characteristic of the inter-layer connection, daisy chains with three layers of BCB are fabricated, measured, compared to the short-circuit MSLs on the top layer. Figure 7 shows the daisy chain test vehicle used to measure dc resistance of the interlayer connection. The detailed descriptions of the measurement methods to obtain the wall angle of BCB as well as the resistance of the inter-layer connection are referred to [11]. In this work, 20 groups of specimens are measured, and the average DC inter-layer connection resistance with vias of 100μm in diameter is measured to be 79.02mΩ.

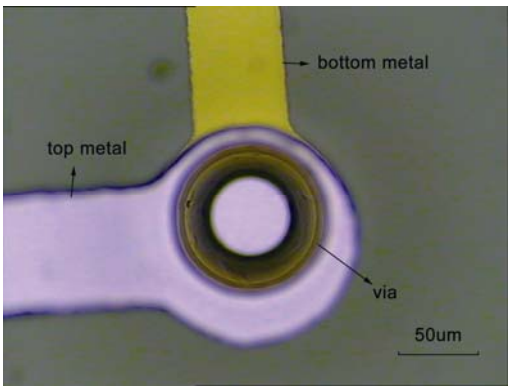


Figure 6: photograph of the metal/BCB interlayer connection through via

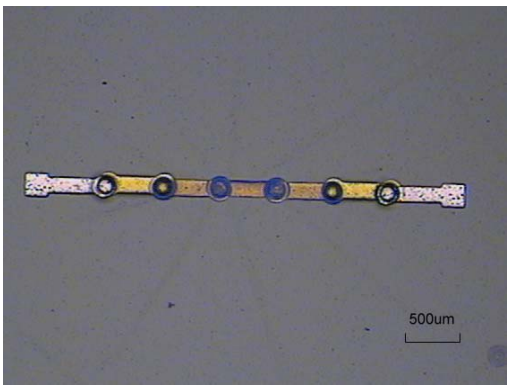


Figure 7: the daisy chain test vehicle used to test dc resistance of the interlayer connection.

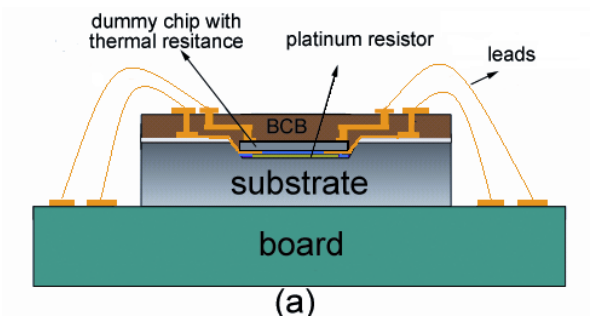
Heat Dissipation Characteristic

In the integration structure, the MMIC chips are embedded in the silicon trench and covered by layers of BCB which is not a good conductor of heat. So it is necessary to build a test structure to evaluate the heat dissipation characterized by thermal resistance. Figure 8 (a) and (b) illustrates the test structure and specimen for thermal resistance measurement. Meander resistor is fabricated on the

bottom of the trench where underlying silica has been deposited to isolate the resistor from the silicon, as shown in figure 8(b). Outlet strips are fabricated by seed layer sputtering and electroplating to lead the resistor pads out to the substrate surface. After a layer of silica is deposited to fully cover the resistor by PECVD, the dummy chip with resistance heater is placed into the trench and fixed. Then the specimen is fabricated according to the process flow mentioned above. The test model after package is also shown in figure 8(b). Several materials have been tried to fabricate the resistor, e.g. tantalum nitride (TaN_x), chromium (Cr), boron doped semiconductor and platinum (Pt). Considering the linearity of the temperature coefficient of resistance (TCR) and the measurable range, Pt is finally selected as the resistor. During the test, the specimen is stuck on the PCB board and is kept in an oven of which the initial temperature is set as 30°C. Figure 9 shows the measurement results of the resistance of Pt changing with the temperature from 30°C to 130°C. The TCR of Pt is calculated to be 1528 ppm/°C. The power of the resistance heater keeps 0.16w which is very close to the power of our MMIC chip (0.15w). After the temperature is stable, the thermal resistance of the integration specimen which means the temperature difference per power between chip-substrate interface and the atmosphere can be expressed as [13]:

$$\theta_{ja} = (T_j - T_a)/P$$

T_j represents the junction temperature, T_a represents the atmosphere temperature and P is the power. With the whole test system stood at 30°C for enough time until the temperature is stable. The interface temperature kept 37.2°C and the thermal resistance was calculated to be 45°C/watt. It should be noted that since silicon have a high thermal dissipation capability, part of thermal dissipation is contributed to the PCB board on which the specimen is stuck.



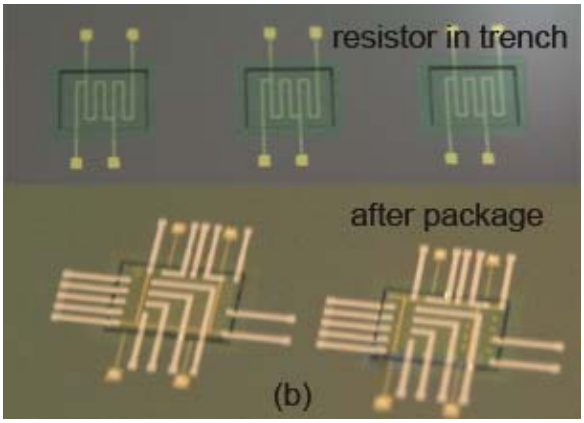


Figure 8: The test structure and specimen of the integration for thermal resistance test. (a) schematic diagram; (b) platinum resistor in silicon trench and the top view after package.

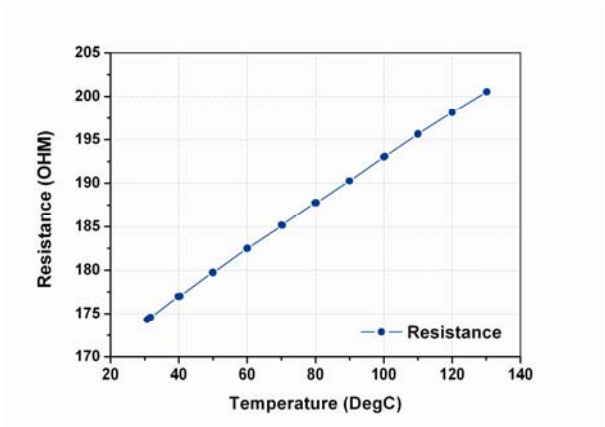


Figure 9: the measurement results of the resistance of Platinum versus the temperature from 30°C to 130°C

Microwave Performance

A specimen including an embedded MMIC chip (active amplifier) and a band-pass filter are fabricated to measure the microwave transmission performance of the integration structure which is a part of the RF front-end subsystem. The filter is fabricated on the top of the package and connected to the input end of the MMIC chip. The centre frequency of both the BPF and the MMIC chip is designed to be 24GHz. The gate voltage and the drain voltage of the amplifier are -0.4V and +3V, respectively. Figure 10 shows the photograph of the specimen, and the measurement results of S parameters are shown in figure 11 from 15GHz to 30GHz.

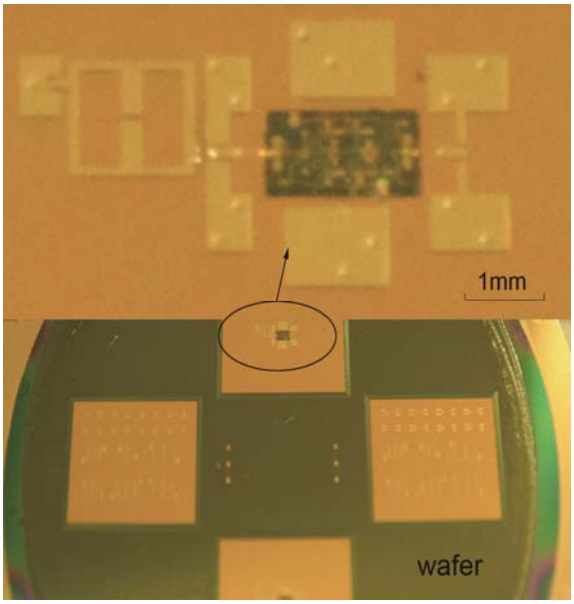


Figure 10: Photograph of the specimen and the wafer for microwave performance test

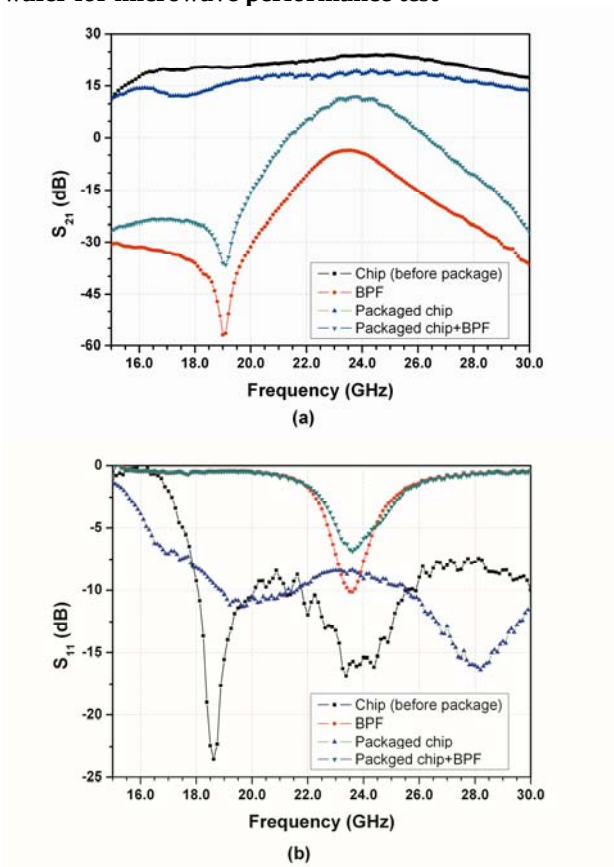


Figure 11: the measurement results of S parameters. (a) S_{21}; (b) S_{11}

As shown in figure 11(a), the gain around the centre frequency ranges between 18.3dB and 19.4dB, i.e. the average gain degrades for about 5dB. The maximum gain is 19.4dB at 24.3GHz where the centre frequency drifts for 500MHz. The 3dB pass-band width of the BPF is 2GHz from 22.5GHz to 24.5GHz, and the centre frequency is 23.5GHz with the minimum insertion loss of 3.6dB. When the BPF is connected to the input end of the amplifier chip, the maximum gain degrades to 11.95dB with an additional gain drop of more than 7dB. And the gain exceeds 10dB in the range between 22.9GHz and 24.6GHz. Figure 11(b) shows the measurement results of S_{11}. The return loss of the packaged chip is better than 8.35dB in the measurement range. However, the maximum return loss is 6.8dB which is increased by about 1.6dB.

Discussion

In microwave performance results, a relatively large loss is noticed after packaging. After a measurement of the MSL that is the same in structure and length with the lead-out MSL in the integration, the loss of lead-out MSL is about 1dB. The loss of about 3.6dB is obtained from the BPF in the integration structure including the packaged chip connected with the BPF. An additional degradation of about 4dB appears in both cases after the package. We attribute the loss mainly to the impedance mismatch resulting from the interlayer connections between MSLs and the MMIC chip as well as the connection between the filter and the MMIC chip. A possible reason for the impedance mismatch is the deviation between design and process because of the inadequate process accuracy. Compared to our previous work using dry-etch BCB [10], the gain of the MMIC chip after packaging degrades seriously in this work. It means more losses are caused by using hallo tapered vias to achieve the interlayer connection than by using metal columns to some extent despite the frequency is higher here. The possible reason could be attributed to that more parasitic parameters were induced in such structure and the match between inter-layer connection and the MSL was not as good as the original designed one due to the deviation caused by process inaccuracy, for example, the deviation in width of MSL. It should be noted that the performance could be improved by optimized design and more accurate process control.

There will be some approaches to be applied to electronic static discharge in our future process. For example, grounding circuit can be designed in the course of layout and process design. And if the chip can be embedded after most processes are completed, the potential failure of electrostatic problem will be reduced more or less. So the integration method that MMIC chips are embedded on back of the substrate may be prospective.

Conclusion

An integration of MMIC chip and microwave IPD with BCB/metal multilayer

interconnection at wafer level on low-resistivity silicon is presented. The key fabrication technologies and the brief process flow are introduced. Test structures for both dc resistance of the inter-layer connection and thermal resistance are designed and the measurement results are presented. A specimen including a microwave amplifier chip and a BPF which connect together is fabricated and measured. The results demonstrate the feasibility of the integration method. And this technology is applicable in microwave band and is cost-effective. More efforts on wafer-level microwave system integration are in progress.

Acknowledgments

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