Use of Wafer Applied Underfill for 3D Stacking

Antonio La Manna, K. J. Rebibis, C. Gerets, E. Beyne
IMEC, Kapeldreef 75, B-3001 Leuven, Belgium
Tel: +32 16 28 199, Fax: +32 16 281 097; Antonio.lamanna@imec.be

Abstract

A key element for improving 3D stacking reliability is the choice of the right Underfill materials.
The Underfill is a specialized adhesive that has the main purposes of locking top and bottom dies; it must fill the gap between bumps and between dies, while reducing the differential movement that would occur during thermal cycling. Traditional underfill processes are based on local dispensing after solder bump reflow (Capillary dispensing), or before flip chip operation with no need of reflow (No Flow Underfill, NUF). In case of 3D stacking, such processes present some limitations: need of a dispensing area (die size increase); material flowing (spacing between dies) and cost (low throughput). After an introduction on typical underfill applications like die-to-package and die-die assembly, we report the work done to assess the properties of several Wafer Applied Underfill (WAUF) materials and their integration in 3D stacking. These materials have been initially applied on silicon wafers in order to assess the minimum achievable thickness and the material uniformity. The wafers have been coated by using different methods: spin coating and film lamination. After this initial assessment, the most promising materials have been used for 3D stacking. The test vehicle used has Cu/Sn µbumps with a pitch of 40µm. The quality of the materials is judged by electrical test, SAM (Surface Acoustic Microscope) and X-SEM (Scanning Electron Microscope).

Key words: wafer applied underfill, 3D Integration, multi-die stacking

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2011/1/000008/2343492/isom-2011-ta1-paper2.pdf by guest on 23 November 2022

Introduction

The semiconductor industry has followed the Moore's Law for more than 40 years. The concept of scaling based on this law is now nearing the end and to maintain the same scaling concept new routes are being investigated. These new routes are commonly identified as 'More-than-Moore' technologies and the most important of them is 3D-IC integration.
Although significant results have been achieved, 3D-IC integration still presents uncertainties that are delaying high volume production. One of these concerns is the reliability of 3D stacking.
A key element in 3D stacking reliability is the choice of the correct UF to integrate in the assembly processing: die stacking and final packaging. During thermo-cycling or normal working conditions, the solder joints die-package or die-die (3D-IC) are affected by fatigue and local stress that can generate failures (e.g. cracks, delamination, refer to Figure 1). The main scope of UF is to mitigate the effects of this stress and protect the chip from moisture entrapment and other contaminants (refer to Figure 2), which can compromise chip performances in next steps [1]. The requirements for underfill are different as they depend on the target assembly process: die-to-package or die-to-die. In both cases, the choice of the right material is not straightforward.

In case of die-to-package assembly the UF will have to mitigate the differences between the package substrate (typically an organic laminate), the solder bumps (typically ~100µm sizes), the silicon die and the package overmolding. While in case of die-to-die assembly the underfill have to mitigate the difference between two silicon dies and micro-bumps (typically ~10µm sizes).

In the following paragraphs we will give some more details on the die-to-package and die-to-die assembly approaches, later we will focus on Wafer Applied UF for die-to-die and die-to-wafer assembly.

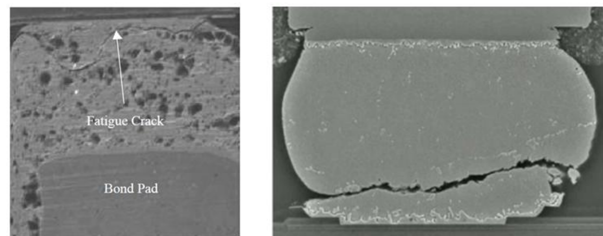


Figure 1: Example of solder fatigue cracks

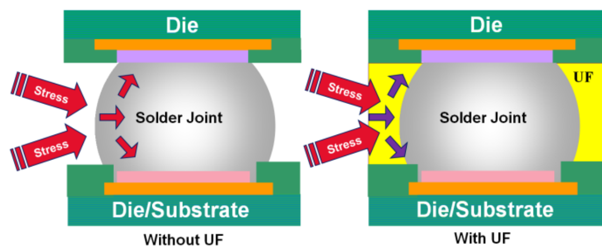


Figure 2: Underfill mitigates the stress on the solder joint

Underfill in die-to-package assembly

Underfill materials and processing are key elements in flip chip BGA (Ball Grid Array) packages. In a flip chip BGA (refer to Figure 3) the die is assembled on multi-layer organic substrate, which is finally soldered onto a PCB (Printed Circuit Board) by solder balls.
In the case of a 4-metal-layers substrate, the stack-up typically consists in a thick BT (Bismaleimide-Triazine, resin based), usually identified as laminate core and coated with copper (inner copper layers).

The inner layers are enclosed by new dielectric layers (*Pre-preg*, pre-impregnated composite fibers) that are followed by a new copper lamination. The external copper layers are finally protected by coating a Liquid PhotoImageable (LPI) solder resist (typically epoxy or epoxy-acrylate). The solder resist is than selectively etched to allow the connections die-substrate (FC pads) and substrate-board (Solder Ball pads).

To avoid pad oxidation and/or improve solder-ability, FC and Solder Ball pads can have different metal finishing (Ni, Au, NiAu, etc.) or OSP (Organic Solder-ability Preservatives) coating. The different properties of all these materials heavily affect the thermo-mechanical loads applied to the solder joints.

In a standard working environment, the flip chip BGA package is exposed to several thermo-cycles (e.g. -40°C/+125°C for reliability check), this creates materials deformation and fatigue damages like cracks and/or delamination as shown in Figure1. This kind of failure can be limited if the materials used have similar properties. CTE (Coefficient of Thermal expansion) and Young's modulus (E) are two main parameters to consider when defining a BGA package. On the other hand, for adhesives like UF, another important parameter that needs to be taken into account is the Tg (glass transition temperature). The Tg of an adhesive indicates the temperature at which the adhesive changes from being a glassy solid to a rubbery material, and usually these transition means a significant increase in the CTE value. The CTE value below Tg is defined as $\alpha 1$ and the CTE value above Tg is defined as $\alpha 2$. The high CTE values of underfill, especially $\alpha 2$, would cause high shear strain in the thermal shock condition, induced by the CTE mismatch. This is the reason why most underfills are formulated to have a Tg value well above the use temperature.

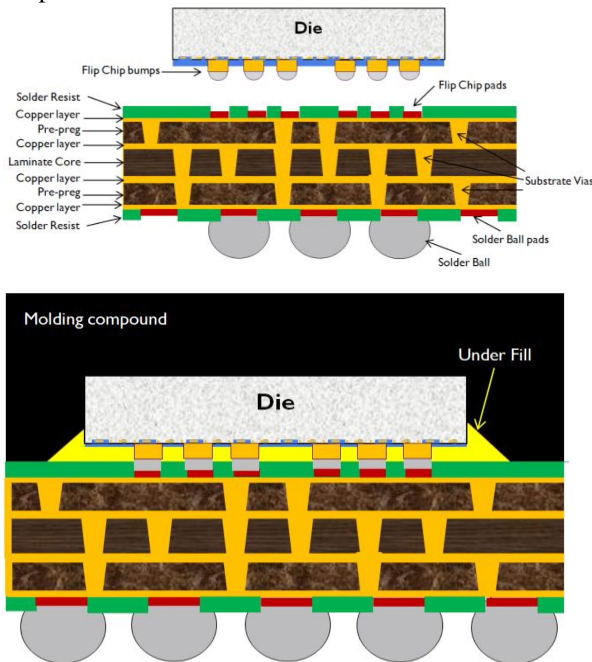


Figure 3: Typical stack-up for Flip Chip BGA

Table 1 illustrates the Young's modulus and the CTE values for typical materials in FC BGA package.

Material	E (GPa)	CTE (ppm/°C)
Aluminum	70	23
Copper	117	17
Diamond	940	1
Nickel	200	13
Silicon Carbide	450	2.77
Silicon	169	3
Gold	80	14
Solder bump *(Pb90Sn10)*	27.3	24.5
Solder bump *(Sn3.5Ag)*	30	21.5
CuSn IMC	110	23
Polyimide	8.3	15
Silicon Nitride	250	3.2
Epoxy	15	55
Molding compound-1	17	18
FR-4 substrate	17	3
BT-substrate	15	27
Ceramic-substrate	85.3	14

Table 1: Young's modulus and CTE for typical FC BGA package materials

Material	E (Gpa)	Tg (°C)	CTE (ppm/°C) $\alpha 1$	CTE (ppm/°C) $\alpha 2$
Capillary_UF1	9.0	100	26	90
Capillary_UF2	2.9	125	40	125
Capillary_UF3	2.0	110	50	160
NUF_1	2.6	81	75	190
NUF_2	5.8	87	31	64
NUF_3	8.6	87	30	71
NUF_4	3.4	152	56	172
F-WLUF_1	8.4	110	31	116
F-WLUF_6	6.8	118	47	147
F-WLUF_7	3.8	128	35	148
F-WLUF_3	5.6	109	43	89
L-WLUF_4	8.5	93	32	165
L-WLUF_5	2.8	117	78	210
L-WLUF_2	1.7	74	49	284
Molding compound-1	23.5	125	0.9	3.4
Molding compound-2	18	180	13	38

Table 2: Material properties for some evaluated materials. Notes: F-WLUF indicates Film wafer level UF, L-WLUF indicates Spin coatable UF. Molding compounds are included as reference

In flip chip package, the underfill is used to fill the gap between the die and substrate (refer to Figure 2). The application of underfill reduces the thermal expansion mismatch between the silicon die and the organic substrate and protects the solder bumps [1]. Underfill is normally applied at one or more sides of the die by filling the gap die-package under capillary action (Capillary underfill). The quality of the filling process is depending on parameters like die size, bump pitch, gap height, underfill viscosity, flow time, surface tension, wettability of substrate solder mask, die passivation layer, and bumps material [2,3]. The best combination of all these parameters is the key factor for successful flip chip package. The use of capillary underfill is time consuming as it requires enough time

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2011/1/000008/2343492/ism-2011-ta1-paper2.pdf by guest on 23 November 2022

for the capillary action and an additional curing step. These two aspects are not negligible and negatively affect the assembly throughput.

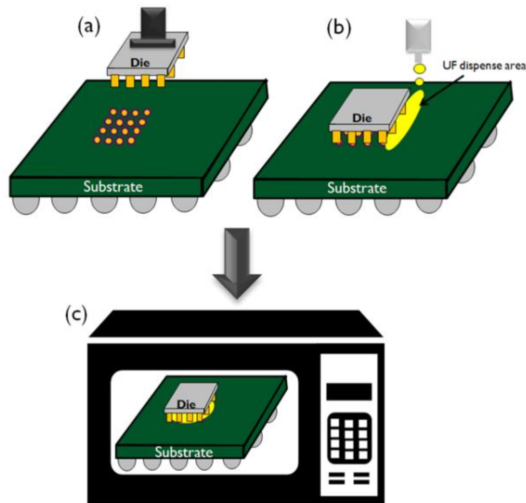


Figure 4: Assembly process in case of capillary UF: a) Die Flip chip; b) UF capillary dispense; c) UF curing.

Furthermore, apart the processing time, another concern that is related to capillary underfill is the area required for dispensing. To ensure a complete gap filling in acceptable time, enough dispensing area should be available on the landing substrate. This is not always the case for components requiring high system integration and, together with timing requirements, represent a key disadvantage of capillary underfill.

To circumvent these issues, two approaches are nowadays being considered: vacuum underfill and no flow underfill (NUF).

The first approach (vacuum UF) is mainly an extension of the capillary UF by enhancing material flowing with gas pressure [4]. This approach is at the moment still in a concept phase and far away from becoming a standard for volume production. It offers advantages in term o good gap filling (e.g. no air bubbles trapped), but still presents concerns in term of throughput and required equipment upgrade.

The second approach based on NUF is instead more used. In this approach, the material is dispensed on the landing substrate before die stacking. In this case, the flip chip operation has the double function of bonding die-substrate and curing the UF [5]. This approach well fits the standard flip chip operations and, even if UF is not fully cured during stacking (typically ~90% of material is cured), the complete curing is obtained by the following assembly steps like post molding cure. Also this approach anyway presents a few concerns like: material needs to be transparent to see alignment marks during FC operation, dispense timing (still done for each single die), UF/filler entrapment between bumps, voids and other defects related to material flowing. Problems like transparency and filler entrapment can be solved by using filler-less or nano-filled materials, but both options have disadvantages for reliability and cost.

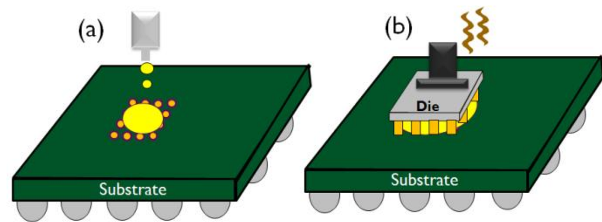


Figure 5: Assembly process in case of No flow UF: a) UF dispensing; b) Die flip chip.

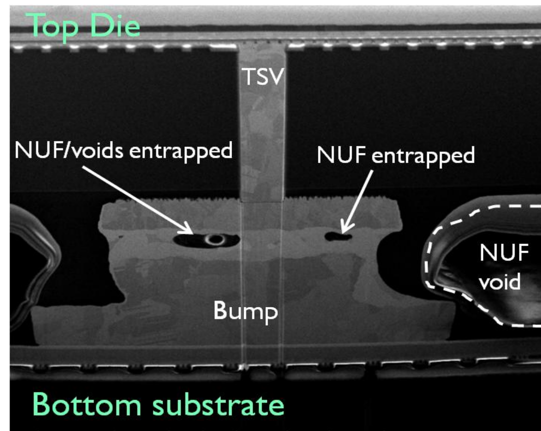
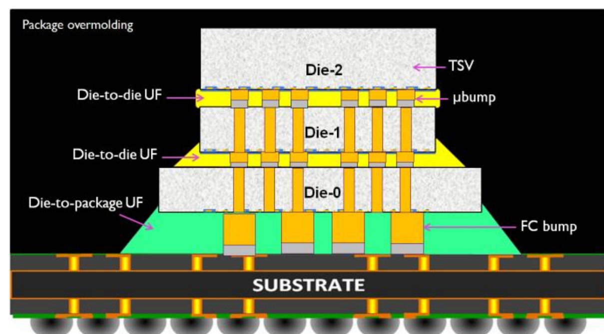


Figure 6: Defects seen in case of assemblies using NUF material.

Underfill in die-to-die assembly

The main goal for 3D-IC integration is to increase device density by using high density vertical connections: 3D-stacking. The processes needed for 3D integration start from the formation of through-silicon-vias (TSVs) and move along wafer thinning, backside processing, micro-bumping and stacking including underfill [6, 7]. The underfill used in this die-to-die assembly enhances the bonding between dies and prevents entrapment of moisture and other contaminants. In 3D-stacking the main challenges for underfill are the narrow gaps between dies (~10µm) and fine µbumps pitches (~20µm). The final package in which 3D-stacks will be encapsulated will depend on the final application, and considering that mobile applications are the main driver for 3D integration, BGA package is the typical option (Refer to figure 7).



Downloaded from http://meridian.allenpress.com/ism/article-pdf/2011/1/000008/2343492/ism-2011-ta1-paper2.pdf by guest on 23 November 2022

Figure 7: Typical stack-up in case of BGA package with multi-die stack.

Considering the challenges of die-to-die assembly in 3D integration, the use of capillary underfill is not an immediate choice. This is mainly due to following reasons: a) narrow gap and the fine bump pitch, which will require extremely low viscosity materials and/or process development (e.g. vacuum supported underfill [4]); b) need for dedicated dispensing area, which will limit the possibility of stacking dies with same size.

Better choice is considered to be the use of No Flow UF. In case of NUF, apart the same concerns present for die-to-package assembly (material transparency, dispense timing, UF/filler entrapment, voids, etc.) another issue is related to the volume control required to avoid UF overflows on die backside. The UF overflow can contaminate backside pads. Excess UF can also be thicker than µbumps and prevent die-to-die stacking (Refer to figures 8, 9). Avoiding backside overflow is a fundamental requirement for multi-die stacking where dispense volume control is critical.

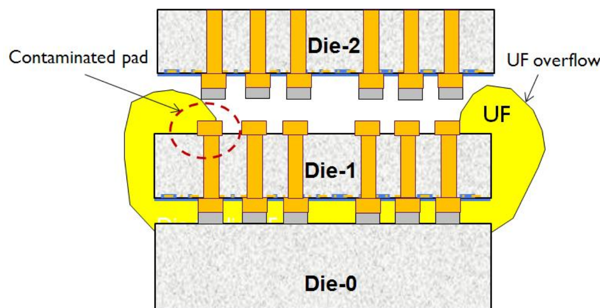


Figure 8: UF flowing to die backside contaminating backside pad/bump

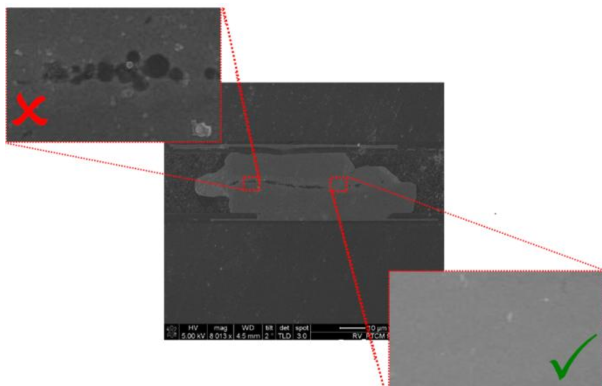


Figure 9: Example of UF filler entrapment between bonded bumps (Top left picture indicates areas with entrapped filler, while the bottom right picture shows area filler-free)

Wafer Applied UF and 3D integration

Local dispensable under fill like the capillary or no flow UF have both a fundamental limit that is related to the timing for dispensing: for both kind of UF the dispense is done locally for each die/stacks with negative effects on throughput. Wafer Applied UF (WAUF) is therefore a valuable candidate to increase UF processing throughput. Wafer applied underfill can be categorized in 2 main categories: spin coatable WAUF (UF is applied on wafer by spin coating) and film WAUF (UF is laminated on wafer, preferably by vacuum lamination). Typical process flows for both materials are depicted in Figure 10.

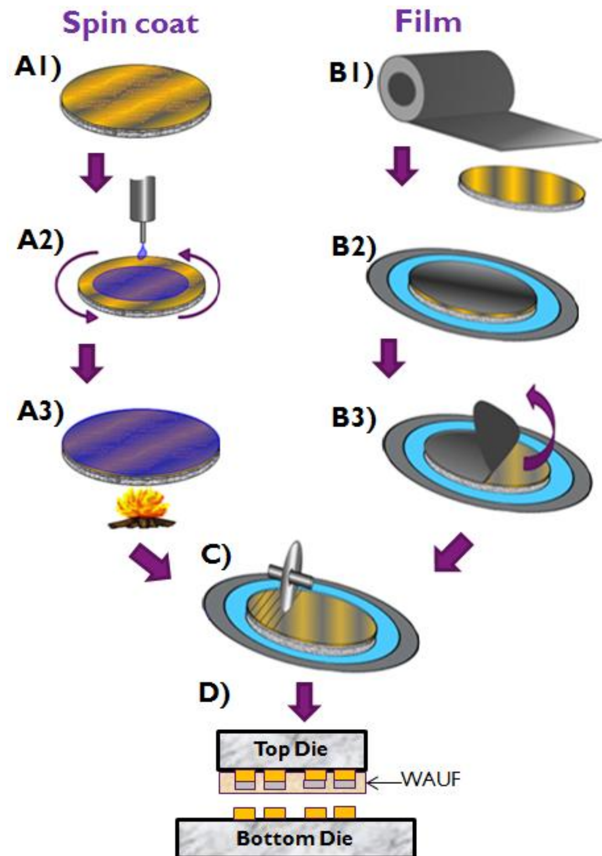


Figure 10: Process flows for spin coat or film Wafer Applied underfill.

Spin coat flow: *A1) Incoming bumped wafer (200mm diameter), A2) Spin coating using manual spinner, A3) B-stage (curing) on hot-plate, C) Dicing of coated wafer, D) Die-to-die assembly.*

Film lamination flow*: B1) Vacuum lamination on bumped wafer, B2) Wafer mounting on dicing frame, B3) removal of UF protective film, C) Dicing of laminated wafer, D) Die-to-die assembly.*

These two categories of materials can be compared in term of material properties (refer to Table 2) but also in term of processing. From a processing point of view, both categories of underfill present advantages and disadvantages. The Table 3 presents an initial comparison between the two categories.

Another way to compare these materials is to identify the possible advantages and disadvantages that they will bring to 3D stacking flow.

To achieve 3D stacking there are three main approaches that are currently pursued: die-to-die (D2D), die-to-wafer (D2W) and wafer-to-wafer (W2W). In this work we have considered only the first two approaches.

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2011/1/000008/2343492/ism-2011-ta1-paper2.pdf by guest on 23 November 2022

The D2D approach has also two alternatives: a) die to package followed by sequential die-to-die stacking (typical approach used by packaging houses) and b) die to die stacking to make ‘die-cube’ followed by die-cube to package stacking (typical approach that could be used by device manufacturer). The D2W approach has also two variations: a) Die to wafer with individual bonding (each die is individually bonded on the landing wafer) and b) die to wafer with collective bonding (dies are firstly placed on the landing wafer and the collectively bonded).

In case of D2D stacking, the WAUF is applied at wafer level prior dicing and stacking (Figure 11).

Spin coat WAUF	
Pros 🙂	**Cons** 🙁
Freshness: material defrosted just before use	Material waste disposal: drainage system required
Easier to use: spinner more common and less expensive than vacuum laminator	Need low viscosity materials for uniform coating and low thickness
	Limited pot life (~days)
	B-stage step is critical
Film WAUF	
Pros 🙂	**Cons** 🙁
Longer pot life (~weeks)	Need vacuum laminator
Not strongly depended on bumps distribution, thanks to vacuum lamination	Need protective film to avoid contamination
No B-stage required: less process steps	
Easy material waste disposal	

Table 3: Comparison for processing Spin coat WAUF vs. Film WAUF

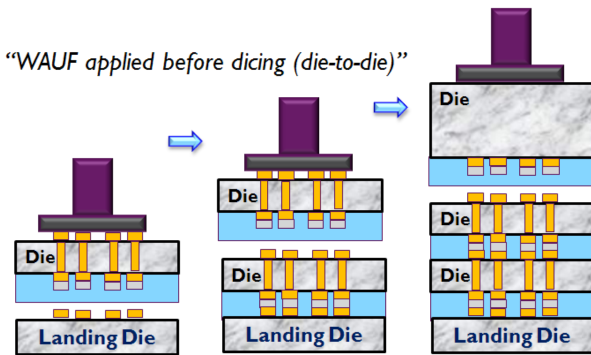


Figure 11: Die-to-die stacking using WAUF

In case of D2W, the options are multiple: WAUF applied before die-to-wafer bonding (after dicing, same as in case of die-to-die), WAUF applied on landing wafer during die-to-wafer bonding, a combination of both options (Figure 12). The option of having the WAUF applied before die-to-wafer offers more advantages in term of process manufacturability: UF coating/lamination can be done in bathes (all wafers processed before dicing), final dicing can be done using the alignments marks of the landing wafers (these marks are less visible in case WAUF is present on the wafer), etc. More complete comparison is offered in Table 4.

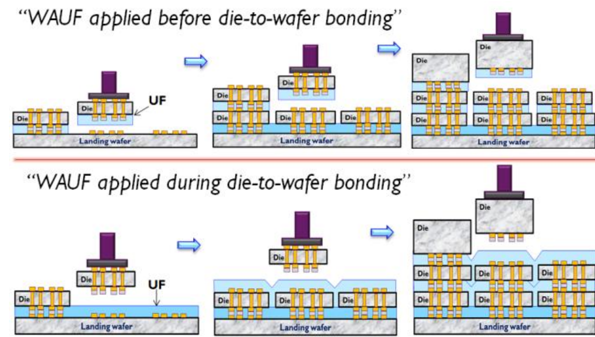


Figure 12: Die-to-Wafer stacking using WAUF

WAUF before D2W stacking	
Pros 🙂	**Cons** 🙁
Wafer can be processed in batches and then go to dicing	Special trays required to carry dies with UF (UF can stack die in the tray)
Spacing between stacks is free from UF material (marks on landing wafer are visible)	Dicing can contaminate UF (particles)
Fits both stacking approaches: D2D and D2W	Lamination of thin wafers can be complex (need of carrier? Or covering when on dicing frame?)
Easier to integrate: wafer is not transferred to other equipments for UF coating/lamination	
WAUF during D2W stacking	
Pros 🙂	**Cons** 🙁
Gap between stacks is filled while stacking: ‘free’ wafer reconstruction	Application after die stacking can induce topography between stacks
No particles contamination due to dicing	UF material will cover marks on landing wafer
	UF covering after die stacks will require transfer to new equipment: coater/laminator

Table 4: Comparison for processing WAUF before D2W bonding or during D2W bonding

Evaluation procedure for Wafer Applied UF

WAUF materials have been evaluated in three subsequent phases: *pre-screening* and material selection; *requirements assessment; assembly test.*

In the pre-screening phase, before starting any evaluation, the material vendors have been requested to propose materials that could full-fill (at least partially) the following requirements:

- Able to reach uniform material thickness (<30um, 10µm target)
- Able to fill gap for small bump pitch (≤40um)
- High transparency to allow die alignment based on control marks
- Good tackiness at T ambient

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2011/1/000008/2343492/ism-2011-ta1-paper2.pdf by guest on 23 November 2022

- Low curing temperature
- Process capability up to 250°C

After this initial screening, mainly based on material datasheets and supplier's suggestions/experience, the selected materials have been moved to requirements assessment phase.

Requirements assessment and test vehicles

The scope of this phase was to assess if the materials proposed by suppliers were in line with the requirements. The wafers used in this phase were initially dummy silicon wafers (200mm wafer diameter) and later device wafers.

The device wafers consist in two different test vehicles that are later stacked on top of each other using die-to-die assembly.

The two test vehicles are named: **PTCM** (Packaging Test Chip version M) and **PTCN** (Packaging Test Chip version N). They are processed using 130nm CMOS technology with 2 metal layers BEOL (Back End Of Line). The µbumps are placed in a periphery array configuration with 40µm bump pitch.

The stack PTCM+PTCN (Refer to Figure 13) is electrically characterized by measuring the resistance of the Daisy Chains (DC) structures. These structures are accessible on the bottom die (larger than top die).

The design parameters of test vehicles are summarized in following Table 5.

	PTCM (Top die)	PTCN (Bottom die)
Die size	5.1mm x 5.1mm	8.1mm x 8.1mm
µBump pitch	40µm	40µm
µbump diameter	25µm	25µm
µbump metallurgy	Cu/Sn	Cu
µbump thickness	5µm/3.5µm	5µm
Number of µbumps	480	480

Table 5: Design parameters of used test vehicles

The target requirements for this phase were the following:

1) Thickness range achievable
2) Thickness uniformity
3) Absence of defects
4) Transparency
5) Process easiness
6) Rework-ability

Thickness range achievable

Material is coated on 200mm wafers and then thickness is measured. Target is to get a minimum thickness in the range of 10um and exclude materials that are far from this value (>30um).

Thickness uniformity

After coating, the material uniformity is measured by Ellipsometer. Target is to get material uniformly distributed on the wafer with a max TTV (Total Thickness Variation) below 2µm

Absence of defects

Coated material should not present any visible defects: voids, cracks, residues, etc.

Transparency

Coated material should be transparent to allow bonding alignment based on pattern recognition (alignment marks).

Process easiness

The judgment is based on the complexity to prepare the material, repeatability of the process, storage requirement, shelf life, frost-defrost, tool cleaning, drainage.

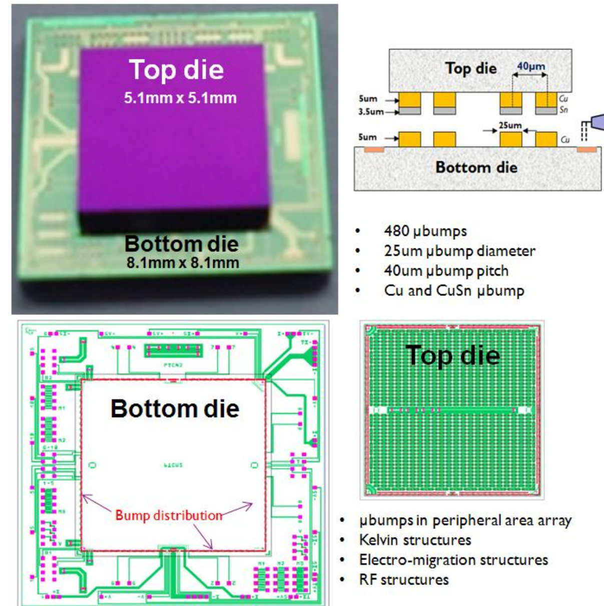


Figure 13: Lay-out and characteristics of used test vehicle

Requirements assessment results

A total of nine suppliers were contacted in this phase and only three of them were able to provide materials (other materials have been proposed later, but the evaluation results are not reported in this paper).

The selected suppliers provided a total of five materials, named respectively: A1, A2, A3 (spin coatable types), and B1, B5 (film types).

The first spin coatable (A1) material was immediately discarded after spin coating exercise. The material A2 could be slightly optimized but still not in line with requirements, even the highest rotation speed (3000rpm) could not grant uniform material coating on the wafers (Refer to Figure 14).

More promising where the remaining 3 materials (the spin coatable (A3) and the 2 films (B1, B2)).

The material A3 was initially processed to identify the best spinning conditions on full thickness (725µm) wafers. These conditions were then confirmed/assessed in the following cases: a) Full thickness blanket wafer; b) Thinned (25µm) blanket wafer on carrier; c) Full thickness top-die bumped wafers.

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2011/1/000008/2343492/isom-2011-ta1-paper2.pdf by guest on 23 November 2022

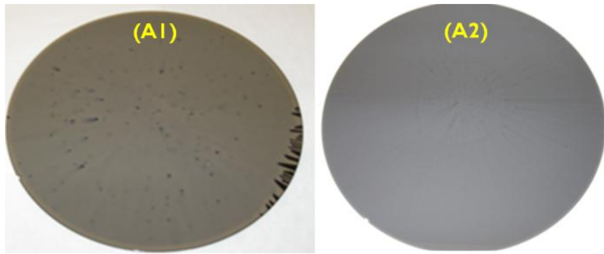


Figure 14: Aspect of materials A1 and A2 after spin coating at 3000rpm.

The results of this evaluation are showed in Table 6 and Figure 15, and they are well in line with most important requirements: 15µm thickness (+/-2µm), high transparency and absence of defects.

Spinning Speed *rpm*	Wafer type	Ellipsometer (avg) *[µm]*	Δ (Max-min) *[µm]*
2500	Blanket full thickness	16.49	0.14
2500	Blanket thinned on carrier	16.41	0.27
3000	Blanket full thickness	13.72	0.28
3000	Bumped full thickness	15.42	1.3

Table 6: Thickness measurements with WAUF material A3

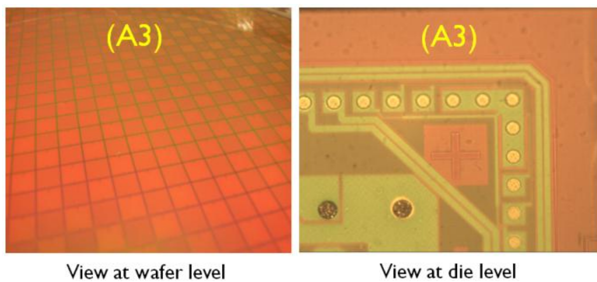


Figure 15: Aspect of material A3 after spin coating on top-die bumped wafer and dicing (die level)

While all the process steps for the spin coatable materials have been performed at IMEC facilities, the two film materials have been laminated at supplier site. This was due to the requirement for a vacuum lamination system that is not at available at IMEC.

The two film materials where laminated also in this case on the top-die wafers.

The thickness measurements showed good alignment with the requirements (15µm +/-2µm) but the transparency of the materials was inferior to the case of material A3; we also observed more particles where than in case of A3 material (Figure 16).

The transparency of the material is in general related to the filler content (percentage and size) and the base chemistry; these properties are reported in Table 7 for all evaluated materials.

Regarding the higher number of particles observed on the film types, this is maybe due to the tackiness of the materials: film materials were tackier than the spin coatable, therefore trapping more particles during dicing.

Material	A1	A2	A3	B1	B2
Base chemistry	Epoxy	Epoxy	Epoxy	Hybrid	Epoxy
Filler %	50/60	40/50	20/30	20	40
Filler size	µm (10µm max)	µm (5µm max)	nm (~50nm)	nm (~50nm)	nm + µm
Flux agent	Yes	Yes	Yes	Yes	Yes
Optical clarity	Translucent	Translucent	Transparent	Transparent	Transparent/Translucent

Table 6: Material properties in term of filler content and optical clarity

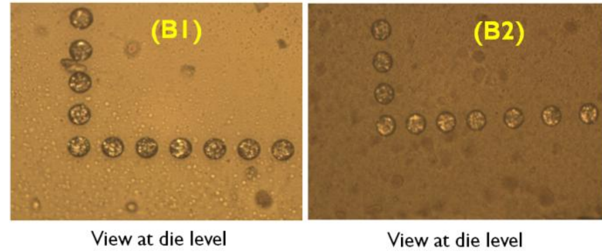


Figure 16: Aspect of material B1 and B2 after spin lamination on top-die bumped wafers and dicing (die level)

Even if materials B1 and B2 were both opaque and not allowing alignment marks recognition, bumps were anyway visible so that the assembly could be performed by using manual bump-to-bump alignment.

Assembly test

After the previous phase, the materials A3, B1 and B2 have been moved that the next phase that consists in the assembly test.

The assembly flow used to stack the two test vehicles is showed in Figure 10.

The three materials have been assessed based on the following criteria:

1) Dicing
2) Tackiness
3) Electrical test
4) SAM
5) X-SEM

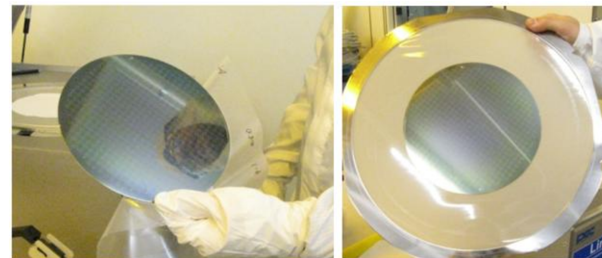


Figure 17: Removal of protective film from wafer with WAUF and placement of dicing tape.

Dicing

After removal of the protective film, the wafers covered with WAUF material are placed on a dicing frame and later diced. The requirements are:

- No smearing due to dicing
- No delamination
- No particles trapped in the material during dicing
- No material degradation due to blades/water interaction

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2011/1/000008/2343492/isom-2011-ta1-paper2.pdf by guest on 23 November 2022

Tackiness

The dies are placed on a landing wafer heated at 80°C with lowest pressure. The requirements are:

- Dies stay in place (no movement) after wafer population -> ~1hour
- Dies stay in place (no movement) if wafer is transferred from a tool to another one (2 meters distance)

Electrical test

After dicing, the dies with WAUF are bonded on the bottom dies using die-to-die assembly process.

The bonding yield is defined by the number of functional daisy chain connections, and it is the main parameter to assess the materials in this phase (Refer also to Figure 13).

XSEM and SAM

After bonding, the stacked dies will be analyzed by SAM (Surface Acusting Scanning) to check eventual material delamination and cross-sectioned to check failures and µbump interconnection.

Assembly test results

The first two criteria for the assembly test (Dicing and Tackiness) have been performed by optical inspection after each step with following results:

- No UF delamination or smearing
- No dirtying of the blade observed
- Some particles trapped in UF (mainly in case of materials B1, B2 (film))
- No deterioration of UF material
- Tackiness test passed by all materials (dies stay in place for at least 2 days)

For what is regarding the electrical test, the stacks have been assembled using different bonding profiles where the following parameters have been considered:

- Simple/Multiple heating profiles
- Higher/Lower bonding pressure
- Shorter/Longer bonding time

For each bonding profile we have assembled 10 stacks. An example of heating profiles is given in Figure 18, while in Table 7 and Table 8 the achieved electrical yield is reported in the cases of all bonding profiles (Pr_1... Pr_10).

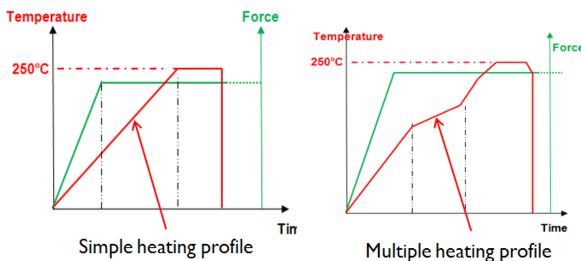


Figure 17: Examples of Simple/Multiple heating profiles used for assembly test

Material	Pr_1	Pr_2	Pr_3	Pr_4	Pr_5	Pr_6	Pr_7	Pr_8	Pr_9	Pr_10
	Simple Heating Profile				Multiple Heating Profile			Multiple Heating Profile		
A2	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO
A3	NO	NO	NO	NO	YES (40%)	YES (40%)	YES (50%)	NO	NO	YES (20%)
B1	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO
B2	NO	NO	NO	NO	YES (50%)	NO	NO	YES (30%)	YES (20%)	NO

Pressure

Table 7: Summary table indicating electrical yield for defined bonding conditions in function of pressure and heating profiles.

YES*=Daisy chains are electrically yielding;* ***NO****= Daisy chains are not electrically yielding*

Bonding Profile	Material / Electrical yield			
	A2	A3	B1	B2
Pr_1	0%	0%	0%	0%
Pr_2	0%	0%	0%	0%
Pr_3	0%	0%	0%	0%
Pr_4	0%	0%	0%	0%
Pr_5	0%	40%	0%	50%
Pr_6	0%	40%	0%	0%
Pr_7	0%	50%	0%	0%
Pr_8	0%	0%	0%	30%
Pr_9	0%	0%	0%	20%
Pr_10	0%	20%	0%	0%

Table 8: Summary table of electrical yield results based on bonding profiles (Note: 10 stacks done for each profile: total 100 stacks)

From Table 7 and Table 8 it appears evident that only 2 materials gave electrical yielding stacks: material A3 (spin coatable) and material B2 (film).

It is also evident that the bonding profile can sensibly affect the final electrical yield, therefore can be further optimized for yield improvement.

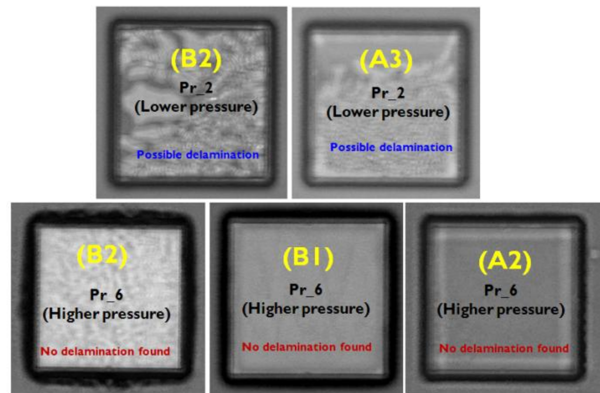


Figure 18: SAM inspections of stacks bonded with different materials and bonding profiles

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2011/1/000008/2343492/isom-2011-ta1-paper2.pdf by guest on 23 November 2022

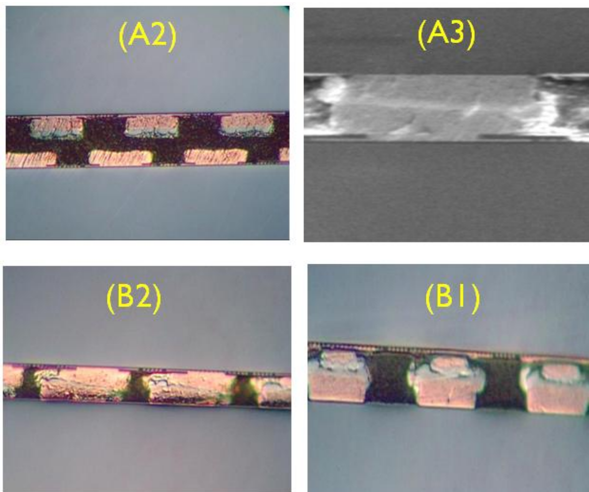


Figure 19: X-section of stacks with different materials

Summarizing the previous assessments, the electrical results, data coming from SAM images (refer to Figure 18) and cross-sections (refer to Figure 19), we have deduced the following indications for justifying the failure/success of the 3D stacks:

- Material A2 is too opaque and thick so dies cannot be properly aligned during bonding and material is not squeezed out to allow connection. It is believed that required improvements to achieve an acceptable yielding percentage (>80%) are out of range for this material: material is not considered for further development.
- Material A3 has the required uniform thickness and it is transparent, these factors allow proper material squeezing and good bonding alignment. It is believed that further material improvements can grant an acceptable yielding percentage (>80%): material is considered for further development.
- Material B1 needs further optimization in the base chemistry to allow good intermetallic formation. Even if opaque, good alignment is achieved but this is not enough to grant an electrical yield. It is believed that improvements will be not enough to grant an acceptable yielding percentage (>80%): material is not considered for further development.
- Material B2 is slightly opaque, but good alignment is achievable. Thickness material is also fine and the base chemistry allows some electrical yielding stacks. It is believed that further material improvements can grant an acceptable yielding percentage (>80%): material is considered for further development.

Conclusions

Wafer Applied UFs offer advantages if compared with standard capillary or local dispensable materials: high process throughput, in line with multi-die stacking processing (also in case of same dies size) and process scalability for small µbump pitch (≤40um).
In this work we have reported about the evaluation of 5 WAUF materials (3 spin coatable and 2 films). The evaluation has been performed on blanket wafers and functional devices with 40µm bump pitch in peripheral area array configuration. Among the evaluated materials, only two have showed good electrical yielding on the selected test vehicles.
The achieved electrical yield can be easily improved by modifying the bonding profiles. The results obtained with this evaluation are very encouraging for future use of WAUF materials in 3D-IC integration flows.
New activities are now ongoing at IMEC to investigate/develop new WAUF materials.

Acknowledgments

This work has been strongly supported by IMEC FPS units, Assembly Integration and Reliability and Modelling teams.

References

[1] Peng Su et al., *The Effects of Underfill on the Reliability of Flip Chip Solder Joints,* Journal of Electronic Materials, Vol. 28, No. 9, 1999

[2] E.W. Washburn, “The Dynamic of Capillary Flow”, Physical Review, Vol. 17, pp 273-283, 192

[3] Jinlin Wang, “Wettability analysis for C4 OLGA Package”, Journal of Surface Mount Technology, Vol 14, Issue 4, 21, 2001.

[4] Katsuyuki Sakuma et al., Development of vacuum underfill technology for a 3D chip stack, Journal of Micromechanics and Microengineering, 21 (2011) 035024

[5] Agarwal R, Zhang W, Limaye P and RuythoorenW2009 *Proc.Electronic Components and Technology Conf.* pp 345–9

[6] A. Jourdain et al., *Integration of TSVs, wafer thinning and backside passivation on full 300mm CMOS wafers for 3D applications*, Proc. IEEE 61st Electronic Components and Technology Conference (ECTC), June 2011

[7] Rajen Chanchani, *3D Integration Technologies – An Overview,* Materials for Advanced Packaging 2009.

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2011/1/000008/2343492/isom-2011-ta1-paper2.pdf by guest on 23 November 2022