Comparison Between Multilayer Ceramic and Organic Package Substrates Based Upon Signal and Power Integrity

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Abstract:

Comparisons between organic and ceramic packaging is a difficult task given the considerable number of differences in material properties and potential tradeoffs between cost, electrical performance, thermal performance, and environmental factors. This paper presents a power and signal integrity comparison between a select set of multilayer organic technologies (HDBU and CPCore) and multilayer ceramic technologies (HTCC and LTCC). The geometry and material property impact on electrical performance for the flip-chip first level interconnect are qualitatively discussed and compared. The broadband frequency performance for the ball grid array (BGA) second-level interconnect to a PWB is simulated and characterized to 40 GHz for a differential pair using full-wave simulation. The impedance of the power distribution network (PDN) for a ceramic package is characterized by measurement to correlate with full-wave simulation to then subsequently compare with an organic substrate PDN.

Introduction

For many applications, the material selection process can be a difficult task when based upon trade-offs between cost, environmental, thermal, mechanical, and electrical requirements. Studies have been done in the past to compare organics and ceramics based on the cost, design and reliability and concluded that the material's solutions are widely varied and strongly dependent on the specifics of each application [1]. However, in almost any comparison between ceramic and organic technologies it is most often the case that ceramic solutions cannot be competitive based on cost alone [2]. In those cases where performance requirements make cost a secondary consideration, the technical parameters in the design trade-off space take on a larger role on the selection between various package substrate technologies. Organic substrate design rules have an inherent advantage in power integrity comparisons to ceramics [3,4], however, there are applications where environmental requirements (e.g. harsh environments) dominate the design trade-off space and require an existing organic technology solution to be converted to a ceramic technology solution. In these cases it becomes necessary to understand the performance trades between the previously existing organic solution and a potential ceramic solution.

In this paper, key features of the flip-chip assembly process are discussed in the context of electrical performance considerations. The flip-chip process is the most common first level interconnect for many high-speed and mixed signal products. As speeds increase the details of this interconnect will also increase in significance. The ball grid array is a common second level interconnect for high-density high-speed packages. This interconnect is characterized and compared in the frequency domain by considering the electrical performance of a differential pair constructed for two organic technologies and two ceramic technologies. Finally, a comparison of a power distribution network for an organic package and a corresponding ceramic package solution is discussed using the target impedance as a figure of merit [5].

First Level Interconnect Discussion

The first level interconnect for many mixed signal devices, ASICs, and processors is a flip chip process. Much has been written about the reliability of this joint and these mechanical concerns can and do effect the electrical performance. In the most basic terms, the underfill material used to couple and keep joints sound have some dielectric properties, which also more tightly couples the electrical signals. Secondly, between the ceramic and organic packages, the manufacturing processes are so different, the different design rules will again affect the electrical concerns. For a quick look at some design rules, Table 1 illustrates some differences as compared to Si technology, which in the end drives these packaging roadmaps.

Table 1: Some material properties and design guides based on different packaging

	Units	Alumina	HiTCE	Build-up	CPCore	Si
Via Pitch	um	150	176	120	175	120
Line/Space	um	50 / 50	60 / 60	12 / 13	25 / 25	.04 / .04
CTE	ppm / C	6	12	15	6 - 12	3.2
Modulus	Gpa	250	75	30	30	165
Conductor		W	Cu+glass	Cu	Cu	n/a

From Table 1, we can also see the organic build-up technologies have kept pace with the Si geometries the best with regard to fine pitch I/O and tight line / space dimensions. From this pitch data, it is clear that as the signal vias that come from the package, through the underfill, to the Si surface, this dimension remains the same. At the same time, the materials of the package, underfill, and Si clearly have different dielectric properties, so the impedance mismatch consequences are different for each material choice. Figure 1 is an example in the organic technology.

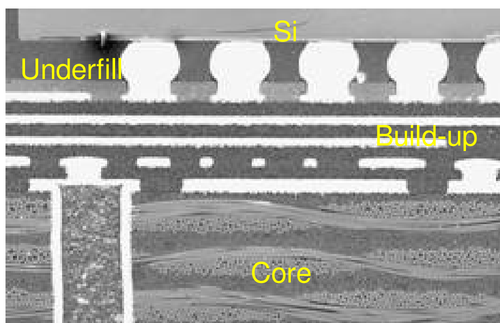

Figure 1 A cross section of an organic package showing the pitch of the die and the matching package structure.

Based on these technologies and limitations, the industry depends on temperature cycling testing to stress these joints to ensure reliability. Given the different nature of the base materials, this testing will cause strain in the joints. Figure 2 is a tested ceramic joint.

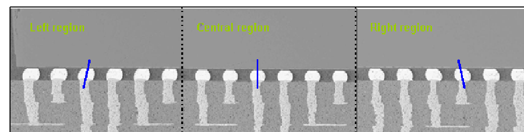

Figure 2 Sections of a flip chip die after TCT excursions on HITCE. Notice the slanting of the left and right C4 bumps where strain can be seen through the temperature difference compared to the center balls (see blue line).

Although the strain in the outer areas can be seen, because the contact is not broken and this is considered a life test, this is an acceptable tested condition. Also, in this image, the via structure can be repeated throughout the package, so impedance can be designed throughout the thickness. This is slightly different from the build-up technology also demonstrated in Figure 3.

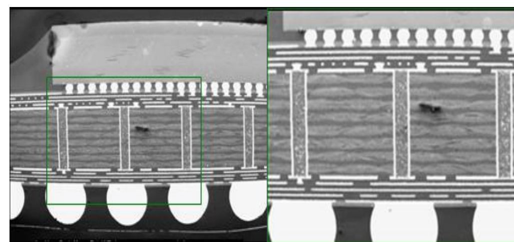

Figure 3 An overall cross-section of a build-up package and a magnified area showing the core vias and fiber layers. This sample has not gone through TCT.

Therefore, given the materials and processing of either ceramic or organic packaging, table 2 below can qualitatively look at the mechanical and electrical consequences of the packaging.

Table 2: Qualitative advantages and disadvantages of generalized packaging materials

Compared w/ Si	Alumina	HiTCE	Build-up	CPCore
CTE	+	0	-	+
Via Pitch	0	0	+	-
Routing	0	0	+	-
Impedance	+	+	0	0

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Signal Integrity Comparisons For Differential Pairs

In this section we discuss and compare the signal integrity performance of 4 package substrate technologies: two organic package technologies and two ceramic technologies. The figure of merit for the signal integrity comparison is the insertion and return loss for an 88 ohm differential pair transitioning from the substrate on to a ball grid array (BGA) and then onto a differential pair on an FR4 PWB board. The 88-ohm value is chosen to match the HDBU differential pair. We use the full-wave EM simulation tool HFSS to obtain the S-parameter data from 0 to 40 GHz.

Table 3 lists the electrical properties of the material technologies used in the modeling of the differential pairs in 4 technologies discussed in this section. High Density Build Up (HDBU) is a laminate technology having a Core (ε_r=4.8, tanδ=0.019 @1GHz) sandwiched between Build Up layers (ε_r=3.2, tanδ=0.0248 @1GHz, Rs_{Cu}=3m Ω/□). CPCore technology (ε_r=4.2, tanδ=0.0061 @3.3GHz, Rs_{Cu}=3m Ω/□) is a second organic material for consideration. This technology replaces the spiral via structures typically found in HDBU, as shown in Figure 4, with stacked vias. This stacking of vias has an important consequence in the performance of the transition of the differential pair from the substrate to the PWB as we shall illustrate.

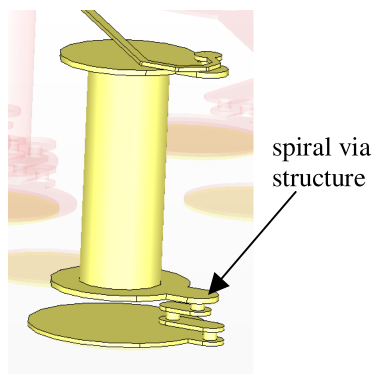


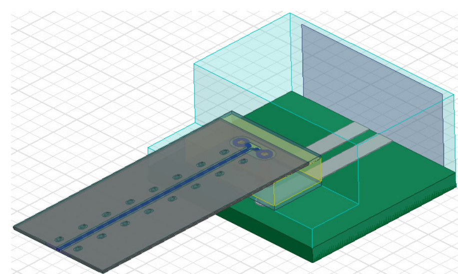
Figure 4 HDBU plated through hole connected to spiral via structure.

The two ceramic technologies considered were HITCE™ (ε_r=5.3, tanδ=0.001, Rs_{Cu}=3m Ω/□), a Low Temperature Cofired Ceramic (LTCC) , and alumina (ε_r=8.8, tanδ=0.0011, Rs_W=10m Ω/□), a High Temperature Cofired Ceramic (HTCC). Both ceramic technologies support stacking of vias.

Table 3: Electrical properties of 4 materials

	HDBU BuildUp	HDBU Core	CPCore	HITCE	HTCC	FR4
ε_r	3.2	4.8	4.2	5.3	8.8	4.2
tan δ	0.0248	0.019	0.0061	0.001	0.0011	0.02
Rs	3 mΩ/sq	3 mΩ/sq	3 mΩ/sq	3 mΩ/sq	10 mΩ/sq	0.6 mΩ/sq

Figure 5a shows a single differential pair model in HDBU. The 88Ω differential pair interconnect begins in a stripline topology with coplanar power plane that is not connected to the top and bottom return paths, also power planes. Figure 5b shows the HDBU stackup: The stripline transitions to spiral vias then to plated thru holes (PLTs) in the Core section. The PLTs are connected to spiral vias in the bottom build up section (3 layers) then to the BGAs. The BGA transitions to a 100 Ω microstrip differential pair on FR4 (ε_r=4.2, tanδ=0.02 @5GHz).



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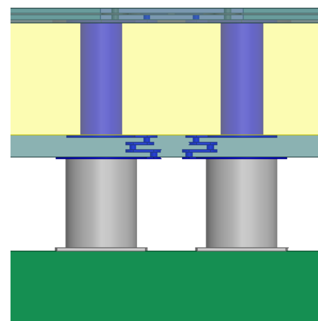

(b

Figure 5 a) High Density Build Up Differential Pair, b) HDBU Stackup -- Stripline to Via to Plated Thru Hole.

Because each material technology has different material properties and manufacturing design rules, it is not easy to compare this HDBU structure to an exact structure in a different material technology. However, we proceed by constraining certain dimensions to achieve electrical characteristics commensurate with the HDBU substrate. For example we use the 88 ohm differential mode impedance as our baseline and

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derive appropriate dimensions in other material technologies to provide the same impedance. In this fashion we can make some generalizations as to performance and density comparisons. In Table 4 we compare the trace width dimensions and substrate thicknesses necessary and available for the construction of the 88-ohm differential pairs for the CPCore and ceramic technologies to match that of the HDBU structure. The associated substrate thickness necessary is determined by the minimum trace width and spacing available for each material technology.

Table 4 Stripline width and substrate thickness dimensions for Zdiff= 88 ohm

	HDBU	CPCore	HITCE	HTCC
stripline width	1.2mil	1.6mil	2.4mil	4mil
stripline spacing	2mil	3.7mil	4.3mil	9.5mil
conductor thickness	0.6mil	0.4mil	0.4mil	0.4mil
stripline substrate thickness	3.3mil	4.1mil	8mil	24mil

For the transition from the differential pair to the BGA (and subsequently the differential pair on the PWB), we again use the HDBU electrical characteristic to determine the structure and dimension in the other material technologies. The characteristic impedance of the plated through holes in the HDBU is nearly 100 ohms. We target this value in the other material technologies. Table 5 lists the BGA pitch and via diameter and pitch dimensions targeting a 100 ohm impedance for the via structure in all 4 material technologies. The values denoted for via diameter and via pitch using HDBU are for the plated thru holes. The smaller 2mil spiral via structures are used to transition between the stripline to the plated thru holes, and then from the plated thru holes to the BGA pads.

Table 5: Comparison of differential Via transition for 4 material technologies.

	HDBU	CPCore	HITCE	HTCC
BGA Pitch	1mm	0.8mm	0.8mm	1mm
Via Diameter	12mil*	4mil	2mil	5mil
Via Pitch	40mil*	11.2mil	8.3mil	30mil
Zdiff	99.3Ω	107.2Ω	110.3Ω	98.8Ω

Figure 6a shows the 88-ohm differential pair model for the CPCore technology. Figure 6b shows the via transitions to the BGAs, which are attached to a microstrip differential pair constructed to be similar to the PWB used for the HDBU substrate. As can be seen, this technology does not require the construction of spiral vias to interconnect signals between layers. This means, of course, that there are fewer discontinuities along the signal path, and subsequently, as we will show by simulation, will exhibit superior return loss performance at higher frequencies. However, based on the selection of minimum via dimensions, and the targeted 100-ohm differential impedance, design rule constraints and material properties, the required BGA pitch was 0.8mm, rather than the 1mm BGA pitch used in the benchmark HDBU. The distance from the bottom ground plane of the stripline section to the BGA pads was kept as close to same distance as is in the HDBU model. With the exception of BGA ball pitch., the BGA pad diameter, BGA ball diameter and PCB differential pair load are kept the same as the HDBU model.

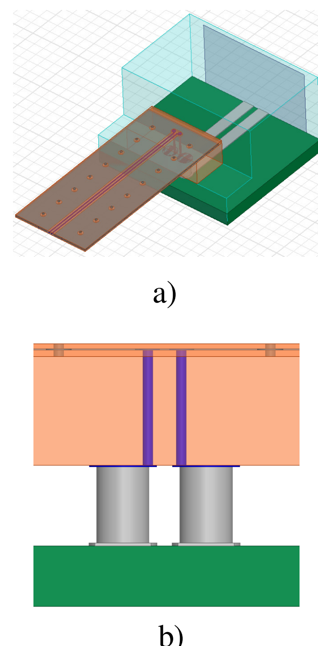

Figure 6 a) CPCore Differential Pair to BGA to PCB, b) CPCore Differential Stripline to Via to BGA to Microstrip

Figure 7a shows the model for the 88-ohm differential pair model in the LTCC technology. This technology has a lower dielectric constant than the HTCC ceramic considered in this section and allows 2 mil via diameters. Figure 7b shows the cross section of the model. In an effort to compare to the LTCC routing density to organic substrates, the line and via dimensions were selected to be the minimum size available. Also, as in the CPCore model, the distance from the bottom stripline ground to the BGA pads is kept close to the nominal distance in the HDBU model. The BGA and PCB load are kept the same as the two

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organic models. The 2mil differential vias necessitated a 0.8mm ball pitch to allow straight routing to the ball pads and keep the differential impedance as close to 100Ω, the nominal impedance set by the HDBU plated thru holes.

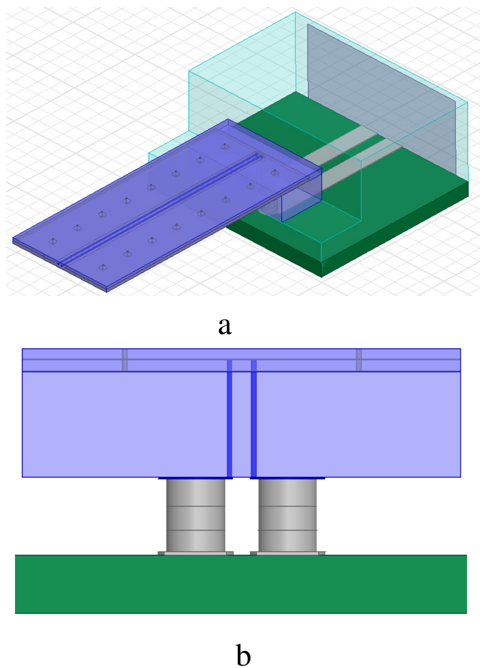

Figure 7 a) LTCC Differential Stripline to PCB model b) LTCC Differential Stripline to Via to BGA to Microstrip

Figure 8 shows the 88-ohm differential pair for the HTCC process for alumina. HTCC results in thicker tapes, larger via diameters and line widths, thus comparable density is harder to achieve for applications with high I\Os. Again, the distance from the bottom stripline ground to the BGA pads is kept close to the nominal distance in the HDBU model. Figure 8 shows the cross section of the HTCC model. The BGA and PCB load are kept the same as the two organic models with the exception being that the ball pitch is 1mm, which is the same as in the HDBU model. The larger design constraints allowed for a 99Ω differential via section using a 1mm ball pitch.

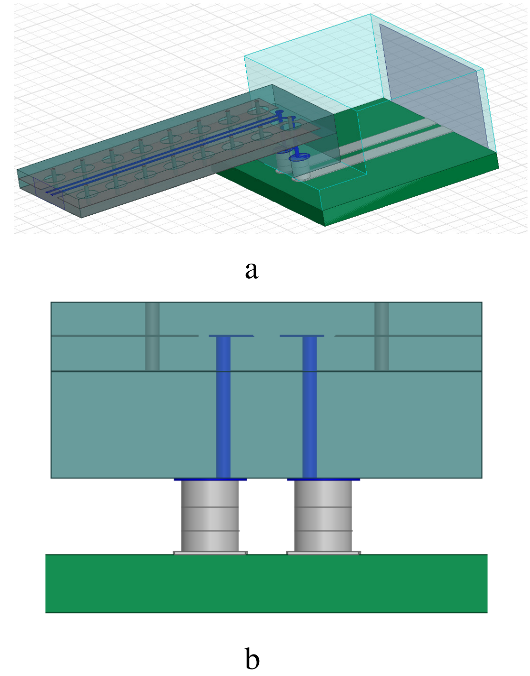

Figure 8 a) HTCC Differential Stripline to PCB, b) HTCC Differential Stripline to Via to BGA to Microstrip

Simulation Results for the Differential Pairs

The differential pair models were simulated using the full wave solver, Ansys HFSS, for the frequency band of 0.5-40 GHz. Both conductor and dielectric loss were included in the simulation. Figure 9 shows the differential mode return loss for the 4 models described in the previous section.

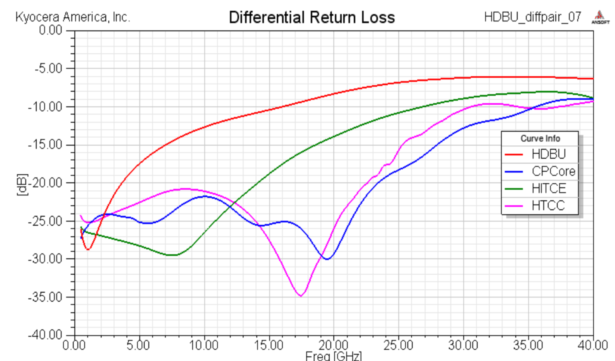

Figure 9 Differential Return Loss of the Organic, LTCC, and HTCC substrates.

The substrate technologies with stacked vias for differential via transition have much lower return loss than the nominal HDBU case. While the HDBU process allows for 2mil vias in the build up sections, the differential pair must be routed through the core section using plated thru holes with a 12mil diameter. In addition, the vias in the

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build up layers are spiral constructions as described previously. These discontinuities lead to a degradation in the high frequency performance of the HDBU substrate. The return loss performance of the HTCC and CPCore technologies are comparable, while the performance of the LTCC is not as good. It is conceivable that the return loss can be improved with better impedance matching in the differential via section. Since no optimization beyond the best practice control of impedance along the interconnect was implemented, further improvement is possible for the LTCC case. For example, the LTCC differential pair has the largest via impedance discontinuity, because selecting 2 mil diameter vias requires a tighter 0.8mm BGA pitch and larger via pitch to connect to the BGA pads. A 4mil via would have required a 13.5mil pitch: spaced enough to land on the BGA pads and have a Zdiff=99Ω, rather than the Zdiff=110.3Ω using 2mil vias.

Figure 10 shows the show the differential mode insertion loss for the LTCC, HTCC, and organic substrate technologies. The LTCC substrate, which had a higher return loss than the CPCore and HTCC substrates shows the lowest insertion loss across the .0 to 40 GHz bandwidth. This could be in part due to its high conductor conductivity and low dielectric loss tangent, but results also suggests that the other substrate transition designs are leaking energy along the interconnect path, which could be manifested in higher cross-coupling between traces.

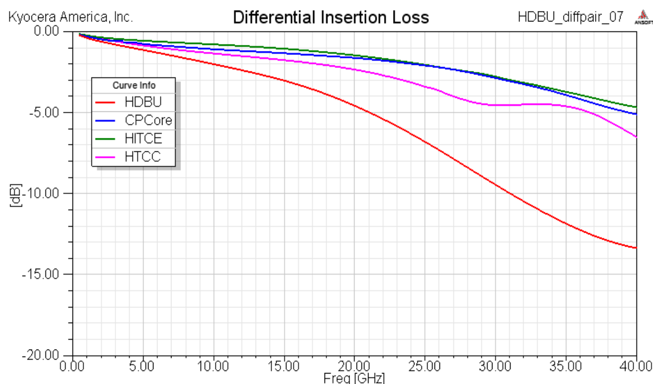

Figure 10 Differential Insertion Loss of the Organic, LTCC, and HTCC substrates.

Figure 11 is a model of two side-by-side differential pairs. This model is constructed for each material technology to study and compare the potential crosstalk between two adjacent differential pairs.

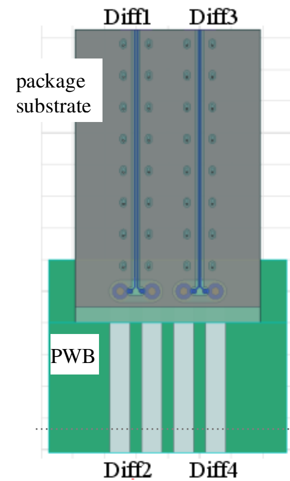

Figure 11 Two parallel differential pairs.

Figure 12 shows the near-end cross-coupling for the substrate side for each material technology. Up to about 15 GHz, the coupling is about –30 dB for each technology. Given the number of design variables it is not clear if any technology has advantage in this aspect.

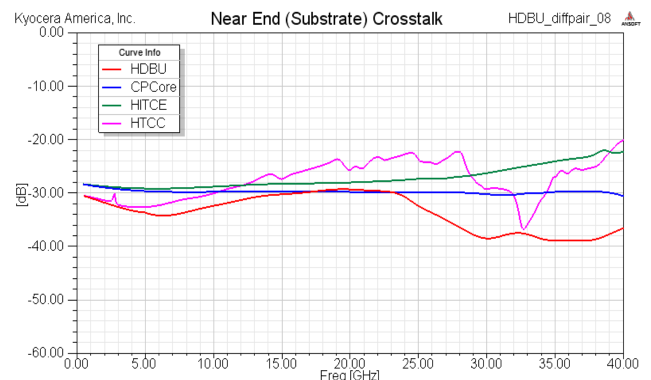

Figure 12 Near End cross-coupling for two parallel differential pairs

Figure 13 shows the Far End coupling for each substrate. The cross-coupling is highest for the HTCC and the HDBU. Both the LTCC and the CPCore demonstrate lower cross-coupling up least up to 35 GHz than HTCC and HDBU.

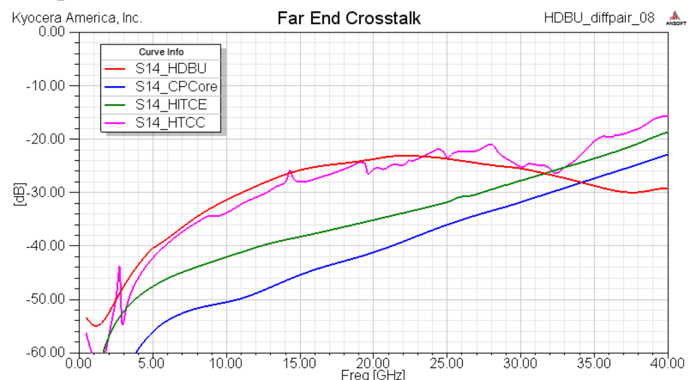

Figure 13 Far End cross-coupling for two parallel differential pairs

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Power Integrity Comparison for Core Power and High Speed Power

To compare the power integrity of an organic package to that of a ceramic package is a difficult task given the considerable number of material, design, and costs variables. As a reasonable constraint on the design universe, we compare an organic package with a die similar in complexity and functionality to its next generation version given an environmental specification requiring that the device be packaged in a ceramic multilayer package. Figure 14 shows a "stretched" view of the organic substrate and the ceramic substrate. The packages are for a single relatively large die and the ceramic version requires package decoupling capacitors whereas the organic version did not. The substrates are BGA with an I/O provided by a 39 x 39 array sans the four corner balls for a total of 1517 balls available for power, ground and signals.

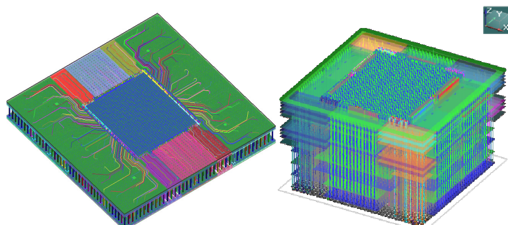

Figure 14 Organic substrate and ceramic substrate

The design guideline on the ceramic package was that it replicate the power distribution network (PDN) performance of the organic package. The criteria chosen to compare the two PDN was the target impedance for each power net as defined in the following equation [5]:

$$Z_{target} = \frac{(PowerSupplyVoltage)X(Allowed\ ripple)}{(Average\ Current)}$$

Table 6 is a side-by-side comparison of the organic substrate and the final design of the ceramic substrate, which, assuming full functionality for each similar die, provides the physical trades and costs made in conversion from the organic to the ceramic package. The package footprint increased somewhat, but this is partly due to the larger die being packaged with the ceramic substrate. Clearly, the largest physical impact is in the required number of layers and overall substrate height, which increased by approximately a factor of two and three, respectively.

Table 6 Ceramic vs. Organic

	Ceramic substrate	Organic substrate
Number of die	1	1
Die size(s)	26 mm x 31mm	19mm x 17mm
Assembly	F/C	F/C
Total Chip I/O	>7000	>10000
VDD I/O	>2500	>4800
VSS I/O	>2800	>4800
Capacitors	Y	N
Substrate Mat'l	A440	HDBU
Substrate I/O	1517	1517
VDD I/O	105	127
VSS I/O	273	316
Substrate 2nd Level Type	LGA	LGA
Assembly	BGA	BGA
Substrate size	1.75in x 1.75in	1.54in x 1.54in
Total dielectric thickness (mil)	120	43.5
Layers	19	10

Core Power Impedance

To compare the PDN of the organic and ceramic substrate electrically we used Sigrity PSI to generate the impedance vs. frequency profiles for select ports on the die pads of the substrate. Given the relatively large die size, the impedance of the PDN is expected to depend significantly on the particular location of the power/ground pins. Figure 15 shows the locations on the dies that were selected as suitably mapping this variation.

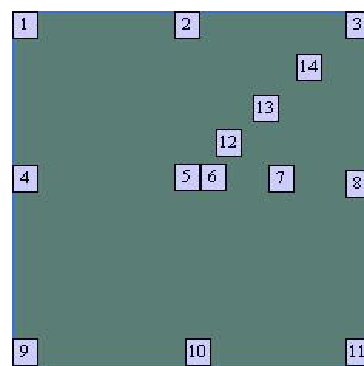

Figure 15 Power/Ground pin pair locations for corresponding organic and ceramic die

Figures 16 and 17 show measurement vs. simulation open circuit impedance profiles for a worst location on the ceramic substrate core power area: corner ground/power pin pair and a center side ground/power pin pair. As can be seen, the correlation between measurement and simulation is excellent. Overlaid on these curves is a corresponding open circuit impedance profile for

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the organic package. At these locations, the ceramic and organic substrates are almost indistinguishable in impedance profile. However for the port located at the center of the die, Port 5 shown in Figure 18, the organic substrate has a significantly lower open circuit impedance profile. This is true in general for any power/ground pin pair inside the periphery of the core area..

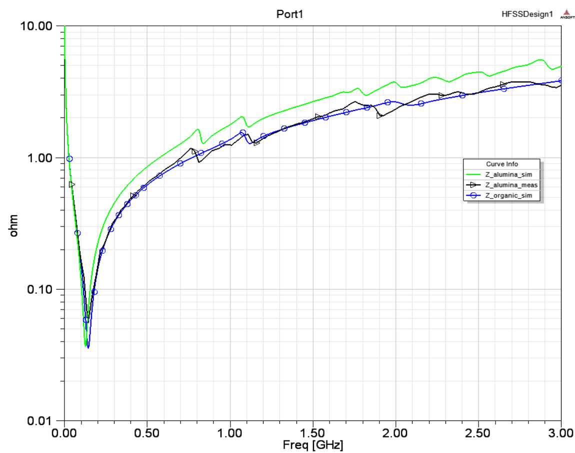

Figure 16 Open circuit impedance simulation and measurement for Port 1

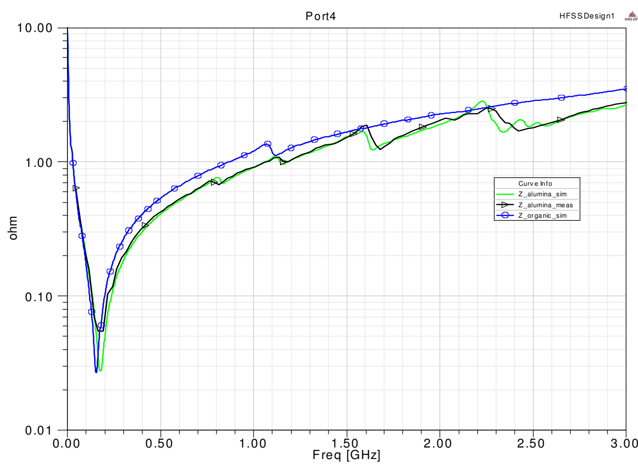

Figure 17 Open circuit impedance simulation and measurement for Port 4

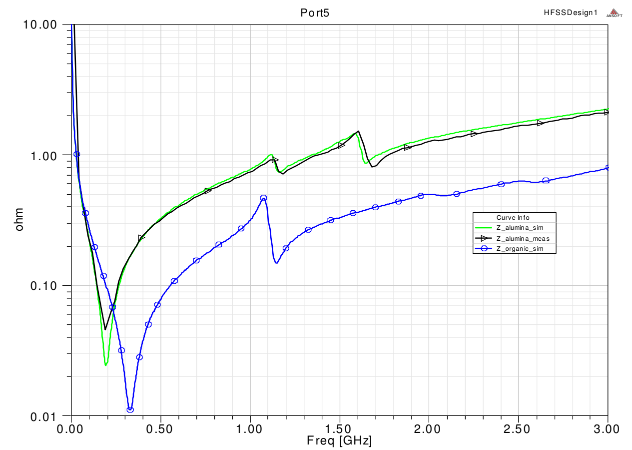

Figure 18 Open circuit impedance simulation and measurement for center Port 5

Of course, the impedance profile of the PDN will depend on many factors including decoupling on the PWB and on-die decoupling. As a benchmarking assumption for a simulation comparison, we provide a perfect voltage to the substrates PWB/substrate interface, however, with no on-chip decoupling. Figure 19 shows the impedance profile for a corner port 3 and the interior port 5. Again, the ceramic and organic impedance profile is very similar at the corners, however again, the interior port at the center of the die displays a very low impedance profile relative to that of the ceramic substrate.

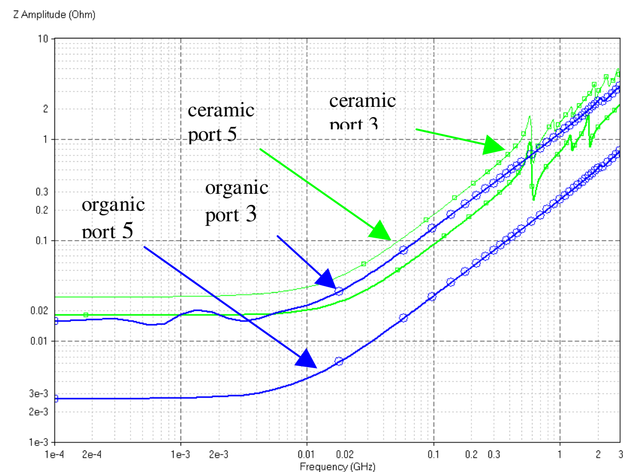

Figure 19 Short circuit impedance simulation for die corner port 3 and center port 5.

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High-speed PDN Impedance

The PDN for the high-speed signals is separated on the package substrate from the core ground for both the ceramic and organic packages. Both packages have a limited area for the PDN as illustrated in Figure 20. Figure 21 shows an impedance profile for each substrate. The organic package has a resonance at slightly over 2 GHz. The ceramic substrate without decoupling has a resonant peak at around 450 MHz. The ceramic substrate high impedance peak can be reduce by placing decoupling capacitors on the top layer of the ceramic substrate. The impact of this resonance is of course application specific, however from appropriate selection of decoupling capacitor values and location, the resonant peak can be reduced and shifted to about 800 MHz as shown in Figure 21.

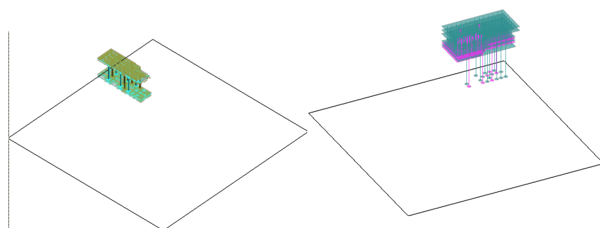

Figure 20 a) Organic HSD PDN, b) Alumina HSD PDN

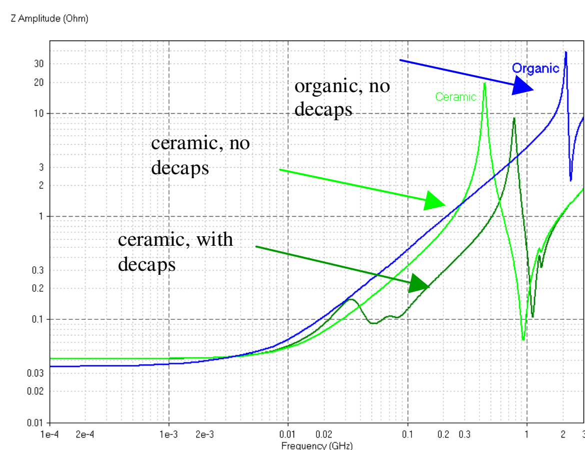

Figure 21 Impedance vs. Frequency for high-speed PDN

Summary and Conclusions

This paper utilizes signal and power integrity metrics to compare organic to ceramic package technologies. The signal integrity impact of the first level flip-chip interconnect is qualitatively discussed. The underfill process necessary to increase the mechanical reliability of the first level interconnect is possibly not sufficiently charcterized for higher speed signals. The signal integrity of the differential signals transitioning to a BGA is strongly design dependent, however the spiral via strutures of some organic technologies limits the performance for very high speed signals. The impedance of power networks for an organic and ceramic package is compared. The organic package has overall lower impedance profile and higher frequency resonances, however, the impedance profile of the ceramic package can be reduced with decoupling capacitors.

References:

[1] Sigliano, Richard E., “Ceramic Vs. Plastics: Part I, Is Perception Reality?” MEPTEC Report Quarter One 2003 pp.26-28

[2]Bechtold, F., "A comprehensive overview on today's ceramic substrate technologies," *Microelectronics and Packaging Conference, 2009. EMPC 2009. European* , vol., no., pp.1-12, 15-18 June 2009.

[3]Haitian Hu, Nanju Na, Baez, F., Lafontant, G., "Design-performance aspects of Glass Ceramic in comparison to Alumina Ceramic and organic FCPBGA packages for high link densities of high speed SerDes," *Electrical Performance of Electronic Packaging, 2008 IEEE-EPEP* , vol., no., pp.243-246, 27-29 Oct. 2008.

[4]Budell, T., Audet, J., Kent, D., Libous, J., O'Connor, D., Rosser, S., Tremble, E., "Comparison of multilayer organic and ceramic package simultaneous switching noise measurements using a 0.16 µm CMOS test chip," *Electronic Components and Technology Conference, 2001. Proceedings, 51st* , vol., no., pp.1087-1094, 2001.

[5] Smith, L.D., Anderson, R.E., Forehand, D.W.; Pelc, T.J.; Roy, T. , "Power distribution system design methodology and capacitor selection for modern CMOS technology," *Advanced Packaging, IEEE Transactions on* , vol.22, no.3, pp.284-291, Aug 1999.

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