Mix of analog and digital circuitry analysis in a noisy environment

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Abstract

High transient current from a digital circuitry, fast di/dt, within an analog circuitry co-existence is very demanding. Analysis of the diverse potential noise coupling path, and suggested solutions, is required to guarantee proper functionality and performances of both circuitries. Our noise analysis includes the die, package and PCB power supply and decoupling strategy. This analysis takes into consideration the efficiency of the power delivery Network, PDN, at a Macro and Micro environment.

The analysis is using 3D Simulations techniques based on causal model. With this novel technique, we investigate the potential noise induction through the ground path and isolation. For the conclusion, we suggest a method that improve the PI analysis over a mix signal IC..

Keywords: Digital, Analog, Ground coupling, Mix signal

Introduction

For the longest time, designers taught that more, and diversified, decoupling the better. It was true to some extent with lower core clock switching frequencies and slower *di/dt*.

Now, the performances of the silicon reach limits that requires further capabilities to isolates the cells that might exceeds the limits of IR drops (Dynamic & Static) due to higher current peaks in a smaller time constraint window which increase the noise ripple given by V=Ldi/dt

We will emphasis the requirements to include the die, substrate and PCB together to understand better the effects of the PDN [5] system.

In this paper, we will also emphasize on the common ground coupling noise between the digital core, VDD, and analog circuitry, DVDD.

Common Ground Noise coupling within the IC

Common ground noise coupling is another mechanism to inject noise into sensitive circuitry such as the Analog Macro. There are in theory, several ways to connect the grounds and isolating the analog to the digital macros. It raises a question on how the die, package and PCB designers should define the overall specifications to minimize ripple and meet specifications in both digital and analog macro.

Figure 1 demonstrate the potential destructive path of the return current from the digital circuitry, close to 100's of Amps, towards the analog circuitry.

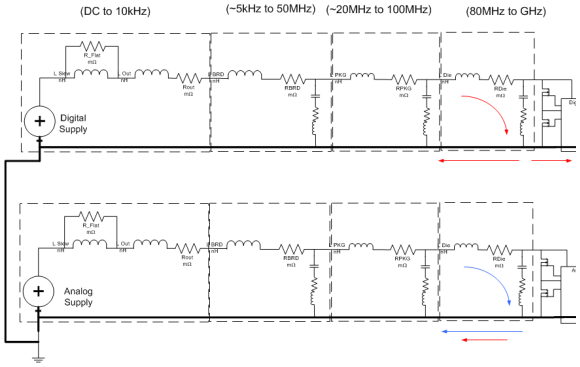


Fig. 1 PDN and nominal decoupling caps range in bracket

For the frequency domain potential ground coupling, the package model was included in the simulations with PCB, with corresponding stackup and power plane structures and PCB/Package decoupling caps and voltage regulator module, VRM, with bulk capacitors.

The noise source could be from the ground bounce or via ground coupling from one Supply domain to another. As well, it was proven that PCB decoupling [6] caps located on the same side as the silicon was lowering the impedance and inductance, but not practical due to space and thermal and high speed constraints. Our analysis demonstrate that with the digital supplies located in the middle of the package was detrimental and increased inductance via the blocking effects of the surrounding BGA pads.

For the PCB, we used state of the art decoupling strategy which includes Buried Capacitance, BC, from the PCB and via in pad to minimize total Inductance L.

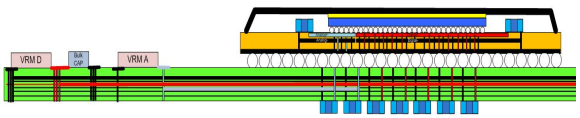


Fig. 2 PCB, Package and die representation

Time Domain procedure and analysis

For VDD analysis, we used Apache Redhawk to extract chip power model for PDN noise and impedance system analysis. An Encounter layout of GDSII/DEF file is imported to the tool, which include the gate level netlist and layout information. Other design files are also imported for the signal net parasitic loading information in the SPEF format; the timing file from a static timing analysis tool about the frequency of operation cells, input slew and transition timing window.

In order to do an accurate analysis based on switching activity of the logic, the switching information, in a standard format of VCD (Value Change Dump), is generated.

In order to do a preliminary analyze and estimation during the early design cycle, the analysis is based on RTL.

Gate level VCD is applied later for sign-off analyze with accurate power consumption, peak current and DVD (Dynamic Voltage Drop). Meanwhile static IR drop for average voltage drop is simulated to do sanity check before DVD.

The measured dynamic and static IR drop is 114mV and 8mV respectively for a VCD based analyze within a few blocks.

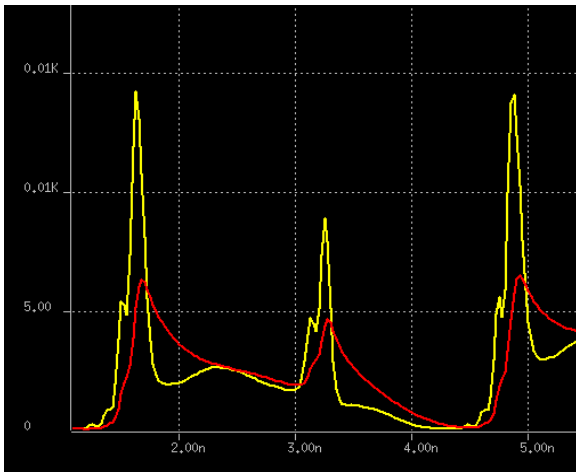


Fig 3 Current waveform at die bump

On the next time domain results, simulation demonstrates the noise waveform at power/ground for one instance is shown in Figure 4, which has worst voltage drop.

In Figure 4, the VDD ground noise exceeds 50mV where the maximum that the analog macro specified was less than 1mV.

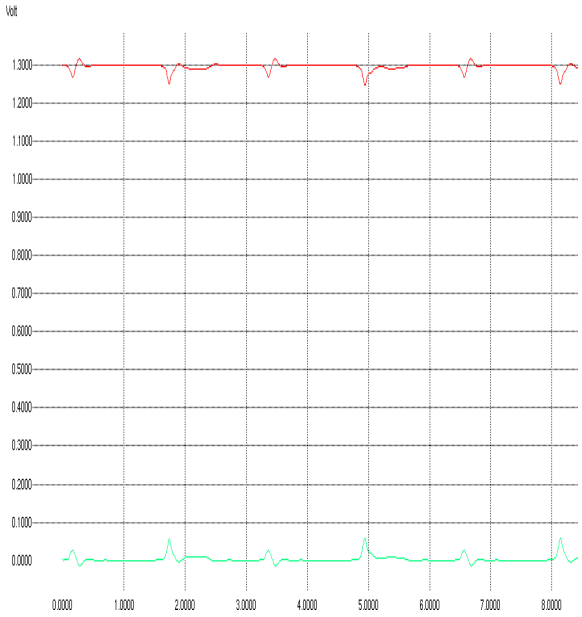


Fig 4 VDD Noise waveform power/ground

Meanwhile, for chip-package-PCB system co-simulation, a CPM (Chip Power Model) model is generated for full chip. It is a multi-port, per bump or groups of bumps, a layout based electrical representation of the chip in an open spice format.

It captures the switching and leakage current together with the parasitic elements present in the chip. This model cap mimics the behavior of the fully detailed chip layout and the devices from DC to multi-GHz range. It is a simplified full chip model, which can speed up the system simulation greatly.

Figure 5 shows CPM current/voltage waveforms read within Synopsys Hspice. We can see the ground noise waveforms of different bump groups of the chip. It is very convenient for ground bounce noise analyze with very high current, and fast, transient in system simulation explained in the next sections.

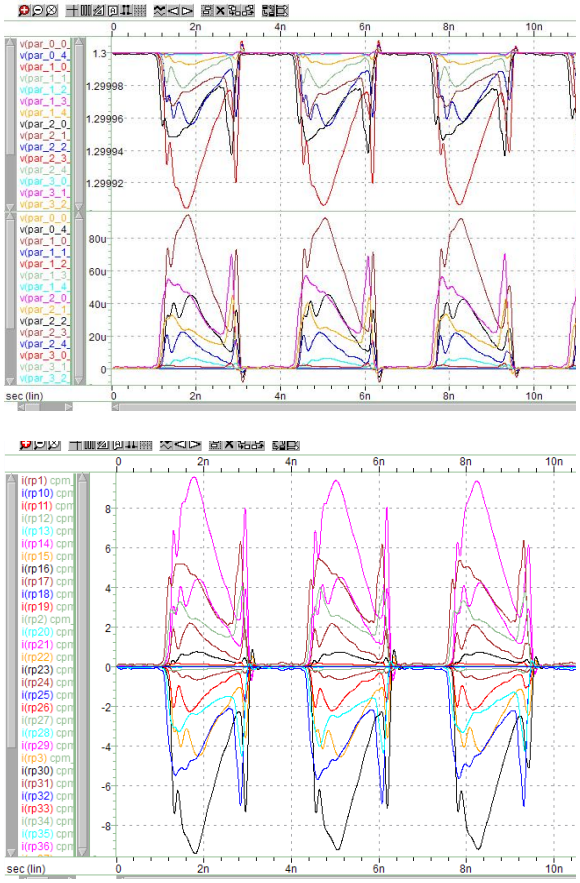


Fig 5 CPM Current and Voltage for different bumps

Frequency Domain Procedure and Analysis

In order to model and simulate the entire PDN, the structure of the package S parameters, spd2, from Figure 6 and PCB structure are inserted in the simulations.

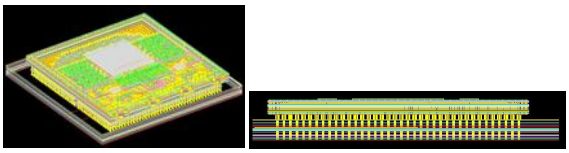
The spd2 file of the package is imported into Sentinel-PSI (fast 3D field solver) for conversion. The PCB file is also imported and converted.

Package and PCB are merged into one structure and connected through the BGA balls.

The package die areas are divided into 22 divisions to form 22 ports.

From Figure 6, the model has a total of 248 ports in total which includes the VDD and DVDD supplies, VDD and DVDD Package Decap, VDD and DVDD PCB Decap, VDD and DVDD PCB parallel ports.

There are some shared ground planes in Package and PCB for VDD and DVDD. In this case, the last metal layer of the package joins the ground from all sources.



a) b)

Fig 6 a) ISO and b) side view of the combined Package and PCB model

The frequency domain results, shown on Figure 7, without the die, demonstrate the ground coupling effects between VDD and DVDD. By applying uniformly a fix current source of 100A to VDD, the ground noise coupled into DVDD_GND is 0.204mV.

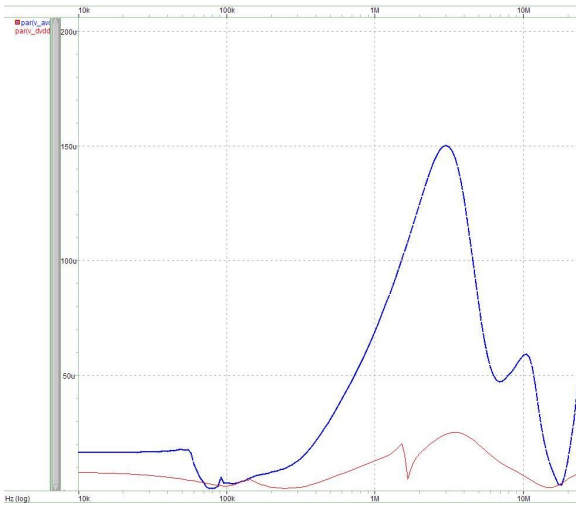


Fig 7 DVDD die pad coupling versus frequency

Conclusion

This paper demonstrates that on the frequency domain analysis, the ground return isolation is meeting the noise requirements for the analog supplies isolation by connecting the ground together on the last layer of the package. The results are applicable to a real system behavior, but every design has their own requirements and particular constraints where those results may not be applicable.

Next step

The next steps will be to progress on the time domain analysis. As well, measurements and correlations will be done and analyze against our simulations published.

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