

# Highly Selective Wet Silicon Etch Chemistry and Process for Advanced Semiconductor Packaging

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## Abstract

A wet silicon etch chemistry and a process using the chemistry as a simple and cost-effective alternative to the polish/plasma etch silicon thinning process are presented in this paper. The new etch chemistry improves the Si etch rate over traditional etchants such as tetramethylammonium hydroxide (TMAH). The chemistry has very high silicon etch selectivity (ratio of Si etch rate to another film etch rate) over SiO<sub>2</sub> and over copper films, with etch selectivity greater than 8000:1 and 2500:1 respectively. Chemical compatibility with typical packaging materials such as polybenzoxazole (PBO) and polyimide (PI) are also discussed. Additionally, real production TSV wafers have been successfully processed on an advanced single wafer etch tool using the chemistry. High uniformity and smooth surface finishing have been achieved.

## Key words

Si Etch, Selectivity, Wet process, Copper, polybenzoxazole (PBO), and polyimide (PI)

## I. Introduction

In recent years, increased demands for thinner, lower power consumption, lower cost, and higher performance semiconductors for consumer electronic products have driven the semiconductor industry's innovation. At the front end, feature size has been continually shrinking following Moore's Law, to achieve today's 14 nanometer technology [1]. At the back end, 3D and wafer level packaging have been the focus, giving rise to More than Moore [1-4]. 3D Through-Silicon Via (TSV) and Fan Out Wafer Level Packaging (FOWLP) are two key technologies enabling the next generation of higher performance and smaller devices by reducing interconnect length to increase device speeds, and increasing interconnect density to reduce the package form-factor [1-4]. In via-first and via-middle TSV integration flows, Si wafers must be thinned from the backside to reveal the Cu plug for the wafer to make contact with another wafer or chips. Typically, this thinning

is performed by grinding the backside of the wafer, polishing to remove the grind marks and subsurface damage to eliminate the stress in the wafer, and then etching by plasma or wet chemical process to reveal the Cu vias as shown in Fig. 1.

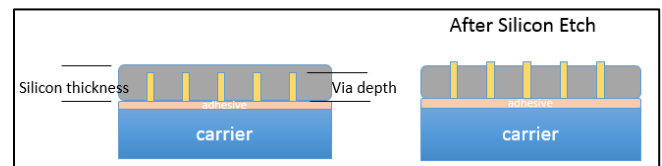


Fig. 1. Schematic of TSV reveal structure before and after silicon etch

A similar silicon thinning/etch process is also involved in various FOWLP process integration flows as shown in Fig. 2.

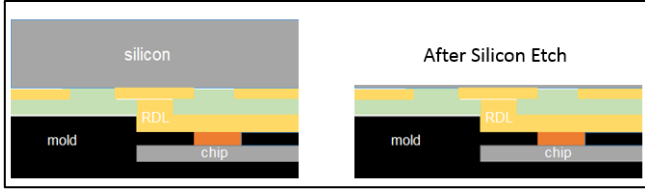


Fig. 2. Schematic of FOWLP structure before and after silicon etch

In many of these silicon etch processes, dry etch can be used. There are several advantages of dry etch, including fast etch rate, typically  $\sim 5\mu\text{m}/\text{min}$ . silicon removal. Also, it is a mature technology with excellent control. However, dry etch equipment and most dry etch gases are more expensive. In addition, the dry etch process generates etch residuals that redeposit on the wafer surfaces and the etch chambers. These residuals need to be removed by a wet clean process which increases complexity and cost. Alternatively, with a wet etch process, equipment and chemicals are typically less expensive. Wet etch also simplifies the process by eliminating the post clean step. However, the shortcoming of traditional wet etch is its slower etch rate. The key to a successful wet process is the selection of the combined optimal chemistry and equipment. The right chemistry matches the dry etch rate as closely as possible, while delivering better selectivity and surface finish, such as roughness and defects. In addition to the chemistry, the equipment must provide tight process control for etch depth and uniformity. It must be configurable to meet customer throughput requirements. This paper introduces a new chemistry and its application results when used in an advanced single wafer wet etch tool with integrated thickness feedback.

## II. Experiments

### Coupon Tests

Si coupons of about 20x20 mm made from P-type single-crystal Si wafers with [100] orientation were used in all lab tests. A coupon was premeasured for surface area, pretreated with 2% HF for 1 minute to remove native oxide, and preweighed. The coupon was then submerged in an etch solution in a PTFE beaker for a specified time. Temperature was controlled at 78-83°C for all tests unless otherwise indicated. After the specified etch period, the coupon was removed from the etchant and immediately rinsed with DI water. The coupon was then dried using  $\text{N}_2$ , and weighed to calculate the total amount of silicon etched and the etch rate.

Copper (Cu) coupons, thermal Si oxide (Tox) coupons, and other coupons were premeasured using a KLA-Tencor, 4 probe resistivity tool or bench-top J. A. Woollam ellipsometry instrument. The coupons were etched without any pretreatments. After etching, post-film thicknesses were determined by the same respective instruments used for the

premeasurement. The etch removal and etch rate were determined using the pre- and post-thickness difference.

### Wafer Tests

Ground Si wafers, Si test wafers, wafers with sputtered Cu films, and Tox wafers (all 300mm) were etched on a Veeco PSP 3300ML single wafer etch tool equipped with Profile Match Technology™ and integrated thickness control to verify the beaker coupon test results. Process and equipment parameters were developed for optimum etch rate, surface roughness, and surface defects. Si etch amount was determined using a Sentronics Metrology StraDex f2-300 IR sensor by measuring the pre- and post-etch wafer thickness. Cu and Tox etch rates were determined by measuring pre- and post-etch film thickness using a Signatone QuadMap 4 Point Probe resistivity measurement system and a Filmetrics F60 Ellipsometer. Surface roughness was measured using a KLA P16 surface profilometer, and reviewed with a Veeco Icon AFM in some cases. Surface conditions and defects were reviewed using a Hitachi S-3700N SEM. Finally, production TSV wafers were processed under the optimized chemical and equipment conditions determined from the test wafers.

## III. Results and Discussions

### Beaker Coupon Test Results

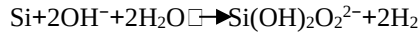
Si wet etch can be realized using two different kinds of chemistry: the HF-based acid etch and strong base etch. HF-based etch needs an oxidizer to convert the Si surface layer to  $\text{SiO}_2$ , and then the HF etches away the  $\text{SiO}_2$ . This method has a relatively high etch rate, but it etches  $\text{SiO}_2$ , which is not acceptable in the TSV reveal etch process. Also, the HF-based process is not compatible where metal film is exposed. Since the targeted applications in this study are TSV reveal and advanced wafer level package process, such as FOWLP, strong base chemistry was selected.

For a successful wet process, a high silicon etch rate is essential because it determines the throughput, one of the key cost factors for the process. Table I shows examples of lab screening etch results of different formulations on coupons.

Table I. Beaker etch rate screening results for coupons

| Formulation   | Base | Additive | Si ER (nm/min) | $\text{SiO}_2$ ER (nm/min) |
|---------------|------|----------|----------------|----------------------------|
| 1             | KOH  | No       | 363            | 0.1                        |
| 2             | TMAH | No       | 800            | 0.1                        |
| 3             | B1   | No       | 646            | 0.1                        |
| 4             | B2   | No       | 450            | 0.1                        |
| 5             | B3   | No       | 142            | 0.1                        |
| 6             | B1   | A1       | 340            | 0.1                        |
| 7             | B1   | A2       | 549            | 0.1                        |
| 8 (SMC6-42-1) | B1   | A3       | 940            | 0.11                       |
| 9             | TMAH | A3       | 900            | NA                         |

All data were from beaker tests in the SACHEM R&D lab and have been updated with new test results over our previously published results [5]. Because  $[\text{OH}^-]$  is considered the dominant active silicon etch specie in strong base solutions through the following general silicon etch reaction [6-11],  $[\text{OH}^-]$  concentrations were kept the same for all these formulations at 1M.



Several organic bases were screened and compared with the commonly used KOH and TMAH. KOH was tested only for reference purposes, with no further study conducted with it due to the industry concern for K metal contamination. As shown in Table I, the organic base B1 matched closely with TMAH in terms of etch rate, and performed significantly better than the other non-TMAH organic bases. Although TMAH is widely used in the semiconductor industry, an alternative should be used whenever possible due to TMAH toxicity concerns. For this reason, more studies were focused on formulations with B1. Detailed discussion of our new chemistry toxicity and comparison with TMAH toxicity were presented in our previous publication [5].

Different additives were studied to increase the Si etch rate even further. The results indicate that additive A3 has a significant synergistic effect with organic base B1 to increase the Si etch rate. All base formulation tests showed an excellent Si/SiO<sub>2</sub> etch selectivity of greater than 3600:1. It should be noted that the combination of the B1 and Additive 3 (SMC6-42-1) significantly increased the Si etch rate, but still maintained about the same low SiO<sub>2</sub> etch rate resulting in a selectivity of over 9000:1. This formulation was selected to test on the 3300 etch tool to confirm its performance.

The etch rate for the B1/A3 (SMC6-42-1) is high compared with the other base formulations. However, the etch rate is still lower than plasma etching. To provide good throughput, a two-step process [12] is utilized, which begins with a fast isotropic acid etch of the silicon for surface smoothing and thickness profile control, followed by the highly selective base etchant.

#### Wafer Test on an Advanced Single Wafer Etch Tool

Etch results using SMC6-42-1 collected on a 3300 etch tool are presented in Table II.

Table II. Etch rates obtained on 300mm wafers in a Veeco PSP single wafer etch tool

| Etchant   | Ground Wafer ER (nm/min) | Tox ER (nm/min) | Cu ER (nm/min) | OH Conc. (M) | Temp (°C) |
|-----------|--------------------------|-----------------|----------------|--------------|-----------|
| SMC6-42-1 | 800                      | 0.12            | 20             | 1            | 95        |
| TMAH      | 260                      | 0.1             | NA             | 2.8          | 80        |
| KOH       | 600                      | 0.1             | NA             | 4.2          | 72        |

TMAH and KOH historical data obtained on the same tool are listed for reference only. Although direct comparison cannot be made due to the difference between test conditions, one can still see the viability of the SMC6-42-1, with an etch rate close to 1μm per minute and 8000:1 selectivity over SiO<sub>2</sub>. Comparing the coupon data in Table I and wafer data in Table II, SMC6-42-1 performance was confirmed. The lower etch rate is believed to be due to the temperature decrease when the solution spreads on the large surface of a 300mm wafer. The Cu etch rate is significant at about 20nm/min. from the 3300ML single wafer etch tool. In the TSV reveal process, the Cu vias are encapsulated in SiO<sub>2</sub>. Therefore, the Cu etch rate may not be that critical. For other applications where Cu is exposed, this high etch rate is not acceptable. This issue is addressed in the Cu Etch Protection section of this paper.

Surface roughness is an important parameter in TSV reveal etch and other Si etch processes because it affects the characteristics and performance of subsequent film depositions. Surface roughness was evaluated during the wafer test phase. As shown in Fig. 3, the incoming ground wafers had rough surfaces with grinding marks of 40nm in height.

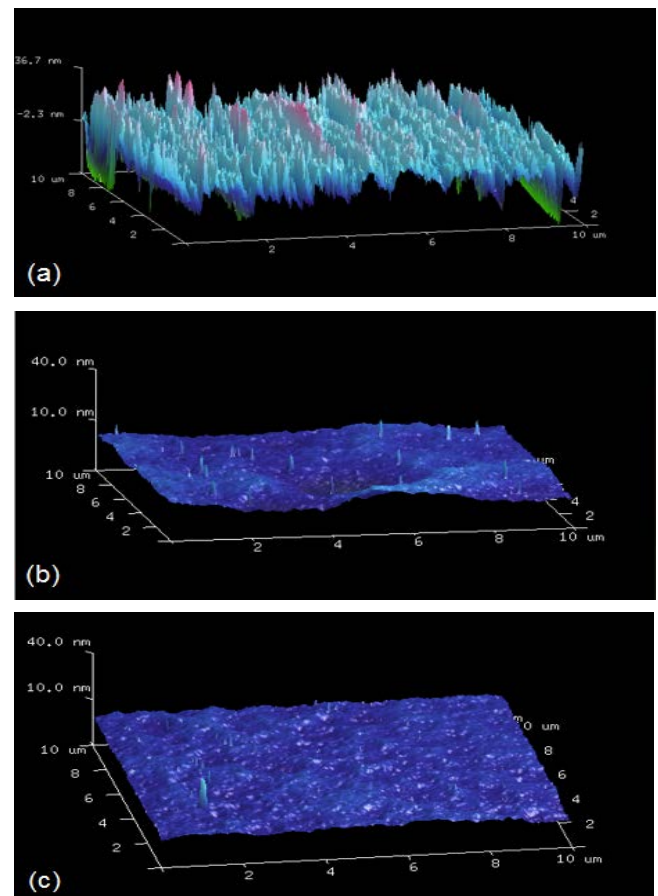


Fig. 3. AFM images of wafer surface after (a) grind, (b) 10μm HF/HNO<sub>3</sub> etch, (c) SMC6-42-1 etch

To smooth the surface, the first chemical etch is performed using HF/HNO<sub>3</sub>-based chemistry that etches silicon isotropically at a very fast rate, up to 10µm/min., depending on the amount of silicon to be removed. The HF-based chemical cannot be used to reveal the TSV because it would etch the SiO<sub>2</sub> liner and the Cu in the vias, or metallic elements or compounds in the FOWLP. The isotropic etch is used to quickly smooth out the peaks and valleys created during the grinding process. Next, the highly selective base etchant is used to reveal the vias or the Cu plugs. The surface remains smooth after the final etch, as shown in the AFM images, with roughness about 1.5nm. This result is very encouraging because it provides the possibility of eliminating the CMP process following the grinding step in the current TSV wafer Si thinning process flow. More data was collected to compare incoming wafers with grinding and CMP steps to wafers etched directly from the grinding step. The results demonstrated that the CMP step can be skipped in favor of the wet etch, the chemistry, the Veeco PSP 3300ML tool, and process optimization. Data and experimental details were published in our previous paper [5].

Actual TSV wafers have been successfully etched with a unique process that uses SMC6-42-1 as the final etchant on the Veeco PSP 3300ML tool to reveal the Cu vias. Fig. 4 shows the revealed vias on one of the real TSV wafers.

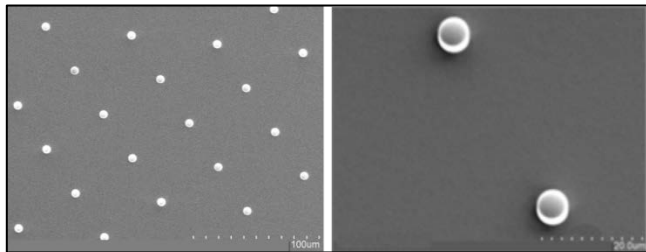


Fig. 4. SEM images showing the revealed vias and defect-free surfaces

As shown in the images, the vias are cleanly revealed with no etch pits or pyramids or other surface defects. Details about the process and equipment were discussed in our previous publications [5, 6] and will not be repeated here.

### Cu Etch Protection

As discussed early in this paper, the Cu etch rate was found to be 20nm/min. on the Veeco PSP etch tool. This high Cu etch rate would be problematic in some applications, such as FOWLP, where Si removal is required and Cu may be exposed. Since we already had a chemistry that works for Si removal for the TSV reveal process, a Cu etch inhibitor seemed the logical approach to add to the Si etch chemistry SMC6-42-1. Table III lists the screening

results for Cu inhibitors.

Table III. Cu etch inhibitor screening results

| Formulation No. | Main Formulation | Inhibitor | Si ER (nm/min) | Cu ER (nm/min) | Si/Cu Selec. |
|-----------------|------------------|-----------|----------------|----------------|--------------|
| 8               | SMC6-42-1        | None      | 600            | 22.5           | 27           |
| 9               | SMC6-42-1        | BTA       | 510            | 4.9            | 103          |
| 10              | SMC6-42-1        | I1        | 420            | 6.2            | 68           |
| 11              | SMC6-42-1        | I2        | 530            | 0.2            | 2524         |
| 12              | SMC6-42-1        | I3        | 140            | 0.4            | 333          |

Since Benzotriazole (BTA) is commonly used in the semiconductor industry as a Cu etch or corrosion inhibitor, it was included in the screening tests. The results with BTA were not very promising for Si etch chemistry. Significant Cu etch of 4.9nm/min. was measured when selectivity was maximized. Further increasing the BTA concentration reduced the Cu etch rate but lowered the Si etch rate, resulting in poor etch selectivity. Inhibitor 2 (I2), on the other hand, showed excellent performance, with a Cu etch rate of only 0.2nm/min. and almost no effect on the Si etch rate. A silicon-to-copper etch selectivity of over 2500:1 was achieved in coupon testing and confirmed on the Veeco PSP etch tool. Surface finish was also examined using SEM. Fig. 5 shows Cu wafer surfaces etched with SMC6-42-1, and with SMC6-42-1 with various Cu etch inhibitors. It is clear that without any inhibitor, the Cu surface is etched with a significant number of pits (Fig. 5 b). With the addition of BTA, Cu etch is reduced, but shallow pits are still observed (Fig. 5 d). Using I2, however, the finished surface has no etch pits (Fig. 5 c) and looks the same as the incoming Cu wafer surface (Fig 5. a).

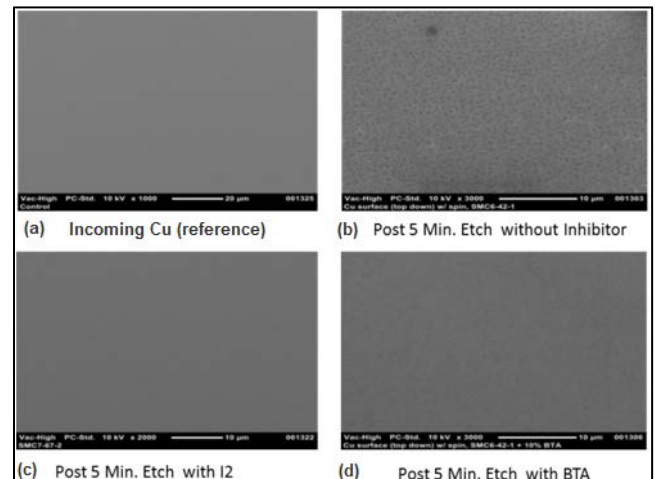


Fig. 5. SEM images of Cu film surfaces etched under different conditions

To help understand the Cu etch/protection behaviors observed, an XPS study was conducted and is presented in Fig. 6.

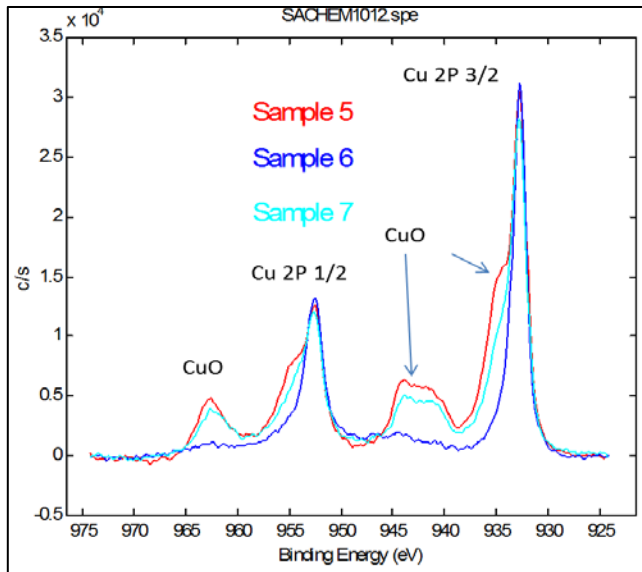


Fig. 6. Cu 2P XPS spectra for Cu films: Sample 5, incoming (no etch); Sample 6, post 5 min. etch with SMC6-42-1 and I2 inhibitor; Sample 7, post 5 min. etch with SMC6-42-1 and inhibitor I2, and extra IPA rinse

XPS results in Fig. 6 show that CuO, and possibly Cu<sub>2</sub>O, were detected on the incoming Cu film surface (Sample 5) presumably due to oxidation in air.

After etching the incoming Cu film for five minutes with I2 as Cu etch inhibitor (Sample 6), copper oxide was clearly removed from the surface. It should be noted that the XPS analyses were carried out more than 48 hours after etching in a third party's lab. This result indicates that there was no CuO regrowth, even after more than 48 hours, if the inhibitor is left on the surface. The small etch removal of Cu measured with Inhibitor 2 addition was probably due to the removal of the native CuO layer on top of the Cu film. On the other hand, if no Cu etch inhibitors or a weaker inhibitor is used, the Cu etch more likely proceeds as many micro galvanic cells between different Cu grains. These etches following the galvanic mechanism generated the etch pits because of preferential etch at the anodes. When the inhibitor was removed from the surface by rinsing with IPA, CuO regrew and is clearly detected by the XPS spectrum (Sample 7). More study with controlled times between etching and XPS measurement should reveal more about the kinetics of oxide regrowth.

PBO and PI are common materials used in the semiconductor packaging industry. It is important for the new chemistry to be compatible with them since they may be exposed during the FOWLP application. PBO and PI coupons were etched in our beaker and the results are

presented in Table IV.

Table IV. PBO and PI etch rates

| Film     | Pre-Thickness (nm) | Removal (nm) | Etch Time (min) | Etch Rate (nm/min) | % of pre-thickness |
|----------|--------------------|--------------|-----------------|--------------------|--------------------|
| PBO      | 7083               | -24.8        | 5               | -5.6               | 0.40               |
| PI       | 5115               | -6.4         | 5               | -4.2               | 0.41               |
| Si [100] | NA                 | 10600        | 20              | 530                | NA                 |

As the data indicate, SMC6-42-1 with Cu inhibitor does not etch PBO and PI. In fact, a small negative etch removal of PBO and PI were measured. We believe the negative removal was an artifact from our ellipsometry measurement. The incoming films were at about 5-7  $\mu\text{m}$  and at the upper range of film thickness the instrument can accurately measure.

Fig. 7 shows microscope images of PBO and PI film surfaces as received and after a five minute etch with SMC6-42-1 with inhibitor.

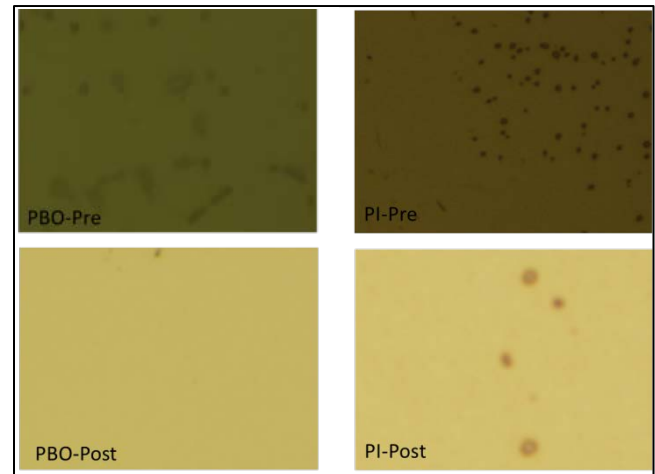


Fig. 7. Microscope images of PBO and PI films. Top as received, bottom after etch using SMC6-42-1 with I2 for five minutes

As shown, both PBO and PI incoming films are dirty with particles and liquid marks. After five minutes of etching, the surfaces are much cleaner. No obvious etch-related defects, such as pits or texture were found. Color changes for the pre- and post-film surfaces were purely from light changes on the microscope.

## IV. Conclusion

We have developed a Si etch chemistry SMC6-42-1 that etches Si at 0.6-0.8  $\mu\text{m}/\text{min}$ . and has a very high selectivity over SiO<sub>2</sub> of 8000:1. The chemistry has been demonstrated with real TSV production wafers on a Veeco PSP 3300ML single wafer etch tool. The wet process using this new chemistry in a two-step etch sequence provides a viable alternative to the CMP plasma etch process for TSV reveal

and other advanced packaging applications such as FOWLP.

To address the relatively high Cu etch rate of SMC6-42-1, we have screened various Cu inhibitors. One Cu inhibitor in particular, I2, works well with a Cu etch rate as low as 0.2nm/min. without affecting the Si etch rate. A Si-over-Cu selectivity of over 2500:1 has been achieved, and the surface finishing of Cu film is smooth and free of any etch defects (pits). This inhibitor works much better than the commonly used BTA in terms of selectivity and surface smoothness. Finally, the chemistry is compatible with common package materials such as PBO and PI. It can be used in advanced package processes where a high Si etch rate and high selectivity are critical.

## References

1. P. Gargini, et al., "The International Technology Roadmap for Semiconductor 2.0", Semiconductor Industry Association, 2015
2. X. Fan, "Wafer level packaging (WLP): fan-in, fan-out and three-dimensional integration." Paper presented at Proceedings of 11th. Int. Conf. on Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems, EuroSimE 2010
3. R. Huemoeller, C. Zwenger, "Silicon wafer integrated fan-out technology." *Chip Scale Review*, Vol. 19 (2), Mar./Apr., 2015. pp. 10-13
4. J. H. Lau et al., "Low-Cost TSH (Through-Silicon Hole) Interposers for 3D IC Integration." Paper presented at Proceedings of 64<sup>th</sup> Electronic Components and Technology Conference, 2014, Orlando, FL.
5. L. Mauer, J. Taddei, R. Youssef, Y. Lu, S. Collins, K. McLaughlin, and C. Allen, "Wet silicon etch process for TSV reveal." Paper presented at Proceedings of 64<sup>th</sup> Electronic Components and Technology Conference, 2014, Orlando, FL.
6. L. Mauer, J. Taddei, R. Youssef, "Silicon etch with integrated metrology for through silicon via (TSV) reveal." Paper presented at 3D Systems Integration Conference (3DIC), IEEE International, 2013, San Francisco, CA.
7. S. Olson and K. Hummler, "TSV reveal etch for 3D integration." Paper presented at Proceedings of 3D Systems Integration Conference, 2011, IEEE, January 31, 2012, Osaka, Japan.
8. L. Mauer, J. Taddei, R. Youssef, "Silicon wafer thinning to reveal Cu TSV." Paper presented at Proceedings of IMAPS Device Packaging Conference, 2012, Fountain Hills, AZ.
9. R. A. Wind and M. A. Hines, "Macroscopic Etch Anisotropies and Microscopic Reaction Mechanisms: a Micromachined Structure for the Rapid Assay of Etchant Anisotropy." *Surface Science*, vol. 460, Issues 1-3, July 20, 2000, pp. 21-38.
10. P. A. Alvi et al. "A Study on Anisotropic Etching of [100] Silicon in Aqueous KOH Solution." *Int. J. Chem. Sci.*: 6(3), 2008, pp. 1168-1176.
11. R. A. Wind et al. 2002. "Orientation-Resolved Chemical Kinetics: Using Microfabrication to Unravel the Complicated Chemistry of KOH/Si Etching." *Journal of Physical Chemistry B* 106, pp. 1557-1569.
12. L. Mauer, J. Taddei, R. Youssef, "Lowering Cost of Silicon Etch for Revealing TSVs" *Chip Scale Review*, Nov/Dec 2013.