Influence of thermal ageing on void content and shear strength for selected lead free solder die-attach

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Abstract

In flip-chip packaging technology, thermal performance can be improved by attaching heat spreader to the backside of the heat generating silicon die via thermal interface material. Solder thermal interface materials (STIMs) are preferred to their polymer-based counterparts because they relatively offer higher thermal conductivities. Unlike lead-based solders which have had a longer application history, lead-free solders are relatively new; thus, the reliability of these lead-free solders are subject of research interest. In this study, lead-free solder preforms with compositions of 96.5Sn3Ag0.5Cu, 99.99In, 97In3Ag and 58Bi42Sn were used for silicon die attachment on copper heat spreader. The void content and shear strength of the soldered joints after thermal ageing at 125^{o}C for 50 hours, 100 hours, 200 hours and 300 hours were evaluated. Generally, the four studied solder joints show decrease in voids with thermal ageing though 96.5Sn3Ag0.5Cu and 58Bi42Sn comparatively manifested more reduction in voids. The shear strengths of 96.5Sn3Ag0.5Cu alloy and 99.99In are shown to be relatively more stable throughout the ageing time. The results also indicate that samples with lower void content comparatively result in higher shear strength and vice versa. These results are especially important for high temperature application environments of Pb-free STIMs like in automotive systems.

Keywords: Pb-free solder; Die-attach; Thermal ageing; Voids; Shear strength; Chip scale package.

1. Introduction

Chip scale packaging (CSP) technology [1] offer promising solution for packaging power electronics due to the technology's relatively improved thermal and electrical performance [1-2]. In flip-chip CSP technology, heat removal from the device is primarily through the backside of the silicon die (chip)[3]. Heat spreader is usually attached to the backside of the heat generating silicon die in an effort to improve the surface area available for heat dissipation, thereby enhancing thermal performance. The bonding of the heat spreader to the heat generating silicon die is often done using die-attach solders (STIMs) in order to improve contact between the mating surfaces and thermal transfer across the interface [4-5].

The result of the aforementioned coupled with the concept that CSP is a growing technology is that the performance and reliability of die-attach solders have become subject of research interest [6-8]. Furthermore, the fact that lead (Pb)-free solders are recent development compared to Pb-based solders has necessitated the

extensive examination of various Pb-free solders in order to understand their potentials as thermal interface materials especially for high temperature applications. This is because the applications of these solders usually experience elevated temperature for a long period of time during service life. For example, in the automotive applications, components and interconnects can be subjected to temperature in the region of 125°C or above for extended periods of time [9]. Hence, high temperature storage (thermal ageing) is one of the reliability tests employed to simulate the effects of such high temperature exposure over an extended period of time. Successful Pb-free solder alloys should manifest high shear strength and resistance to thermal ageing during temperature excursion of up to 125°C.

The objective of this work is to evaluate the impact of different thermal ageing durations on void content and shear strength for selected Pb-free die-attach solders. This study also aims to correlate the significance of void growth/reduction with shear strength.

2. Materials and Experimentation

The Pb-free solders under investigation are as shown in Table 1. Firstly, standard wetting tests (trial tests) were carried out using two (2) copper substrates of dimensions 10x10x0.3mm (representing the die) and 20x20x0.3mm (representing the heat spreader) to find out the parameter limitations for the reflow profiles of the solder performs. The reflows were done in a SM 500CX Batch forced convection type oven. The temperature and time of the four different zones were varied in accordance to the solder preforms manufacturer's guide to get the reflow parameters (shown in Table 2) that produced good bond and thus were used for the main experiments.

Table 1. Investigated solder performs.

Nomenclature	Solder composition (wt%)	Melting point/range (°C)
SAC	96.5Sn3Ag0.5Cu	220 - 217
In	99.99In (eutectic)	157
In/Ag	97In3Ag (eutectic)	143
Bi/Sn	58Bi42Sn (eutectic)	138

Table 2. Parameters used for the reflow profile.

Solder Type	Zone 1 (Preheat) Temperature (°C)	Zone 2 (Soak) Temperature (°C)	Zone 3 (Reflow) Temperature (°C)	Zone 4 (Peak) Temperature (°C)
Bi/Sn	150	150	160	180
In	150	170	180	197
In/Ag	150	163	170	190
SAC	180	180	220	240
Duration (s)	60	120	180	120

A total of sixteen (16) test vehicles were used for the main experiment. A single test vehicle consists of a solder layer sandwiched between metallised silicon die and copper heat spreader. The backside of the die was metallised with Ti/Ni/Ag layers. The dimensions for the copper heat spreader were 20mmx20mmx0.3mm, eight of the metallised silicon die were of size 2.65mm x 3.15mm x 0.43mm and the other eight were of size 2.59mm x 3.73mm x 0.43mm, the different solder performs were 0.05mm thick and were cut according to the sizes of the silicon die.

The assembly process as schematically shown in Fig. 1 commenced with the cleaning of copper heat spreaders with isopropanol, distilled water and finally acetone. A commercially available flux operating at 125°C - 350°C temperature from Indium Corporation [10] was then applied on the heat spreader. Solder

preforms from the different solder alloys were cut out according to the sizes of the different metallised die and manually placed on the copper substrates, the metallised backside of the silicon die were then placed on top of the solder performs. The soldering was carried out with SM500 CXE convection type reflow oven using the different reflow parameters shown in Table 2 for the different solder performs.

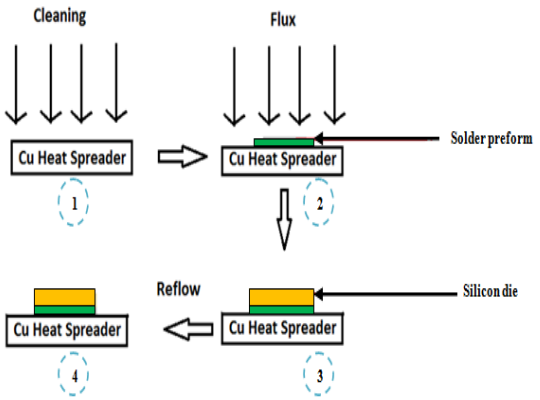

Fig. 1. Schematic of the assembly process.

The as-soldered samples were grouped into four batches. Each of the batches consisted the four different solder preforms sandwiched between the same size of die and copper heat spreader. The void contents in the different solder joints were evaluated using X-ray inspection before thermal ageing of the test vehicles. Samples were subjected to thermal ageing at 125°C for 50 hours, 100 hours, 200 hours and 300 hours. It should be noted that the ageing temperature 125°C is one of the standard high temperatures in both JEDEC[11] and MIL-STD standards (MIL-STD-750C) [12]. At the end of each ageing time, one batch was taken out to check the influence of the temperature soaking on the void content of the Pb-free solder joints using the X-ray machine. Shear tests were subsequently carried out on the four types of solder in a batch after the voiding inspection. A shear tester (Type Series 4000) from Dage Precision Industries was used. The parameters for the shear test were as listed in Table 3.

Table 3. Parameters for shear test.

Test speed	700.0µm/s
Test Load	75N
Maximum Test Load	500.0N
Land Speed	500.0 µm/s
Shear height	100 µm

3. Results

3.1 Study on voids

Voiding is almost unavoidable in solder joints as a result of the complexities and interactions associated with the many factors that affect void formation. Researchers have classified the several factors that can lead to void formation into four categories – methods/machine, materials, human factors and environment[13] (Fig.2).

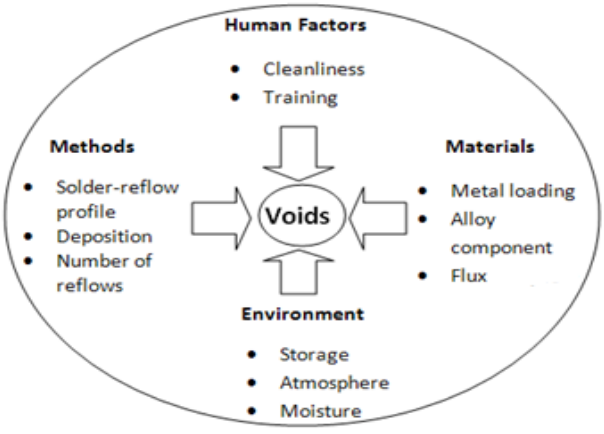

Figure 2. Factors contributing to void formation.

Fig.3 shows an example of void detection in one of the samples using the X-ray machine; the red spots in the figure indicate the presence of voids. The void percentages after reflow soldering (before thermal ageing) and after thermal ageing at

50 hours, 100 hours, 200 hours and 300 hours are accordingly depicted from Fig.4 – Fig.7. During reflow soldering, voiding is mainly caused by the outgassing of entrapped flux within the solder joints when the material is in a molten state [14] and poor wetting of solder [15-16]. Lead (Pb)-free solders are well known for their relatively poor wetting ability [17]. This could be one of the causes of the relatively high percentage of voids in the Pb-free solder joints after reflow soldering coupled that voiding reportedly [18] increases when the substrate area to be soldered is comparatively large. For all samples in a batch, reduction in void percentages was observed in the four different solder joints after each thermal ageing time as shown from Fig.4 – Fig.7 for the different thermal ageing time. This reduction in voids could be attributed to the high flux activity under exposure to elevated temperature. Xu et al. [19] suggested that the selection of a more highly activated flux is vital to the promotion of wetting in Pb-free soldering. The surface tension between the molten solder and substrates is decreased and wetting improves as fluxing reaction increases under exposure to high temperature for a long time [18].

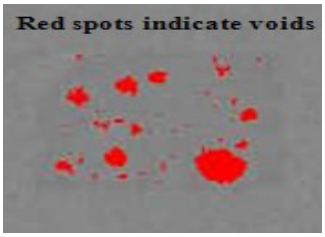

Fig. 3. Example of void detection for a sample using the X-ray machine.

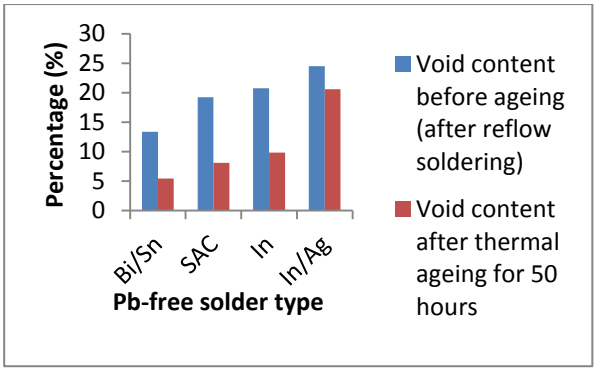

Fig. 4. Void content before and after thermal ageing for 50 hours

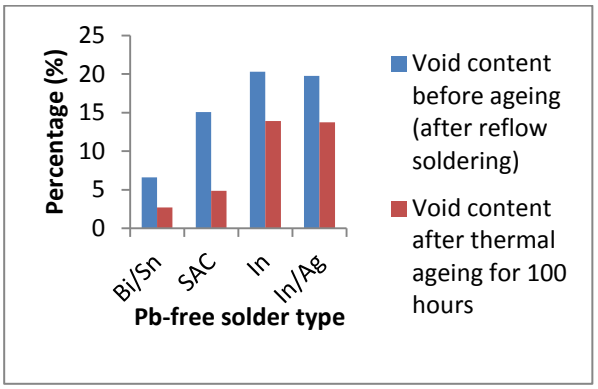

Fig. 5. Void content before and after thermal ageing for 100 hours.

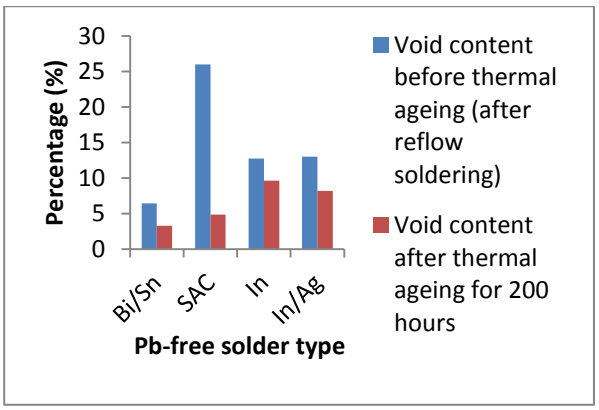

Fig. 6. Void content before and after thermal ageing for 200 hours.

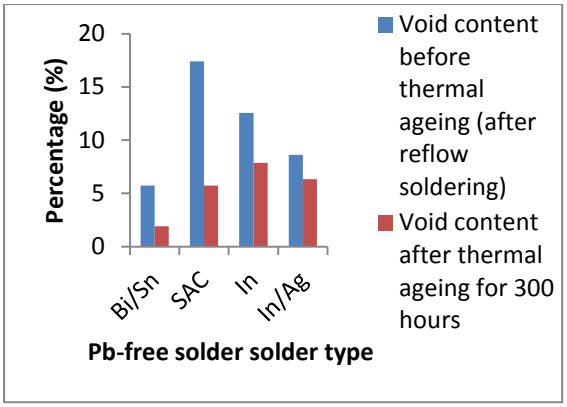

Fig. 7. Void content before and after thermal ageing for 300 hours.

Based on the calculation for average values of void reduction in each solder across the thermal ageing time as shown in Table 4, SAC and Bi/Sn alloys relatively manifested the highest amount of percentage void reduction. As both alloys contain Sn unlike In and In/Ag, the significant amount in void reduction in Bi/Sn and SAC over the thermal ageing time could be attributed to the reportedly improved wetting ability of Sn [20]. The addition of Sn is suggested to improve the wetting ability of Bi/SAC and SAC alloys and thus allows the molten solder to more effectively fill up the air voids and the surface area available for soldering during temperature soak. It is the authors' opinion that the higher surface tension of In might have also contributed to a reduction in spreading out of In containing solder alloys which could impede the wetting ability of the studied In and In/Ag solder alloy and subsequently lead to comparatively less reduction in voids.

Table 4. Percentage reduction in voids for each solder.

Solder type	Percentage reduction in voids (%)				Average values of void reduction across thermal ageing time
	50 hours	100 hours	200 hours	300 hours	
Bi/Sn	59.4	59.09	48.91	66.32	**58.43**
SAC	57.83	67.59	81.21	67.10	**68.43**
In	52.70	31.44	24.37	37.39	**36.48**
In/Ag	15.91	30.45	37.17	26.24	**27.44**

3.2 Study on Shear strength

The shear force values (shown in Table 5) obtained from the Dage bond machine were used to calculate the shear strength of the solder joint using the equation:

$$\tau = \frac{F}{A} \qquad (1)$$

Where τ is the shear strength, F is the shear force applied to the joint and A the wetting area of the solder joint [21].

Shear strength results (Fig. 8) show that the shear strength of the studied SAC solder joint is in the region of 10 N/mm^2 throughout the ageing period. The standard deviation of the set of values obtained for the shear strength of SAC during thermal ageing was less than 1N/mm^2 (0.34N/mm^2). The results suggest that the extended periods the SAC alloy was exposed to do not have a significant effect on its shear strength. The possible reason for this was explained by Oliver et al. [22]; it was found that before ageing, the grains present in SAC solder were mainly small with the larger grains lower in volume. As thermal ageing progresses, the larger grain increases in volume due to coarsening thereby allowing the smaller grains to effectively lock dislocation movements and grain boundary sliding, thus retains the shear strength during ageing. Even though

the magnitude of the shear strength values obtained for In was less than that for the SAC alloy under the same thermal ageing time, similar to the SAC solder joint, there was no significant variation in the shear strength values (within 4N/mm^2) of In as thermal ageing time increases. The standard deviation of the set of values obtained for the shear strength of In during thermal ageing was equally less than 1N/mm^2 (0.52N/mm^2). Similar result trend as regards the less significant discrepancy in shear strength values of In as thermal ageing time increases was also reported by Ding [23]. The In/Ag alloy shows a non-monotonic trend in shear strength, the solder shear strength is seen to increase and decrease across the ageing period. The variation is between 1.5–2.5N/mm^2 between the test intervals. It can be seen that for the Bi/Sn, there was a rise in shear strength with increase in isothermal ageing time up to 300 hours. Oliver et al. [22] reported that Bismuth alloys manifested high strengths during lower ageing time which was seen to reverse after 500 hours. In this study, Bi/Sn and In/Ag could only be evaluated up to 300 hours of thermal ageing due to limited resources. The authors suggest that further research should be carried out on Bismuth containing alloys and In/Ag alloy in order to confirm their performance under thermal ageing.

Table 5. Shear force values.

Solder type	Shear force after each test point (N)			
	50 hours	100 hours	200 hours	300 hours
Bi/Sn	43.21	51.00	79.81	12.96
SAC	84.65	86.48	97.48	104.80
In	32.10	37.69	49.43	44.41
In/Ag	31.09	52.44	42.77	62.93

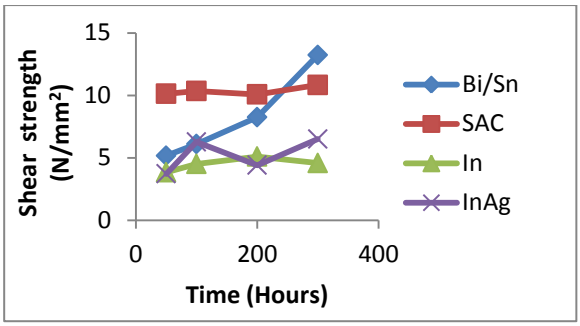

Fig. 8. Shear strength for each thermal ageing time.

3.3 Correlation of voids with shear strength

Fig. 9-12 show that in most cases, samples with lower void percentages mainly manifested increased shear strength when compared to those with higher void percentages. This possibly explains the reason why In and In/Ag were associated with comparatively lower shear strength values as seen in Fig.8 compared to SAC and Bi/Sn that relatively manifested more reduction in voids under thermal ageing as shown in Table 4. In the authors' opinion, the decrease in shear strength of the solder joints with increasing void content is as a result of the combination of reduction in solder joint cross-sectional area due to voids and the initiation and growth of crack in the joint through voids coalescence.

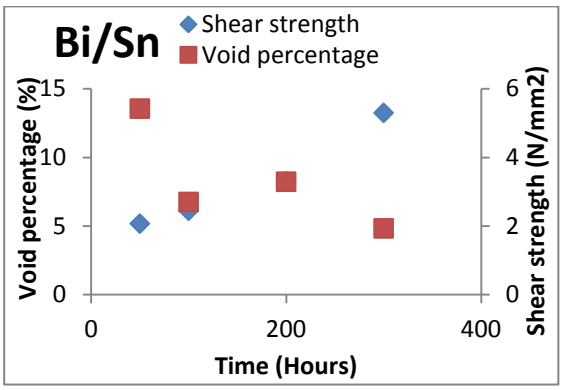

Fig. 9. Correlation between void percentage and shear strength for Bi/Sn.

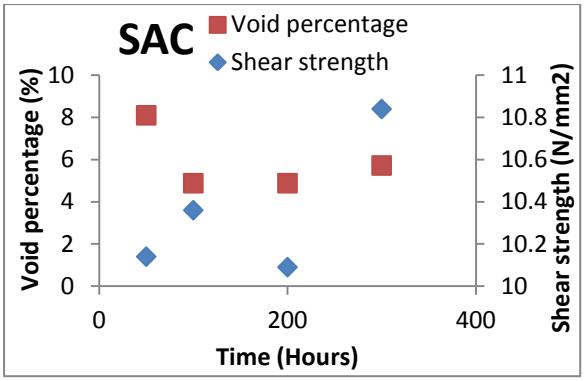

Fig. 10. Correlation between void percentage and shear strength for SAC.

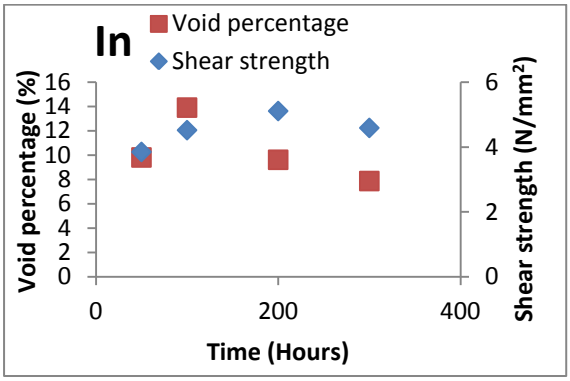

Fig. 11. Correlation between void percentage and shear strength for In.

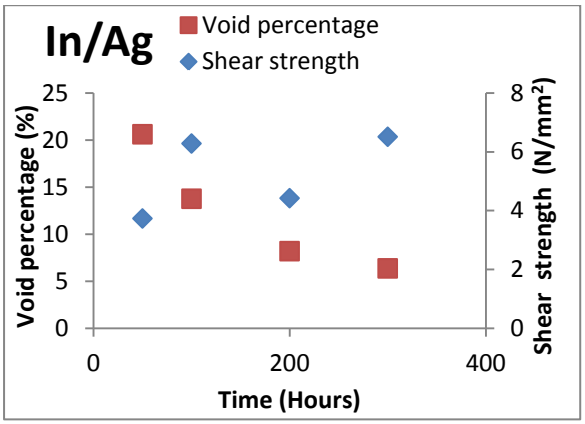

Fig. 12. Correlation between void percentage and shear strength for In/Ag.

The discrepancies in the results of the correlation could be as a result of experimental errors. In addition, the different locations and patterns of the voids may affect the shear strength values of the solder joints. The examination of the role of void locations and void patterns on shear strength is beyond the scope of this study but can form a future study.

4. Conclusion

The influence of thermal ageing on void content and shear strength for selected Pb-free STIMs were evaluated in this paper. The sixteen test vehicles consist of different solder preforms sandwiched between metallised silicon die and copper heat spreaders. After reflow soldering and X-ray inspection for voids, the samples were subjected to different thermal ageing time in order to compare the effect of the duration of thermal ageing on the void content of the solder joints. All the studied solder joints show reduction in voids with thermal ageing with SAC and Bi/Sn relatively manifesting more decrease in voids percentage. After the inspection of the solder joints for voids, shear tests were subsequently carried out on the samples. Comparatively, there was no significant change in the magnitude of shear strengths of SAC and In throughout the ageing period. In and In/Ag relatively showed lower shear strength values. The results also show that most of the samples with lower void content relatively result in higher shear strength and vice versa. Though both SAC and In comparatively performed better in terms of maintaining stable shear strength values throughout the thermal ageing time, SAC appears to compete favourably with In considering that SAC in comparison to In manifested higher shear strength and also showed more reduction in voids under the same thermal ageing exposure. SAC is therefore suggested a better option for die-attach applications subjected to ~125^{o}C temperature.

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References

1. Xuejun, F. and S. Haque. *Emerging MOSFET packaging technologies and their thermal evaluation*. *The Eighth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, 2002. ITHERM 2002.*
2. Xingsheng, L., J. Xiukuan, and L. Guo-Quan. *Chip-scale packaging of power devices and its application in integrated power electronics modules*, *Proceedings 50th Electronic Components & Technology Conference, 2000.*
3. Amy S. Fleischer, Li-hsin Chang, Barry C. Johnson, *The effect of die attach voiding on the thermal resistance of chip level packages.* Microelectronics Reliability, 2006. **46**(5–6): p. 794-804.
4. Otiaba, K.C., et al., *Thermal interface materials for automotive electronic control unit: Trends, technology and R&D challenges.* Microelectronics Reliability, 2011. **51**(12): p. 2031-2043.
5. Subramanian, S.J. *Mechanical Modeling of a Solder Thermal Interface Material: Implications for Thermo-Mechanical Reliability*. 2005: ASME.
6. Kandasamy, R. and A.S. Mujumdar, *Interface thermal characteristics of flip chip packages – A numerical study.* Applied Thermal Engineering, 2009. **29**(5–6): p. 822-829.
7. Ciampolini, L., et al., *Modelling thermal effects of large contiguous voids in solder joints.* Microelectronics Journal, 1999. **30**(11): p. 1115-1123.
8. Manikam, V.R. and C. Kuan Yew, *Die Attach Materials for High Temperature Applications: A Review.* IEEE Transactions on Components, Packaging and Manufacturing Technology, 2011. **1**(4): p. 457-478.
9. Müller-Fiedler, R. and V. Knoblauch, *Reliability aspects of microsensors and micromechatronic actuators for automotive applications.* Microelectronics Reliability, 2003. **43**(7): p. 1085-1097.
10. Indium Corporation, *Thermal Interface Materials*. [cited 2012 9 February]; Available from: http://www.indium.com/TIM/.
11. JEDEC, *Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components*. 2005, Jedec solid state technology association.
12. Department of defense, *Test method standard semiconductor devices*.
13. Anthony A. Primavera, et al. *Factors that affect void formation in bga assembly*. in *Proceedings of the Surface Mount Technology Association*. 1998.
14. W.B. O'Hara, N.-C. Lee, *Voiding in BGAs.* Soldering & Surface Mount Technology, 1995. **7**(3): p. 44 - 48.
15. M. Montano, J.G., W. Shi, M.T. Reiter, U. Vadakkan, K.L. Phillipe, B. Clark, M. Valles, C. Deppisch, J.D. Ferrara-Brown, S.G. Jadhav, E Bernal, MK Kuan, *Novel process techniques to reduce voids in solder thermal interface materials*

used for flip-chip package applications, in *Summer Heat Transfer Conference*. 2005, ASME. p. 2369-2374.

16. Yerman, A.; Burgess, J. ; Carlson, R. ; Neugebauer, C., *Hot spots caused by voids and cracks in the chip mountdown medium in power semiconductor packaging.* IEEE Transactions on Components, Hybrids, and Manufacturing Technology, 1983. **6**: p. 473 - 479.
17. Chang J.; Wang L.; Dirk J.; Xie X., *Finite Element Modeling Predicts the Effects of Voids on Thermal Shock Reliability and Thermal Resistance of Power Device.* Welding Journal, 2006. **85**: p. 63s-70s.
18. Lee, N.-C. (2005) *How to Control Voiding in Reflow Soldering*. Chips Scale Review.
19. Dong-Xia Xu, Yong-Ping Lei, Zhi-Dong Xia, Fu Guo and Yao-Wu SHI, *Experimental Wettability Study of Lead-Free Solder on Cu Substrates Using Varying Flux and Temperature.* Journal of Electronic Materials, 2008. **37**(1): p. 125-133.
20. S. Vaynman, M. E. Fine, *Flux Development for Lead-Free Solders Containing Zinc.* Journal of Electronic Materials, 2000. **29**(10): p. 1160-1163.
21. John H.L. Pang, T.H. Low, B.S. Xiong, Xu Luhua, C.C. Neo, *Thermal cycling aging effects on Sn–Ag–Cu solder joint microstructure, IMC and strength.* Thin Solid Films, 2004. **462–463**(0): p. 370-375.
22. Oliver, J.R., J. Liu, and Z. Lai. *Effect of thermal ageing on the shear strength of lead-free solder joints*. in *Advanced Packaging Materials: Proceedings. International Symposium on Processes, Properties and Interfaces, 2000.*
23. Ding, F., *Flip chip and lid attachment assembly process development*. 2006, A dissertation submitted to the Graduate Faculty of Auburn University in partial fulfilment of the requirements for the Degree of Doctor of Philosophy.