Study of Warpage and Mechanical Stress of 2.5D Package Interposers during Chip and Interposer Mount Process

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Abstract

As data transmission rate increases, flip chip plastic ball grid array (FCPBGA) utilizing a interposer for multiple chips is gaining popularity because of high electrical performance, ease of chip design, ease of thermal management with thermal lid, etc.

The authors assessed package design configuration and key design elements for two chips application assuming 1600 signal I/Os for logic and 800 signal I/Os for memory. Then, we studied warpage behavior of the interposer, and mechanical stress of solder interconnections and low-k dielectric layer under controlled collapse chip connection (C4) pad. We set three different mount process assumptions for chip to interposer and interposer to base organic substrate. The mount process assumptions are (1) two pass reflow of chip to interposer first, then interposer to base organic substrate, (2) reversed sequence of two pass reflow which is interposer to base organic substrate first, then chip to interposer, (3) one pass reflow of chip, interposer and base organic substrate all together. We also set three different interposer material assumptions of Si, glass and organic in this study.

We analyzed warpage behavior and mechanical stress using finite element method (FEM) modeling technique with a set of combinations of coefficient of thermal expansion (CTE) and elastic modulus of the interposers. The study also includes an analysis for conventional multi-chip-module (MCM) FCPBGA as a reference. We show the analysis results of interposer warpage, first principal stress at low-k dielectric layer under C4 pad and von Mises stress at solder interconnections of chip joining and interposer joining.

Keywords: Interposer, Flip chip, PBGA, Low-k dielectric, FEM

Introduction

Higher integration of functionality of the semiconductor device is getting more important to fully utilize high performance of advanced semiconductor technology. One approach is integration on one chip which is called as system-on-chip (SoC). SoC has a challenge of manufacturing yield due to large chip size when large amount of memory is integrated on one chip. Another approach of integration is 3D chip stack using through-silicon-vias (TSV). Typical configuration of 3D package is multiple memory chips, a logic chip and an organic substrate stacked from the top. Wiring to the top memory chip comes from substrate via micro joints and TSV of both logic and memory chips [1, 2]. One of the challenges of 3D chip stack is exactly matched TSV layout between logic and memory chips that requires concurrent physical layout design of electrode terminals. Recently JEDEC published a standard of micro bump layout for wide I/O memory to address the above issue [3, 4].

As TSV technology evolves, an intermediate configuration between SoC and 3D package, which is so called 2.5D package, gains a lot of prominence. 2.5D package utilizes Si interposer with TSV and wiring layers built by re-distribution layer (RDL) technique, and multiple chips are mounted side by side on the interposer [1, 2, 5-9]. There are several advantages of 2.5D package against SoC or 3D package as follows:

- Ease of use of conventional separate chips from chip design point of view.
- Efficiency of active area on each chip because of no keep out area for TSV.
- Efficiency of wiring layers on each chip as the global wiring is built on the Si interposer.
- Efficiency of heat dissipation using thermal lid compared to 3D stack.

Si has been most widely evaluated as an interposer material, but alternative materials such as glass [10-12] or organic are also proposed for interposer. In the previous work [13], the authors studied global package warpage behavior and

mechanical stress at solder joints and dielectric layers under the C4 pad of 2.5D FCPBGA with Si, glass and organic interposers assuming two pass mount process, i.e. chip-to-interposer mount, then interposer-to-substrate mount. In this work, we further investigated thermo-mechanical behavior and thermo-mechanical stress under two other mount sequences with the combination of three interposer materials and three interposer thicknesses.

Model Assumptions

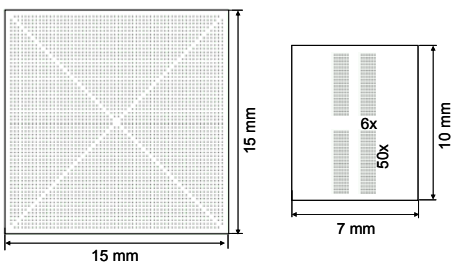
Basic Assumptions

We set basic assumptions of logic chip, memory chip, I/O counts and package size as shown in Table 1. We refer to JEDEC standard MO-305A [4] for micropillar grid array (MPGA) memory chip, and we set simple numbers of I/O count for our design assessment. Custom memory with 200 µm pitch is also assumed for organic interposer and organic substrate as MPGA bump pitch is too tight for organic carrier. Table 1 summarizes the features we use in this study.

The images of bump layout for logic chip and MPGA memory chip are shown in Figure 1. The MPGA memory chip uses a centralized layout, and there are four bump layout blocks in the center.

Table 1 Features of chip and package

Chip size (logic)	15 x 15 mm
Chip size (memory)	10 x 7 mm
Chip thickness (logic and memory)	786 µm
Bump matrix (logic)	94 x 94
Bump matrix (MPGA memory) Bump matrix (custom memory)	(6 x 50) x 4 30 x 40
Signal I/O count (logic)	1600
Signal I/O count (memory)	800
Direct wiring between logic and memory	800
Bump pitch (logic)	150 µm
Bump pitch (MPGA memory) Bump pitch (custom memory)	40 x 50 µm 200 µm
Package size	42.5 mm sq.
Package BGA pitch	1.0 mm
Package BGA ball count	1600
Thickness of base organic substrate	970 µm
Thickness of MCM FCPBGA's substrate	1267 µm

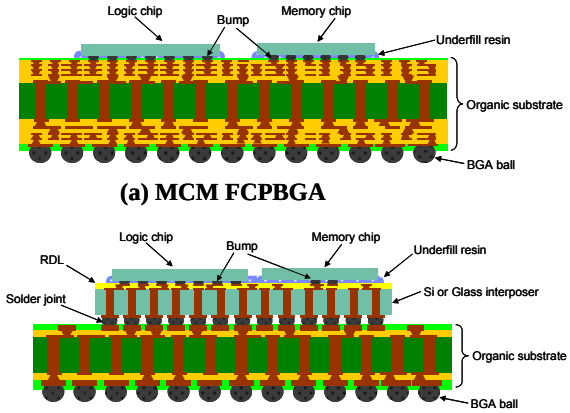


(a) Logic chip **(b) Memory chip**

Figure 1 Bump layout images (not to scale).

Package Configurations

Figure 2 shows package configurations in cross-sectional view. Figure 2 (a) is MCM FCPBGA that uses conventional build-up substrate. Memory chip is assumed to have RDL to convert centralized bump layout to array layout as the escape from centralized bumps to substrate is not feasible with currently available design rule of the build-up substrate. Figure 2 (b) is Si or glass interposer FCPBGA. A logic chip and a memory chip are mounted on an interposer, and the interposer is mounted on an organic substrate. The interposer has RDL on the top side to have escape wirings from both chips and direct wirings from the logic chip to the memory chip. TSV or through glass vias (TGV) is typically laid out in a square matrix, and micro solder balls to interconnect the interposer to the substrate are placed under the TSV or TGV.



(a) MCM FCPBGA

(b) Si or glass interposer FCPBGA

Figure 2 Package configurations.

Design Ground Rules and Key Package Parameters

Table 2 shows the design ground rules of each package configuration. The design rules are used to assess the package key parameters which are the size of interposer and organic substrate, and layer count of build-up substrate and RDL. We set 0.375 mm clearance between logic and memory for Si/glass interposers and 3.0 mm clearance for MCM FCPBGA.

The Si/glass interposer size can be determined by the width of direct wirings between the logic chip and the memory chip (S1 in Figure 3), the width of wirings from logic to TSV/TGV (S2 in Figure 3) and the logic chip size. There are four bump layout blocks on the memory chip (Figure 1). Wirings to the memory's backside bump blocks come from top and bottom side I/O terminals of the logic chip (200 I/Os from top and bottom respectively). Also additional 200 I/Os have to be wired out to TSV or TGV around the direct wirings between the logic and the memory on the top side or the bottom side. Both S1 and S2 come up to approximately 1.6 mm with 4/4 µm line and space ground rule in RDL. The minimum dimension to place these wirings and the chips is approximately 22 mm. Assuming to use

an industry standard solder ball pitch for 1600 micro joints for the interconnection from the interposer to the substrate, 0.65 mm pitch gives the smallest interposer size as 27 x 27 mm with a 40 x 40 solder ball matrix.

Figure 4 shows a typical signal escape of C4 joints. Escaped trace count on one layer can be calculated by the below equation.

$$EscapedTraceCount = \frac{P - D - L}{2L} \qquad (1)$$

Total number of build-up layers is defined by required build-up layer count for signal escape on the top side in case of conventional FCPBGA.

Table 3 summarizes the key package parameters we obtained from the design assessment, and they are used for our FEM modeling.

Table 2 Design ground rule assumptions

Build-up layer (FCPBGA)	
Thickness of one build-up layer	45 µm including Cu
Line / space	15 / 15 µm
Via land diameter	85 µm
Si interposer	
Interposer thickness	200 µm
TSV diameter	60 µm
Line / space in RDL	4 / 4 µm
Glass interposer	
Interposer thickness	200 µm
TGV diameter	80 µm
Line / space in RDL	4 / 4 µm

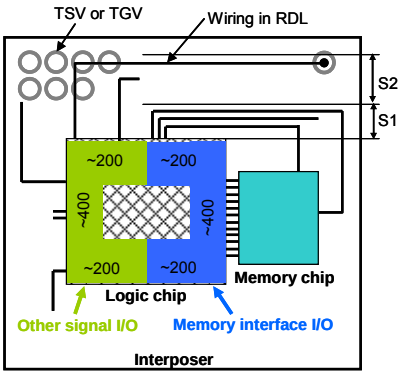


Figure 3 Layout of logic chip and memory chip.

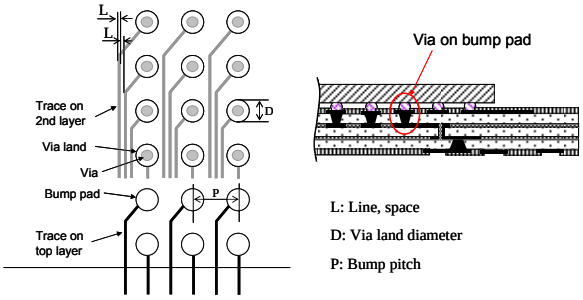


Figure 4 Typical escape design of C4 joints.

Table 3 Key package parameters

MCM FCPBGA	
Substrate layer stack-up	4-2-4
Si/glass interposer FCPBGA	
Layer count in RDL	2
TSV pitch	0.65 mm
Interposer size	27 x 27 mm
Substrate layer stack-up	1-2-1

Mount Process Sequences

We assume that two chips are mounted on a singulated interposer and the interposer is mounted on a base organic substrate. Figure 5 shows three different sequences of chips and an interposer mount process. Sequence-α 'two pass forward' assumes that chips are mounted on an interposer and reflowed first (step-1 joining), then the interposer is mounted on a base organic substrate and reflowed (step-2 joining). Sequence-β 'two pass reverse' assumes that an interposer is mounted on a base organic substrate and reflowed first (step-1 joining), then chips are mounted on the interposer and reflowed (step-2 joining). Underfill is assumed to be applied between step-1 joining and step-2 joining. Sequence-γ 'one pass' assumes that chips, an interposer and a base organic substrate are mounted and reflowed all together. Reflow profile is assumed to be same for all mount sequences in this study.

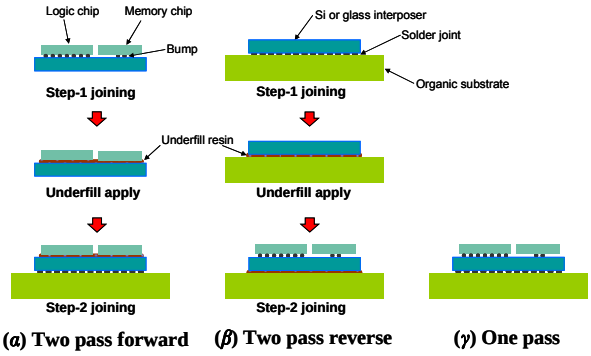


Figure 5 Sequences of chips and interposer mount process.

FEM Modeling and Analysis

We modeled three different sequences of mount process described in the previous section. The models of sequence-α and -β consist of two reflow steps. In the step-2 models, C4 joints of sequence-α and interposer to base organic substrate joints of sequence-β were replaced by composite material of underfill resin and solder. In addition to variations of mount sequences, we examined three different interposer materials and three different interposer thicknesses as listed in Table 4. These models were created in half of the assembled form. The reference temperature is set at 180°C. Z-direction

displacement and mechanical stress are analyzed at 25°C. Table 5 shows the material properties we used in our models.

We analyzed Z-direction displacement of the interposers after step-1 joining of sequence-*α* and -*β*, and Z-direction displacement of the interposers after all components are mounted in sequence-*α* and -*γ*, stress at solder joint between the interposer and the base organic substrate after interposer join reflow, stress at low-k dielectric layers under C4 pad after chip join reflow.

Table 4 Model matrix

Model type	Configuration	Interposer thickness
a	MCM FCPBGA	-
b	Si interposer	100 µm
c	Si interposer	150 µm
d	Si interposer	200 µm
e	Glass-*A* interposer	100 µm
f	Glass-*A* interposer	150 µm
g	Glass-*A* interposer	200 µm
h	Glass-*B* interposer	100 µm
i	Glass-*B* interposer	150 µm
j	Glass-*B* interposer	200 µm

Table 5 Material properties

Material	Elastic modulus (GPa)	Poisson's ratio	CTE (ppm/°C)
Si	165	0.22	3.2
Glass-*A*	77	0.22	3.8
Glass-*B*	74	0.22	6.0
RDL[1)]	28	0.24	17
Build-up layer[2)]	17	0.34	27
Core[3)]	25	0.33	15
Solder	27	0.35	25

[1)] Composite property with Cu

[2)] Composite property with Cu and solder resist

[3)] Composite property with Cu and glass fiber

Warpage of Interposer after Step-1 Joining of Sequence-α and -β

We evaluated warpage of interposer after step-1 joining of sequence-*α* and -*β* to assess feasibility of mounting at step-2 joining. The models do not contain underfill resin to simulate the state after cooling of joining reflow.

Figure 6 shows the contour of Z-direction displacement of the interposer and the chips for sequence-*α* model-*h*. Zero degree of freedom (ZDOF) is fixed along the Z-axis at the center of package as shown in Figure 6. The shape of warpage is concave. Figure 7 shows Z-direction displacement at top right corner point A. Highest Z-direction displacement typically appears at top right corner in our analysis. This is due to the mismatch of CTE between interposer and RDL. Z-direction displacement at point A decreases as interposer thickness increases. Comparing three interposer materials, Si has the lowest Z-direction displacement. Glass-*A* and glass-*B* interposers have similar displacement in spite of the different CTE. 100-µm-thick interposer and 150-µm-thick interposer have more than 200 µm displacement, which will require special mount process technique or interposer flattening technique to mount on the base organic substrate.

Figure 8 is the contour of Z-direction displacement of the interposer and the base organic substrate for sequence-*β* model-*h*. The dotted lines indicate outlines of a logic chip and a memory chip which are not put in this model. Warpage in this case is convex as the organic substrate shrinks more than the interposer because of higher CTE. Z-direction displacement at the logic chip corner point B is shown in Figure 9. Displacements are negative for all model types. Thicker interposer has bigger warpage. This data trend looks consistent with the analysis results shown in Figure 7 although the models for sequent-*β* does not contain chips on the interposer. More than 50 µm warpage of interposer in sequence-*β* is a concern for C4's misalignment at flip chip joining. Glass-*B* interposer has the smallest warpage. This is considered as a result of the highest CTE which is closest to base organic substrate's CTE. Decreasing CTE mismatch between the interposer and the base organic substrate could be an approach to establish stable chip joining in this sequence.

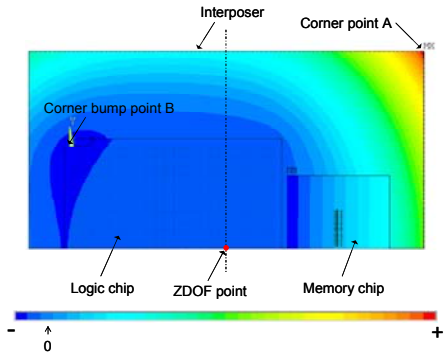


Figure 6 Contour of Z-direction displacement of an interposer and chips: sequence-*α* step-1 model-*h*.

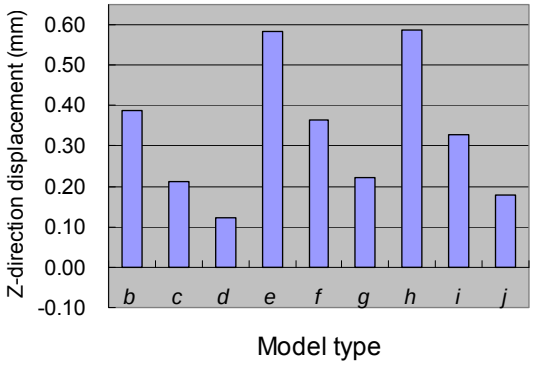


Figure 7 Z-direction displacement at point A: sequence-*α* step-1.

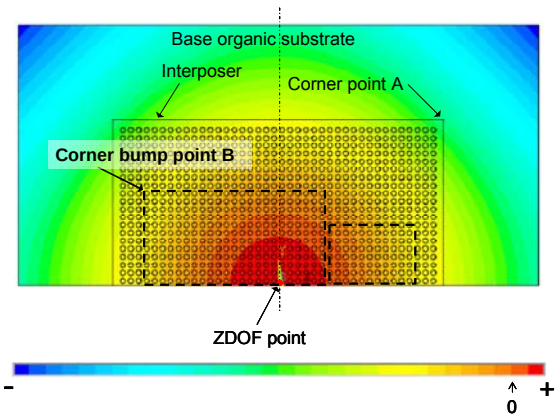


Figure 8 Contour of Z-direction displacement of an interposer and chips: sequence-*β* step-1 model-*h*.

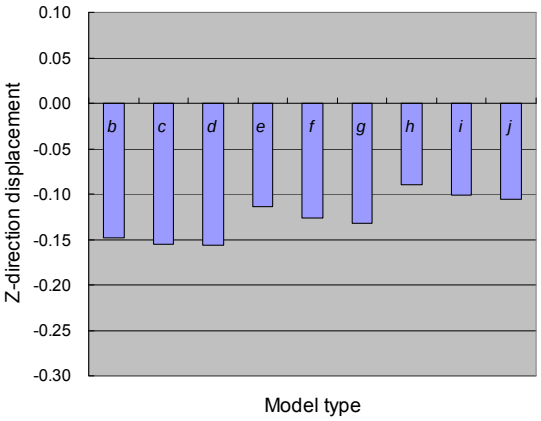


Figure 9 Z-direction displacement at point B: sequence-*β* step-1.

Warpage of Interposer after both Chip and Interposer Joining

Z-direction displacements of interposers were analyzed after both chip and interposer joining for sequence-*α* and sequence-*γ*. Figure 10 shows the contour of sequence-*γ* model-*b*. Figure 11 and 12 show the analysis results for sequence-*α* and -*γ* respectively. Warpage of global package is convex as thick base organic substrate dominates thermo-mechanical global package behavior.

Figure 7 and 11 compares Z-direction displacement after step-1 and step-2. Positive displacements after step-1 decrease in all model types as the base organic substrates shrink at step-2 joining. Si interposer has the biggest warpage in this sequence.

Data trend is very similar between sequence-*α* and sequence-*γ* (Figure 11 and Figure 12). The existence of underfill between the chips and the interposer could be a factor to reduce warpage of the interposer.

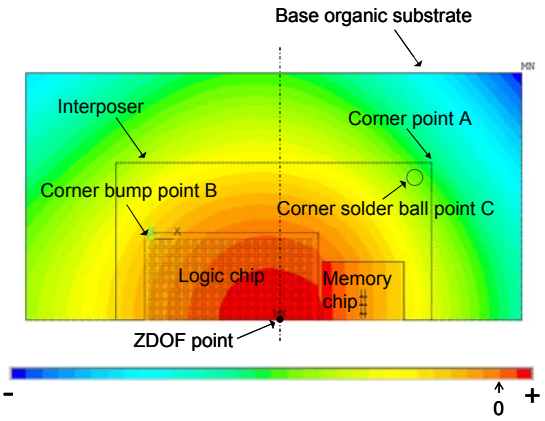


Figure 10 Contour of Z-direction displacement of an organic substrate, an interposer and chips: sequence-*γ* model-*b*).

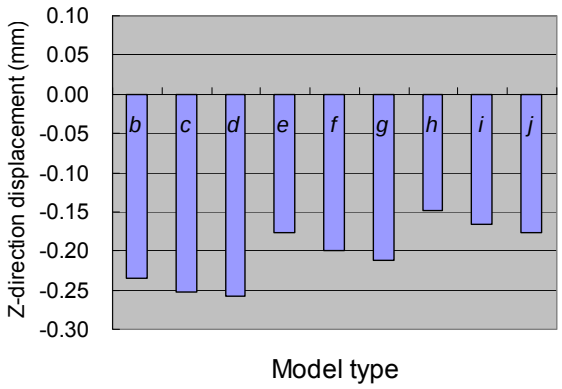


Figure 11 Z-direction displacement at point A: sequence-*α* step-2.

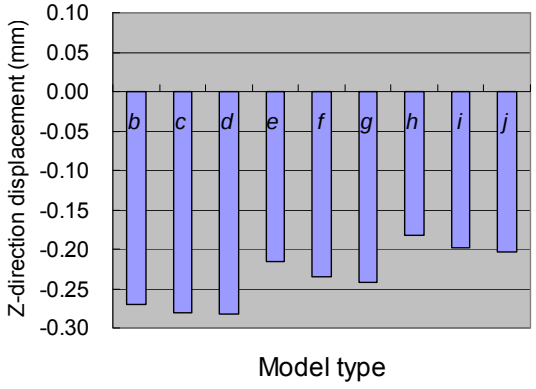


Figure 12 Z-direction displacement at point A: sequence-*γ*.

Von Mises Stress at Solder Joint between Interposer and Base Organic Substrate

We evaluated von Mises stress of solder joint between an interposer and a base organic substrate at corner solder ball point C which is shown in Figure 10 before underfill is applied. Figure 14 shows the results of all sequences and all interposer model types. Comparing three interposer materials, Si interposer has the highest stress and glass-*B* interposer has the lowest stress. This indicates that higher elastic modulus and lower CTE induce higher stress. Also interposer thickness is clearly one of dominant factors. Thicker interposer induces higher stress with all interposer materials. As to mount sequence, there is no clear difference among the three sequences. But the difference of models needs to be noted here. Only sequence-α has underfill resin between the chip and the interposer.

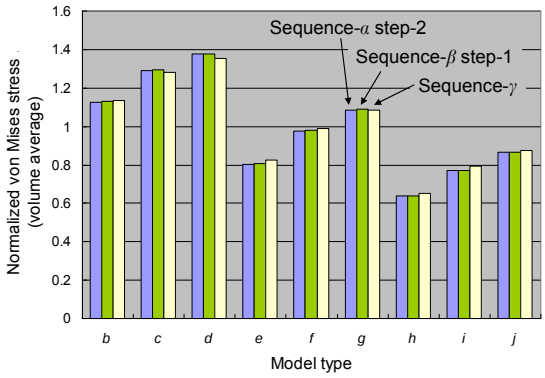


Figure 13 Von Mises stress in volume average at the corner solder ball point C.

First Principal Stress in Dielectric Layer under the C4 Bump Pad after Chip Joining

We analyzed first principal stress in the dielectric layer under the C4 bump pad in the logic chip. MCM FCPBGA was also modeled for comparison to the interposer FCPBGA. Figure 14 shows a micro model of a flip chip joint and dielectric layers under the C4 bump pad. First principal stress was calculated using multi-scale modeling technique by giving strain conditions taken from a macro model to a micro model.

Figure 15 shows typical contours of first principal stress in the dielectric layer under the bump point B which is indicated in Figure 10. Figure 15 (a) Contour of model-*a* (MCM FCPBGA) has the highest first principal stress (tensile stress) in the farthest area from ZDOF under the bump. The other contours show narrower stress ranges compared to MCM FCPBGA.

Figure 16, 17 and 18 show first principal stress in the dielectric layer under bump point B of sequence-α step-1, sequence-β step-2 and sequence-γ respectively. Figure 16 shows that all interposer FCPBGA have much lower stress compared to conventional MCM FCPBGA. Among the three interposers, glass-*B* interposer has the highest stress because of the biggest mismatch of CTE between the chip and the interposer. Comparing Figure 16 and 17, stress induced by sequence-β step-2 is approximately 2.5 times to 12 times higher depending on model types. This indicates that base organic substrate influences low-k dielectric layer through thin interposers. The difference between sequence-β step-2 and sequence-γ is not so big, but sequence-γ has more dependency on interposer thickness and interposer material.

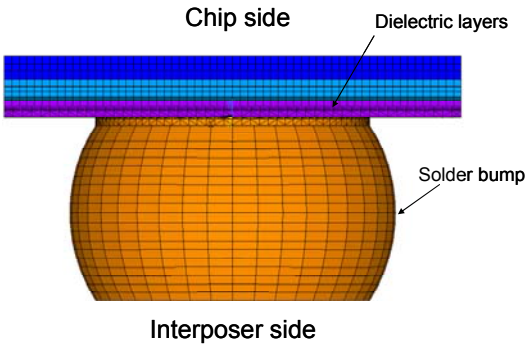


Figure 14 Micro model of a C4 joint and dielectric layers.

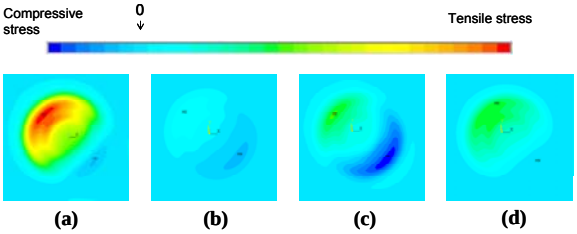


Figure 15 Contours of first principal stress in the dielectric layer under bump point B: (a) MCM model-*a*, (b) sequence-α step-1 model-*h*, (c) sequence-β step-2 model-*h*, (d) sequence-γ model-*h*.

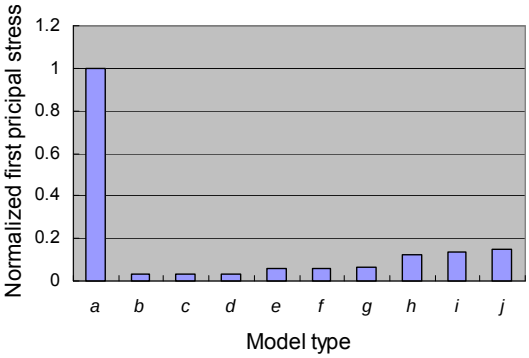


Figure 16 First principal stress in the dielectric layer under bump point B: sequence-α step-1.

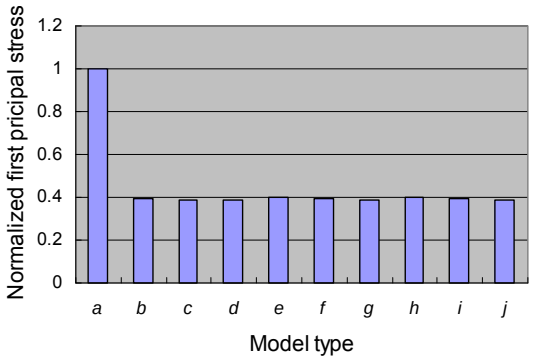


Figure 17 First principal stress in the dielectric layer under bump point B: sequence-β step-2.

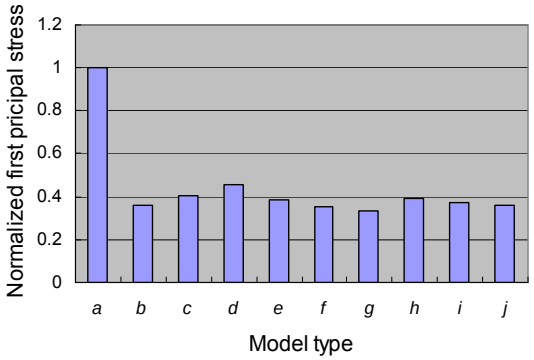


Figure 18 First principal stress in the dielectric layer under bump point B: sequence-γ.

Summary

We investigated feasible interposer designs with the assumption of 42.5 mm package body size, 10 x 10 mm logic chip size, 10 x 7 mm memory chip size, 1600 signal I/O BGA count, 800 signal I/O directly connected between a logic chip and a memory chip. We defined Si/glass interposer size as 27 x 27 mm size using two RDL layers for the FEM analyses. This interposer size can be reduced if we use more RDL layers. In the product design, cost optimization needs to be done considering interposer size and RDL layer count.

We performed FEM mechanical analyses with the combinations of three different mount sequences, three different interposer materials and three different interposer thicknesses. Mount sequence-α and sequence-β are divided into two steps for chip joining and interposer joining.

Analysis of interposer warpage after step-1 joining of sequence-α indicates that interposer warpage is caused by mismatch of CTE between interposer and RDL. Z-direction displacement at the interposer corner point A highly depends on thickness of interposer. 100-µm-thick interposer and 150-µm-thick interposer have more than 200 µm displacement, which will require special technique to mount on the base organic substrate.

Warpage of interposer after step-1 joining of sequence-β is convex. We evaluated Z-direction displacement at the logic chip corner point A. Glass-*B* has the lowest displacement among the three interposer materials, but displacement is more than 50 µm with all interposer thicknesses. It is considered that C4's misalignment is a concern at step-2 chip joining in this case.

Warpage of interposer after both chips and interposer joining was compared for sequence-α step-2 and sequence-γ. Data trend is very similar between the two sequences. Underfill put between the chips and the interposer in sequence-α inhibits warpage in our analysis.

We evaluated von Mises stress of solder joint between an interposer and a base organic substrate at corner solder ball point C before underfill is applied. Comparing three interposer materials, Si interposer has the highest stress and glass-*B* interposer has the lowest stress. This indicates that higher elastic modulus and lower CTE induce higher stress. Also interposer thickness is one of dominant factors. Thicker interposer induces higher stress with all interposer materials. No clear difference is seen among the three sequences in this study.

We analyzed first principal stress in the dielectric layer under the C4 bump pad in the logic chip using multi-scale modeling technique. The analyses include MCM FCPBGA. All interposer FCPBGA models show much lower stress in the low-k dielectric layer than MCM FCPBGA. In case of sequence-α step-1, the stresses with interposers are less than 20% of the stress with MCM FCPBGA. In case of the other two sequences, the stresses with interposers are approximately 40% of the stress with MCM FCPBGA. Thick base organic substrate is considered to increase the stress at low-k dielectric layer in the chip. Dependency on interposer material is clearly seen in sequence-α, and dependency on interposer thickness is clearly seen in sequence-γ.

The authors studied basic thermo-mechanical behavior of 2.5D packages with combinations of mount sequences, interposer materials and interposer thicknesses. The effect of other key parameters such as chip thickness, RDL thickness, and RDL material needs to be studied in the future.

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