Glass Substrates for Advanced Packaging

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Abstract

There has been substantial work done in the past few years to apply glass solutions for Advanced Packaging. Advantages of glass based solutions create significant opportunities by leveraging economies of scale, forming substrates at design thickness and leveraging thermal and electrical properties.

A lot of work is being done to validate the value of glass as an interposer substrate. The ability to leverage both wafer and panel-based metallization strategies for filling glass vias has been shown. Transitioning these processes to cost-effectiveness and high throughput has shown great promise. The electrical performance of glass relative to silicon at high frequencies makes glass solutions very attractive, particularly in RF applications. Electrical models and characterization have demonstrated the advantages of the insulating properties of glass, and its positive impact on functional performance. Reliability tests show that glass solutions can meet device requirements. The substantial progress and readiness in these areas will be presented.

Glass based solutions in panel format provide exciting and cost effective industry opportunities by leveraging economies of scale and glass forming technology. Existing technologies can be used to fill glass vias in a panel format, as well as apply redistribution layers. We will present the status of leveraging panel based technology to enable glass interposers.

Key words

Through-glass-via, TGV, interposer, glass panels.

I. Introduction

Glass has many properties that make it an ideal substrate for interposer substrates such as: ultra-high resistivity and low electrical loss, low dielectric constant, and adjustable coefficient of thermal expansion (CTE). These properties provide opportunities for designers to use glass in new ways for improved packaging solutions [1]-[4].

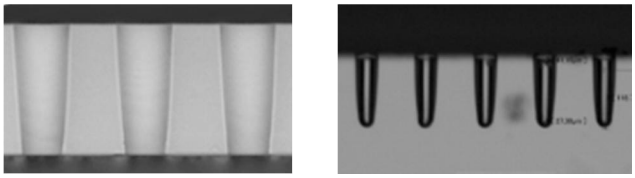
In addition to enhanced technical performance, packaging solutions must also be cost effective. Glass substrates with through-glass-vias (TGV) also provide a number of opportunities for improved performance and cost. There are a number of opportunities that glass provides to enhance cost effectiveness. Glass forming processes such as Corning's fusion forming process gives the ability to form high quality substrates in large formats (> 1 m in size). In addition to scaling glass substrate size, it is possible scale the process to deliver ultra-slim flexible glass to thicknesses down to ~100 µm. Providing large substrates in wafer or panel format at 100 µm thickness gives significant opportunities to reduce manufacturing costs. The advantages given by Corning's fusion forming process for supplying substrates for electronics applications has been previously reported [5], [6].

There has also been a lot of work in recent years demonstrating the ability to leverage and extend existing industry tool sets to fill glass vias with metal, apply surface redistribution layers, and demonstrate reliable structures [7]- [9]. Below we provide a brief summary of this work as well as latest developments for fabrication and performance demonstration of TGV substrates in both wafer and panel formats.

II. Glass Interposer Demonstrators

The ability to provide glass substrates in a cost effective manner as described above is very important. It is also important to enable the leveraging of existing equipment and processes to transform these glass substrates into functional devices.

Corning's process for fabricating high quality vias has been developed to enable fabrication of both through and blind vias in thin (e.g. 100 µm) and thick (e.g. 700 µm) glass substrates to provide opportunities to leverage existing tools. Figure 1 shows recent examples of both through (Fig. 1a) and blind[1] (Fig. 1b) holes in glass substrates. Providing both through and blind holes allows the end user to leverage their existing equipment. For example, wafer based tools are best suited for filling blind vias and many panel-based approaches are suited for metallizing through vias.



(a) Through Holes – Example Above: 35 µm top diameter, 100 µm thick glass

(b) Blind Holes – Example Above: 40 µm top diameter, ~150 µm deep

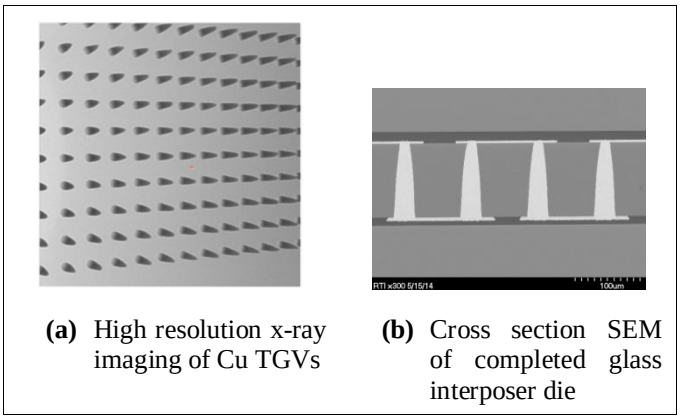
Fig. 1. Demonstration of formation and metallization of high quality through and blind holes in glass.

Fig. 2 shows an example of using wafer based tools at RTI International to fabricate Cu filled, void free blind vias. In this case, the vias had a 35 µm top diameter and 125 µm depth. They were metallized and background to 115 µm thickness and single layer metal was provided on each surface to provide a daisy chain structure [7].

Furthermore, exactly how the metallization is carried out depends on the application. The choice can be driven by cost, throughput, conductivity, hermeticity requirements, etc. For this reason, we have worked across the industry to demonstrate the suitability and availability of a full complement of metallization techniques. Below we highlight several of these.

Fig. 3 shows examples of metallizing through glass vias with both conformal (Fig. 3a) and fully filled (Fig. 3b) plated glass via. Fig. 3a shows a daisy chain structure of conformally plated through vias processed at Georgia Tech's Packaging Research Center (PRC) [9]. Figure 3b shows void free fully filled through vias provided by Atotech [8]. These vias are plated using Atotech's Semi-Additive Process (SAP) and is an approach that should provide significant opportunities for enhanced throughput and cost-effectiveness. The choice of conformal vs. fully filled vias is dictated by application and integration strategies, for example.

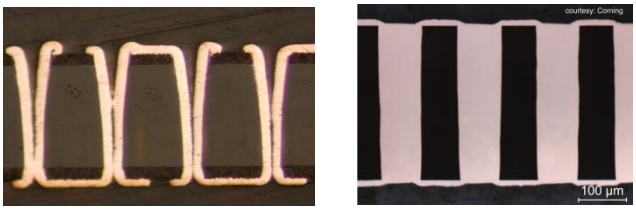
[1] Blind holes are defined as holes that do not extend through the thickness of the glass.



(a) High resolution x-ray imaging of Cu TGVs

(b) Cross section SEM of completed glass interposer die

Fig. 2. Demonstration of filled blind vias. (a) shows x-ray image of void free plating and (b) shows a profile of processed blind vias after metallization and single layer metal layers for daisy chain structure.

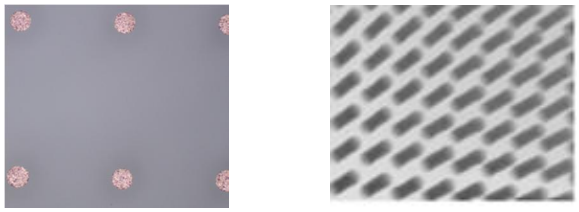


(a) TGV with conformal plating

(b) Fully filled, void free TGV

Fig. 3. Demonstration of formation and metallization of high quality through and blind holes in glass.

Another method to fill primarily through holes is by using paste solutions [10]. There are a large number of paste solutions. Choices can be dictated by firing temperature and conductivity requirements but highly conductive pastes are available. An advantage of paste solutions is the ability to effectively fill large, high aspect ratio holes. Overall performance depends on the particular paste chosen. Fig. 4 shows a top view (Fig. 4a) and an x-ray image void free paste filled hole (Fig. 4b), using a solution from DuPont.



(a) Top view of paste filled 60 µm TGV

(b) X-ray image of paste filled, void free 60 µm TGV

Fig. 4. Images of filled TGV using paste from DuPont.

A. Reliability Testing

We have previously reported the ability to maintain high strength of glass substrates after hole fabrication [6]. Below we report on progress of continued characterization and demonstration of reliability after via fill and additional downstream processing.

We recently reported results demonstrating excellent yield and 100 thermal cycle performance fully filled blind vias after back grind and surface metallization fabricated in conjunction with RTI International [7]. Reliability testing has continued and demonstrated the same performance after 500 cycles from -40°C to 125 °C with 1 hour cycle time. The SEM images of the TGVs and routing metal before and after TCT is shown in Fig. 5. This work is continuing to include 2 side metallization and performance after 1,000 cycles.

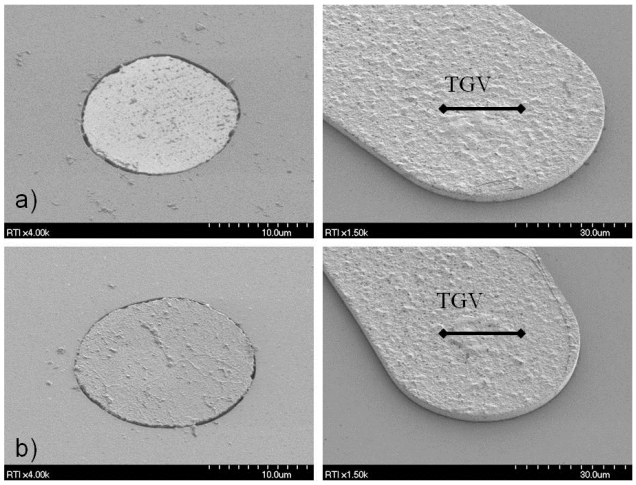


Fig. 5. SEM images of TGVs and first level metal routing layers (a) before and (b) after 500 thermal cycles. No evidence of cracking or lifting was seen in any of the samples after cycling. The black line indicates the position and diameter of the TGV under the Cu routing line.

In addition to the reliability work done above, recent work has been published to evaluate reliability of conformally filled through vias to 1000 cycles [9]. This work consisted of using 30 µm diameter through vias on a 100 µm pitch in 100 µm thick glass. The vias were plated by utilizing a sputtered seed layer and conformal copper plating. Reliability was assessed using accelerated thermal cycle tests between -55 ºC and 125ºC with 15 minute cycle time. There were no failures at the vias, but some failures were seen due to delamination of the copper line (see Fig. 6.)

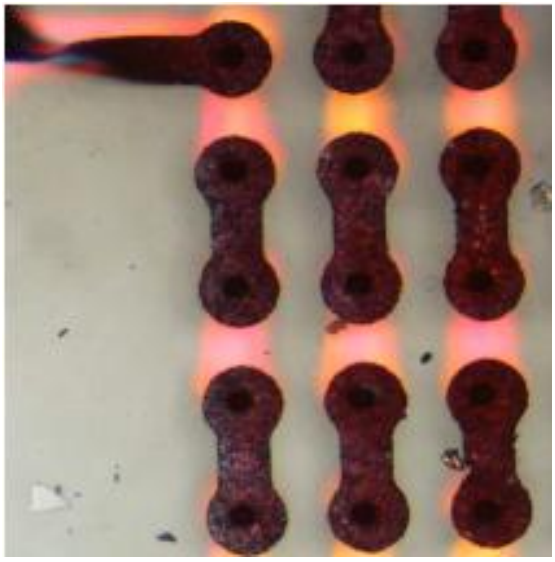


Fig. 6. Image showing copper line delamination – the primary failure mode of 1000 cycle TCT performed at Georgia Tech's PRC.

B. Glass Panel Fabrication

An important aspect of realizing cost effective glass interposers is to leverage the ability to manufacture in panel format and associated economies of scale. Many manufacturing tools exist today that enable fabrication of panel-based glass interposers and electronic components including steps for via fill and lithography.

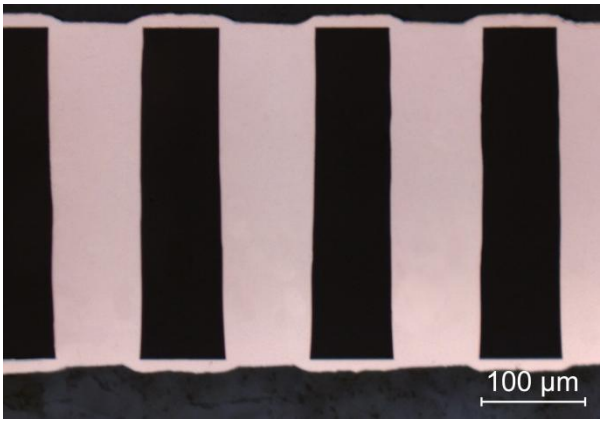


Fig. 7. Results from double side plating using Atotech's Process.

One particularly attractive method to fill through holes in thin glass panels is to process them using a double side plating process. There are challenges in applying standard plating processes to glass, but Atotech has recently reported significant progress in the ability to metallize glass vias using new adhesion promoters [8]. Fig. 7 shows the ability to fill ~80 µm through holes in 300 µm thick glass. As the cross-section image shows, this is done void free today with very little overburden remaining. The advantage of this

approach is that it has the opportunity to leverage existing plating tools and techniques in the industry and provide excellent throughput for panel based interposer manufacture.

C. Panel Level Lithography

Once the holes are filled, it is necessary to have panel level tools to achieve electrical redistribution with fine line and spacing. The thermal stability and low roughness of glass relative to organic substrates provides the opportunity to approach line/space that is achievable in silicon, but in a panel format. Couple this with advancements in the ability to fill holes in a thin glass panel format, significant cost advantages will be realized without compromising L/S requirements. There is an opportunity to leverage tools designed for the flat panel display (FPD) industry to achieve < 3 µm L/S [7].

Recent work has been done with Rudolph Technologies' Jetstep S3500 substrate tool which clearly demonstrates the ability to use advanced packaging toolsets to fabricate fine line and spacing structures on a 370x470x0.3 mm glass panel. A team comprised of Corning Incorporated, i3 Electronics, Rudolph Technologies, and Frontier Industrial Technology worked together to demonstrate ability to apply a single layer Cu metallization to ~3.0 µm L/S. A Cr adhesion layer (50Å thick) followed by a Cu seed layer (2500 Å thick) were sputter deposited to provide the communing layer for subsequent SAP processing. A photoresist layer ~4 µm thick was applied and exposed/developed into several evaluation patterns such as polar/star, escape and interdigitated structures for continuity and bias/leakage testing) targeting 1-10 µm L/S structures. The panels were then plated, stripped, and etched. Fig. 8 shows the example of the metal structures across the panel.

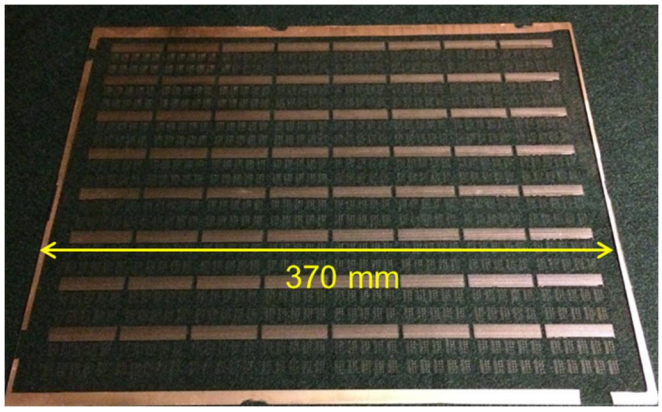


Fig. 8. 370 x 470 x 0.3 mm panel after front side metallization.

Fig. 9 shows close up view of resolution achieved in 1.5 – 5.5 µm structures. The process was able to fully resolve features 3.5 µm and greater. Features 2.5 µm in size were partially resolved. Features 1.5 µm in size were not fully resolved but this is believed to be due primarily to non-optimal photoresist thickness and lithography settings. It is fully expected that additional work would enable the ability to resolve features < 3 µm in size.

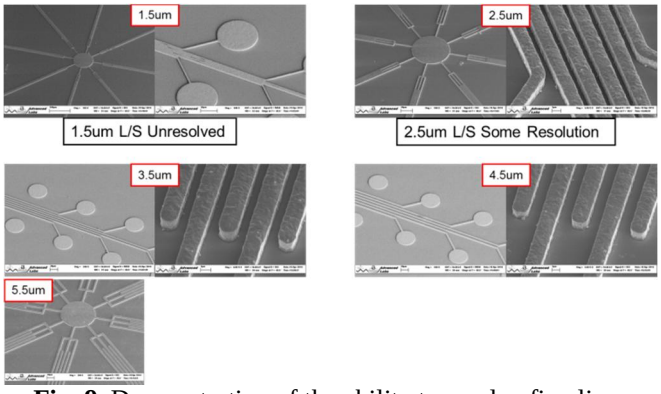


Fig. 9. Demonstration of the ability to resolve fine line spacing on large (370x470 mm) format exposed on Rudolph Technologies' Jetstep S3500. Features ≥ 3.5 µm were fully resolved.

III. Conclusions

The electrical performance of glass, tunability of material properties such as CTE and ability to form in thin large sheets of high quality allowing cost effective processes, generates tremendous incentive for using glass as a TGV substrate for 2.5D and 3D applications.

The ability to generate well-formed through and blind vias has been demonstrated, and fully populated test vehicles using glass interposers have been created. This work shows that existing metallization technology can be leveraged to generate very good Cu filling performance in glass in both wafer and panel formats.

Wafer level is ahead of panel level fabrication for TGV substrates. As reported here, significant process learning and development has been realized in wafer formats with very good results. The RDL results also show that metal can be smoothly plated on the glass with good results. Test vehicles indicate that good electrical, thermal and reliability performance can be achieved using glass vias and the expected advantages in electrical performance of glass relative to silicon have been demonstrated in previous work. This work continues to further demonstrate reliability of these structures on glass substrates.

We report here initial progress in the ability to fabricate and handle large and thin glass panels. With glass, opportunities for truly cost-effective interposer solutions with improved reliability exist, and sustained demonstration of downstream processing continues to move these solutions closer to commercialization.

Acknowledgments

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References

[1] Kim, J, Shenoy, R., Lai, K-Y, Kim, J., "High-Q 3D RF Solenoid Inductors in Glass", Radio Frequency Integrated Circuits Symposium, *IEEE* 2014.

[2] Shenoy, R., Lai, K-Y, and Gusev, E., "2.5D Advanced System-in-Package: Processes, Materials and Integration Aspects", ECS Transactions, **61** (3) 183-190 (2014).

[3] Lai, WC et al., "300 mm Size Ultra-thin Glass Interposer Technology and High-Q Embedded Helical Inductor (EHI) for Mobile Application", International Electronic Devices Meeting (*IEDM*),(2013).

[4] Qin, X, Kumbhat, N., Sundaram, V., and Tummala, R., "Highly-Reliable Silicon and Glass Interposers-to-Printed Wiring Board SMT Interconnctions: Modeling, Design, Fabrication and Reliability", Electronics Components and Testing (ECTC), IEEE 62nd (2012).

[5] Shorey, A; Pollard, S.; Streltsov, A.; Piech, G.; Wagner, R., Electronic Components and Technology Conference (ECTC), IEEE 62nd (2012).

[6] Keech, J.; Piech, G.; Pollard, S.; Shorey, A., "Development and Demonstration of 3D-IC Glass Interposers", Electronic Components and Technology Conference (ECTC), IEEE 63rd (2013).

[7] Shorey, A et al, "Advancements in Fabrication of Glass Interposers", Electronic Components and Technology Conference (ECTC), IEEE 64th (2014).

[8] Fu et al., "Adhesive Enabling Technology for Directly Plating Copper onto Glass/Ceramic Substrates", Electronic Components and Technology Conference (ECTC), IEEE 64th (2014).

[9] Demir et al., "First Demonstration of Reliable Copper-plated 30 µm Diameter Through-Package-Vias in Ultra-thin Bare Glass Interposers", Electronic Components and Technology Conference (ECTC), IEEE 64th (2014).

[10] Crumpton, Cofield, and Bacher, "Through-hole Plugs and Thermal Vias", http://www2.dupont.com/MCM/en_US/tech_info/techinfo01.html