# A Small Feature-Sized Organic interposer for 2.1D Packaging Solutions

***Christian Romero, Jeongho Lee, Kyungseob Oh, Kyoungmoo Harr & Youngdo Kweon***
*Advanced Circuit Interconnect Division*
*Samsung Electromechanics Co, Ltd*
*Suwon City, South Korea*

## ABSTRACT

The continuing advancement of semiconductor devices steadily increase the number of global interconnects and higher I/O counts thus driving more the importance of smaller feature size interconnects. One of the most difficult technical challenge for interconnects involves new material development, however, it is believed that mitigation of the impact of size scaling such as its aspect ratio (thickness/width) and spacing could fill the gap for high dense packaging requirement brought by Moore's Law. The next generation substrate design rules require a process capability with less than 50um pitch to accommodate leading-edge mobile applications such as Wide I/O memory-Logic packaging integration.

In this paper, we describe an organic interposer that is capable of providing high density interface between chips with large I/O counts therefore could be an attractive low-cost 2.1D packaging solution. Our concept can demonstrate ultra fine line interconnects with width/space below 5um with microvias having pitch below 50um which can be effective solution for high density routing. This feature enables the ICs to be attached directly to the substrate therefore eliminating the need for a silicon interposer needed in conventional 2.5D package architecture.

Microvia formation using photo-imageable material is another key feature of our organic interposer offering favorable cost efficiency for designs requiring very large numbers of microvias. The buildup layers could be vertically connected by microvias with min. 10um diameter using this process. Aside from the simplicity in supply chain, the high density organic interposer has the potential to meet both power and bandwidth requirement therefore can be considered an incremental move from conventional system-in-package providing flexibility in performance and yield capacity that allows integration of advanced logic and memory devices.

We will present our various feasibility results of electrical/mechanical performance obtained from our fabricated test vehicles.

## 1. 0 Introduction

### 1.1 Meeting the High Dense, I/O count requirement

As feature size in microelectronics packaging continues to shrink in accordance to Moore's law, the next generation package substrate requires routing with ultra fine pattern capability in order to support increasing chip I/O density with shrinking form factors. Today's leading companies anticipate the innovation in 2.5 and 3D stacked ICs using TSVs to achieve both power and bandwidth requirements associated with the radical increase in I/O count. While 3D TSV integration is potential solution, the ecosystem that it needed for commercialization is still long way to go. Implications and concerns associated with 3D circuits include rising heat dissipation posing higher reliability issues and electromagnetic interactions due to parasitic capacitance and inductance effects [1].

Due to these limitation in 3D packaging, the implementation of intermediate substrate such as high dense interposer in advanced IC packaging is receiving more emphasis as a valid integration solution and is strongly moving forward as compared to 3D IC development. It will also require meeting a combination of stringent design specs in electrical parameters such as IR loss, impedance matching and signal propagation in order to achieve the desired signal integrity at high speed applications.

Common trends in packaging application today is the integration of high performance Logic and memory device such as Wide I/O Memory (WIOM)or High Bandwidth Memory (HBM) and the primary functions of interposer is to accommodate high speed data buses between these two devices. Since the total I/O count of both devices will easily reach by the thousands, a high dense interposer must provide a high dense die-to-die interconnect that would ensure high bandwidth, low loss parallel channels.

Also, as the chip/package I/O count continue to increase, the fine pitch requirement for advanced devices continue to shrink. The Wide I/O memory as defined by its JEDEC standards has minimum required bump pitch is 40um. The high I/O count and density would dramatically increase the need for more escape routing layers and create Signal integrity issues more serious. One of the most difficult challenge for interconnects involves new material development, however, it is believed that mitigation of the impact of size scaling such as line aspect ratio (thickness/width) and spacing could be a potential direction in meeting high dense packaging requirement.

Such concept of a high dense die-to-die interconnect substrate with fine feature size is attractive not only for non-heterogeneous integration but also for highly functional SoC with complex architectures processed in sub-28nm technology. Die split or partitioning in smaller functional blocks may receive greater benefits in terms of cost and higher manufacturing yield performance. The cost potential of this is dependent on the yield curve and process cost of the partitioned blocks as well as the number of dies in the package.

## 2.0 Fabrication of Organic Interposer

The emergence of smart devices, tablets and wearable gadgets has created new drivers for next generation substrates. The work presented in this paper is an organic hybrid interposer with fine pattern that serves as the routing layer for high speed I/O interconnects. The interposer can be the actual package and can be directly assembled to the final system board.

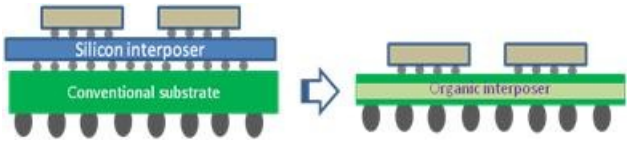


**Figure 1:** Emerging Packaging approaches using high dense, fine feature-size Interposers

The front-end process consists of sequential steps in conventional CCL fabrication that includes panel plating, thru hole drilling and plugging, laminating and metal etching. This process step may involved repetitive build-up of several metal layers depending on the required design for performance. Process variation may be seen during core layer preparation where special adhesion materials may be needed to improve adhesion to the substrate material.

The microvias are formed using photosensitive dielectric material. After the substrate is coated with the photosensitive dielectric layer with about 5 to 10um thickness, exposure is done with a mask aligner, developed and cured. Before depositing copper through electroplating as interconnect on top of the dielectric layer, it is required that a thin seed layer is deposited first. If the seed layer is poorly deposited, the uniformity of the copper will be affected as well as the potential risk of poor adhesion.

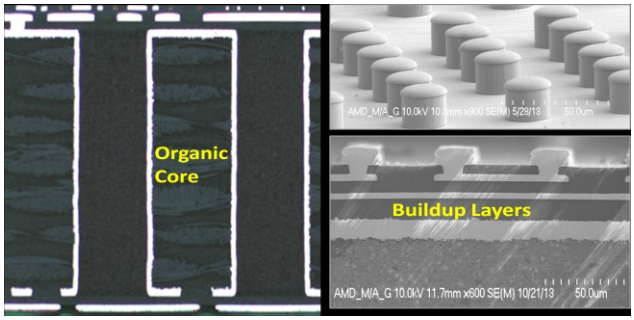


**Figure 2:** Cross section of the organic interposer showing the buildup structures and micro bumps for die attach using thermal compression bonding method

The inner core metal layer thickness can be controlled between 10um to 18um therefore these layers could be effectively used to contain ground and power planes for critical PDN requirements of the active chips. The thickness of the core can be fabricated typically between 100um to 400um depending on electrical and mechanical requirement.

### 2.1 Test Vehicle Structures

Several test vehicles were fabricated and available at different buildup structures. One of these is a test vehicle shown in Figure 3. It was designed to study both electrical and mechanical feasibility of the concept. In this test vehicle, we considered high dense die-to-die interconnect with a minimum line width/space of 3um/3um and minimum via pad pitch of 50um. With these dimension, it is possible to route four (4) traces between vias pad thus these layers can handle high routing density requirement of advanced chip applications such as application processors and high bandwidth memory devices.

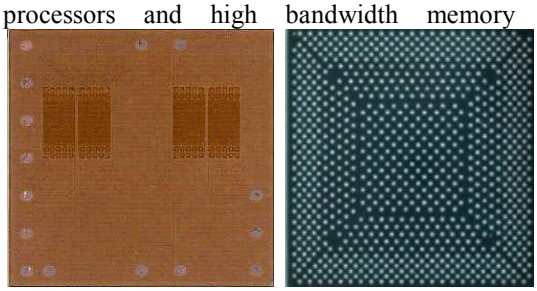

**Figure 3:** Organic Interposer demonstrator sample. Top side for the die attach using micro bumps (Left). Bottom side with pads for the BGA (Right)

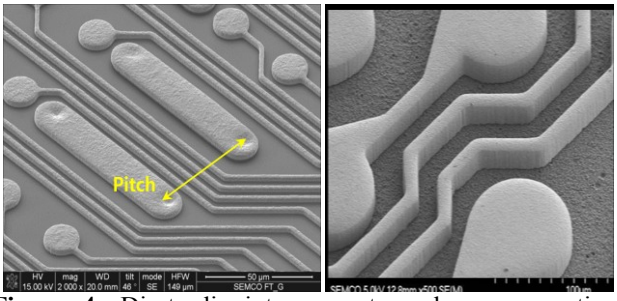


**Figure 4:** Die-to-die interconnects and escape routing lines at pitch below 50um.

The test vehicle described above consisted of total of six layers with size of 21.2 x 22.7mm where two buildup layers are assigned for the die-to-die interconnects carrying critical I/O data.

The buildup layers are typically between 3 to 5um thickness. As a design rule, all nets for the power distribution network (PDN) are located in the inner CCL of the organic core due to its thicker metals in order to control the IR loss of the power delivery.

## 2.2 Surface Roughness measurement

At shrinking feature size, the surface roughness of Cu interconnects is a key parameter in controlling its resistivity. Signal delay will significantly deteriorate due to increased resistance thus will limit the signal transmission.

The roughness was calculated from measured data and was executed at high magnification for better averaging. Parameters measured were Ra and Rz. Ra is the arithmetic mean roughness in a contour surface while Rz can be found by the sum of the maximal peak and maximal valley depth in the contour surface as depicted in Figure 5.

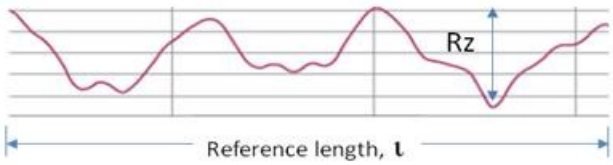


**Figure 5:** Surface roughness measurement specification

Ra is the arithmetic average of height deviations of surface peaks and valleys as given by the formula:

$$Ra = (1/L)\int_0^L |Z(x)|dx$$

where L is the length of the surface being measured, and Z(x) is the function of its profile height.

The physical properties of the interconnects as shown in Figure 6 was investigated using Atomic force microscopy (AFM).

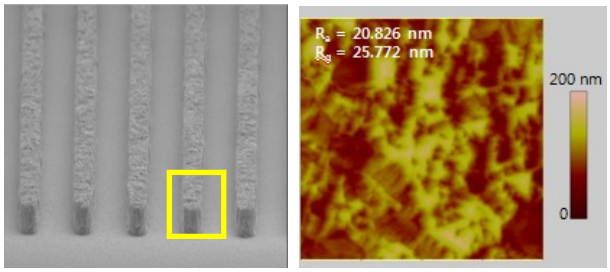


**Figure 6:** Surface Roughness measurement using AFM

## 2.3 Microvia Formation

As the I/O count constantly increasing, the via counts per unit area also drastically increase therefore the challenge for developing a high density interposer is to fabricate reliable microvias with lower cost per area. The traditional method such as drilling or laser has limited process capability in forming diameters smaller than 50um as well as its difficulty in obtaining via-via pitch below 100um. In order to meet the via density challenge, the use of photo-imageable dielectric material to form microvias could offer several advantages in terms of fabricating high interconnect density at lower cost. The microvia formation process that was briefly described in previous section would result one shown in Figure 7 and multiple stacked formation as shown in Figure 8.

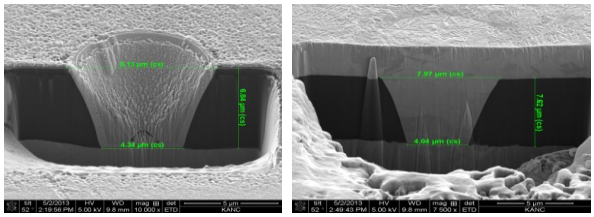

**Figure 7:** Fabricated microvia**.** Non-plated hole before Cu plating (Left), After Seed layer deposition and Cu plating (Center), Final via structure (Right)

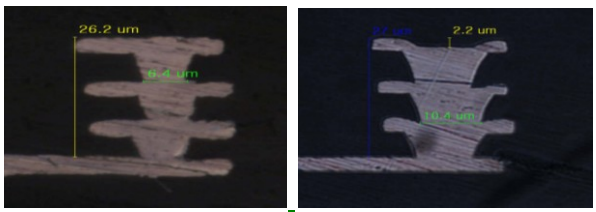


**Figure 8:** Microvias in stacked formation, 6um Diameter (Left), 10um Diameter (Right)

## 2.4 Microvia Resistance

Microvias with smaller diameter obviously reduce the contact size that may lead to an increase in parasitic contact resistance, which can be a limiting factor in achieving high performance and reliable interconnects especially in power distribution network designs. The electrical interface provided by the microvias must be evaluated to ensure electrical reliability with optimum signal delivery performance.

To quantify the microvia resistance, a test structure with concept similar to a Kelvin cross-bridge structure was design and fabricated for laboratory measurement. The total resistance consist of the microvia structure plus its contact area resistance could be estimated empirically by supplying current across the via under test while measuring the voltage difference. The Kelvin test method will dramatically improve the measurement accuracy by removing the parasitic effects of the test probes and feed lines. The microvia diameter under test has a diameter of 10um with height of 5um. However, due to some process variation that may result to via misalignment, the effective contact area presented by the microvia may present certain measurement variations.

Figure 9 shows the statistical result of the measurements done on two different sample build run with 10samples each.

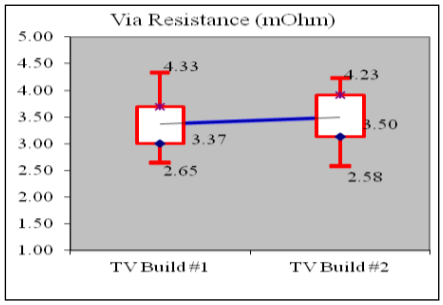


**Figure 9:** Microvia resistance measurement

## 3.0 Reliability Results

The reliability is a critical part of ultra-fine interconnections as much as performance. One leading cause of reliability failure in smaller feature size interconnect is metallic electromigration due to its smaller metal grain size. In order to evaluate electromigration, a test structure was designed and fabricated and subjected to accelerated conditions.

Shown in Figure 11 is the basic implementation of the test structure. The design is a comb-pattern structure with minimum line width/space of 3um with sufficient length to avoid resistance saturation under extreme test conditions. The opposite ends of each comb-pattern are terminated with voltage tap for biasing and monitoring of any resistance changes.

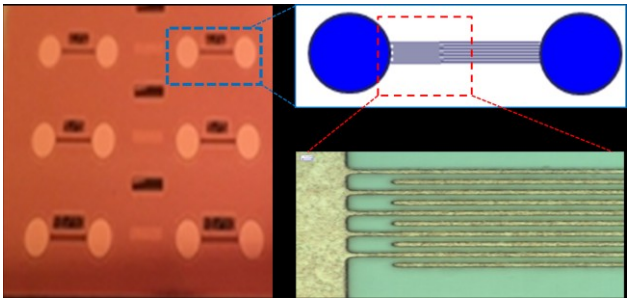

**Figure 10:** Test vehicle for EM Testing with voltage tap for in-situ resistance monitoring. Minimum metal line width/space is 3um/3um.

Electromigration test was performed at 130degC, 85%RH with bias voltage=3.7V. The in-situ resistance was measured over time with duration of 96hours. The resistance was monitored in-situ and failure criteria is set to 10% deviation from its 0-hour measurement. Failures related to dielectric material usually bring dramatic change in resistance brought by the breakdown voltage.

The results in Figure 11 showed no visible effect of metallic migration and no significant deviation of the resistance values as compared to 0-hr readings.

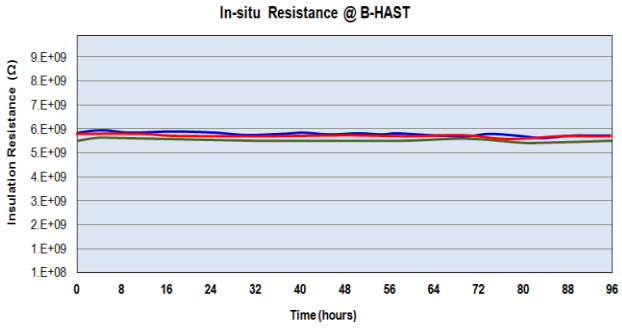


**Figure 11**: Insulation resistance measured during BHAST

## 4.0 Channel Loss Characteristics

For package designs, the interposer could be a major source of signal integrity issue related to the narrower interconnect widths due to impedance discontinuities and other channel losses related to dielectric loss, metal surface roughness and skin effect at high frequency operations. These interconnects must distribute clock and other high-speed signals and provide power and grounding to the various functional blocks of the ICs. The physical length of these interconnects tends to scale according to the available process technology nodes [2]. Although technology scaling is beneficial in extending the

packaging density, it threatens to limit the interconnect performance especially at increasing data rate and higher operating frequency [3].

The RF characteristics of the interconnects were analyzed and measured by designing various test coupons such as the one showed in Figure 12. The line/space of the differential lines is 3um with 5mm length. The test pads are designed with GSG (ground-signal-ground) configuration. S-parameter measurement was done with a measurement system consisted of network analyzer and fine-pitch RF probes. The accuracy of the measurement was improved by performing SOLT calibration from 100KHz to 6GHz. The measurement was particularly focused on high frequency applications common to mobile applications from 1MHz to 3GHz operation.

The RF characteristics was measurement and presented in the Figures below. In Figure 13, the measured forward transmission loss is about -0.2dB up until 1GHz frequency. The half-power frequency point is about 2GHz. Figure 14 shows the measured crosstalk behavior and is seen to be better than -25dB below 1GHz frequency.

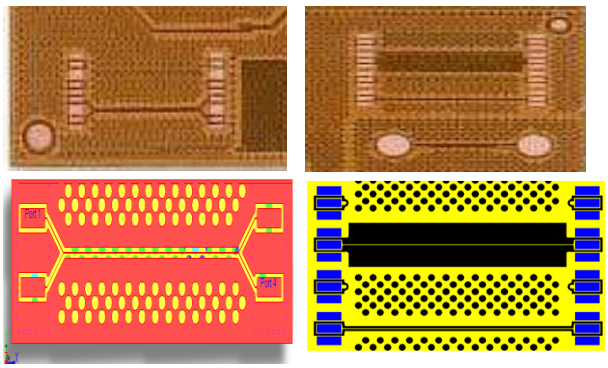

**Figure 12:** Differential and Single-ended lines for characterizing interconnect channel loss.

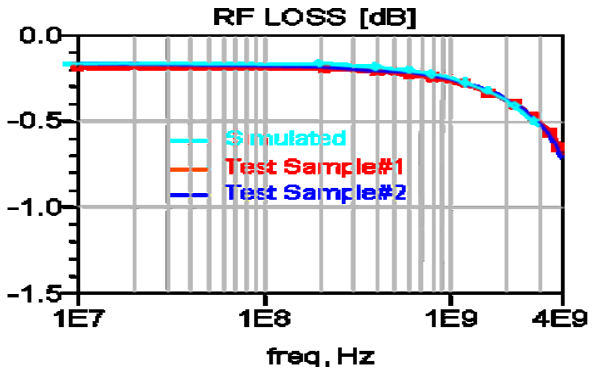


**Figure 132:** Measurement Results for RF Loss of test samples. Simulation model was correlated with measured samples.

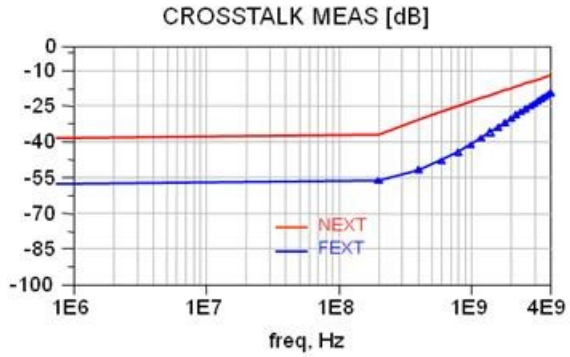


**Figure 14:** Measurement Results for Crosstalk characteristics

## 5.0 SUMMARY

This paper demonstrate the design and fabrication of a novel organic interposer for high I/O pin-count, ultra fine-pitch chips through an ultra fine line/space organic interposer in a 2.1D integration with small form factor and low profile package. The advantage of this concept includes multi-die packaging design that could provide high dense interconnects, and provide a potential step forward to full 3D applications.

## 6.0 REFERENCES

[1] Banerjee, et.al; " 3D IC: A Novel Chip Design for Improving Deep-Submicrometer Interconnect Performance and SOC Integration" Proc IEEE May 2001.

[2] S. Muthukumar, C.D. Hill, S.Ford, W. Worwag, T. Dambrauskas, P.C. Challela, T.S. Dory, N.M. Patel, E.L. Ramsay, D.S. Chan, "High Density Complaint Die-Package Interconnects", ECTC 2006

[3] J.A. Davis, R. Venkatesan, A. Kaloyeros, M. Beylansky, S.J. Souri, K. Banerjee, K. Sawaswat, A. Rahman, R. Reif, J.D. Meindl, " Interconnect Limits on Gigascale Integration (GSI) in the 21st Century", IEEE Proceedings Vol. 89, No. 3, 2001