Understanding Cleaning of Vias Fabricated Using Micro Mechanical Punching in Liquid Crystal Polymer (LCP) Substrate

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Abstract

The objective of the research is to understand the effect of chemical treatment's etching times on via wall roughness; and the direct current (DC) and reverse pulse plating (RPP) of vias fabricated using micro mechanical punching process on liquid crystal polymer (LCP) substrate. One major drawback of micro mechanical punching process is the formation of LCP and copper burrs. Sequential wet chemical etching and oxygen plasma cleaning techniques were developed as an effective tool for the removal of these burrs. The wet chemical process required a sequential oxidation, etching, and acid neutralization treatment for the effective removal of LCP and copper burrs. These treatments have an effect on the surface roughness of the through via wall. Under this research time dependent experimental matrices were designed to observe the effect of the wet chemical etching on the via wall surface roughness. Sequential oxidation, etching, and acid neutralization treatments were done, where only one treatment time was varied for 1, 5, and 10 minutes keeping the other treatment times constant at 5 minutes. After examining three different experimental matrices for via wall roughness using a scanning electron microscope (SEM), it was observed that the longer treatment time using chemical etchant will make the surface rougher. In addition, it was also observed that the oxidation treatment time of greater than 5 minutes produced the same roughness irrespective of treatment time variation. The neutralization treatment time does not have any effect on the roughness of the LCP via wall. Two different approaches named - DC and reverse pulse plating (RPP) were used to plate the vias. It was found that the RPP does not result in good via filling, because it produced high current concentration at the edges and consequently over plating at the edge compared to the inside of the via. In stark contrast, DC plating delivers completely plated vias after 4.5 hours, which is a 7 μm/hr plating rate.

Key Words: *Liquid Crystal Polymer (LCP) Substrate, Micro Mechanical Punching, Wet Chemical Etching of Micro Vias, Via Surface Roughness, Micro Texturing of Surface, Direct Current (DC) plating, Reverse Pulse Plating (RPP)*

I. Introduction:

In research and development of any electronic system significant focus must be given to the packaging of the individual components and the entire system itself [1]. Reasons for this focus is because of four crucial and distinct functions electronic packaging need to provide: (1) power supply between chip and external circuitry, (2) protection from external environment and mechanical support for the die and chip carrier package, (3) signal input/output through interconnects, and (4) transportation of heat that is generated by the chip during its operation [2]. Packaging as a platform of structural and environmental integrity enhances the reliability not only for IC components but also for MEMS devices [3]. In foldable electronics 3-D flex module packaging used, where the reliability of the packaged module is dependent on the stress concentration at different heterojunction of the packaging materials [4]. Packaging for harsh environments like marine and oil mine applications require special care for sustainable mechanical rigidity at high temperature and pressure. In this regard, glob top encapsulation is usually added to the die to add extra environmental protection and physical stiffness to the die [5-6]. In cryogenic packaging (at 4 K) applications, electronic components show a performance magnificent due to its operation at very low temperature with least resistance from the packaging materials [7]. Power electronics generate excessive heat during operation in aerospace applications for example. In this example, the integration of thermal vias and micro heat channels into the packaging is crucial [8]. In addition to performing heat transport, micro vias fabricated at wafer level and chip scale packaging provides necessary electrical interconnection [9-10].

Amid different requirements, various applications, different packaging materials and substrates, liquid crystal polymer (LCP) is gaining the spotlight as a substrate for its advantageous material properties. LCP is a thermoplastic material with very notable qualities that will be described here. With regard to radio frequency (RF) properties, it has a low loss tangent of 0.0025 as compared to the 0.005 in LTCC. For its low dielectric constant of 2.9 at 10 GHz and room temperature makes it a best suitable candidate for RF applications [11]. In addition, LCP has a high chemical resistivity of 98.7% as compared to 95% in Kapton. Likewise, LCP has low moisture absorption of 0.04% at room temperature and 100% relative humidity for 24 hours compared to the 2.8% for Kapton [12-14]. A comparative study of different substrate materials are given in the table 1.

Table 1: Comparative studies of different substrate materials used in MEMS packaging

	LCP - ULTRALAM 3850 [12]	***LTCC - DuPont 951 Green Tape [13]***	***Kapton - Dupont HN100 [14]***
CTE (ppm/°C)	*17 (X & Y axis) 150(Z-axis)*	*5.8*	*20*
Melting Temp. (°C)	***335***	*738*	*360*
Thermal Conductivity (W/m/°K)	*0.2*	*3.3*	*1.09*
Dielectric Constant @ 10 GHz, 23°C	***2.9***	*7.1*	*3.5*
Dissipation Factor/Loss Tangent @ 10 GHz, 23°C	***0.0025***	*0.005*	*0.002*
Chemical Resistance	*98.7%*	-	*95%*
Water Absorption (23°C, 24 hrs)	***0.04%***	-	*2.8%*

Development has been completed for micro via fabrication on different organic substrates like LCP, myler and others. Micro via fabrication on these substrates was done using different via fabrication techniques like mechanical drilling, hot embossing, e-beam machining, plasma cleaning, and laser ablation [15-25]. High aspect ratio vias with diameters ranging from 5µm to several hundred microns can be fabricated using these techniques. However, in this research we have chosen to fabricate micro vias using a mechanical punching technique for its low cost, high speed, repeatability, and uniformity as compared to the via fabrication technique like laser ablation, e-beam machining, mechanical drilling, plasma etching etc. Uniform via arrays with a via size of 50 µm and controlled pitch of as low as 75 µm was reported by the author using this technique [26]. One obvious artifact of any mechanical punching is the production of burrs from the bulk material or the substrate. The mechanical punching of LCP was no exception. LCP and copper burr formation during the micro mechanical punching is the major issue for uniform via metallization, which is necessary for very good electrical interconnection. To address this issue a sequential chemical etching and plasma cleaning was reported by the author [27]. However, there were no study presented on the effect of chemical etching treatment time on the surface roughness of the via wall. In this paper the authors are presenting the correlation between the chemical etching treatment time and the roughness of the vias wall.

II. The LCP substrate and test via specifications:

The LCP substrate used in this experiment was supplied by Rogers Corporation, with brand name ULTRALAM 3850^{TM}, which has very stable electrical properties for highly controlled impedance matching. The surface resistivity of $1x10^{10}$ Mohm, volume resistivity of $1x10^{12}$ Mohm/cm, dielectric breakdown voltage of 3500V/mil allows the circuit designer using ULTRALAM 3850^{TM} to consider using a thinner dielectric layer and more challenging designs. The ULTRALAM 3850^{TM} is available in 25 µm, 50 µm, and 100 µm thickness with ¼ oz. (10 µm) and ½ oz. (20 µm) copper cladding on both sides. Because LCP has a very low dielectric constant it gives the best advantage to choose a thinner film of 25 µm. However, to have more mechanical robustness of the LCP substrate during fabrication process 50 µm LCP with ½ oz. (20 µm) copper cladding was chosen for these experiments.

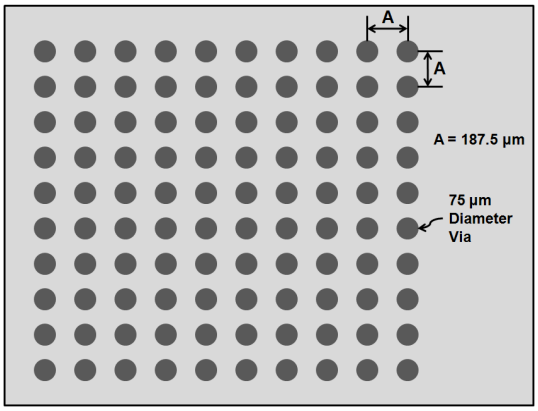

Figure 1: Test via specifications

We attempted aggressive size and space specifications for this development. The vias were fabricated with a diameter of 75 µm and with 187.5 µm pitch as shown in Figure 1. The pitch 187.5 µm came from the unit pitch scheme introduced by Chowdhury, et al. [26]. The number of vias in an array was chosen to be 10 x 10, because it was found that with increasing number of vias in an array there will be more Z-axis expansion of the LCP substrate [26]. The Z-axis expansion will limit assembly yield if it is too large.

III. Test via fabrication using mechanical punching process:

Pacific Trinetrics Corporation, CA, USA (model APS-8718) mechanical punching system was used to fabricate the micro vias. During the mechanical punching process the pin impinges the substrate and pierces through the LCP and Cu cladding. In the micro via fabrication process using mechanical punching, the substrate is placed on top of a die bushing which has a larger diameter than the punch pin. If the die bushing is smaller than the punch pin, for example 3.5 mil (87.5 µm) die instead of 4.5 mil (112.5 µm) for a 3 mil (75 µm) punch; will tend to break the pin very easily. This is because of its increased probability of hitting the die edge rather than the die center due to die and pin alignment tolerance limits. In addition, a smaller die will tend to leave a slug clogging the die. Clogging of the die makes it impossible to clean and reuse. Larger die eliminates the chance of clogging and makes the die reusable. Therefore, a 4.5 mil (112.5 µm) die was used for 3 mil (75 µm) pin. A vacuum connection was made to the underside of the die to remove ejected material.

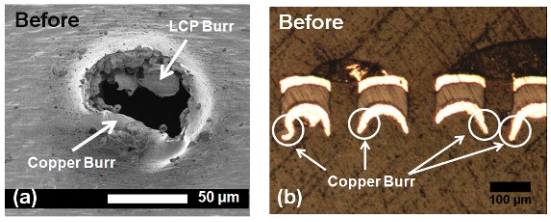

Figure 2: (a) LCP burr formation inside the though via wall, (b) copper burr formation in the bottom copper film after micro mechanical punching

One major concern for the uniform via fabrication and its subsequent metallization is the LCP and copper burr formation during the micro mechanical punching process. The bottom view in Figure 2(a) and cross sectional view in Figure 2(b) shows burr formed in a mechanically punched via. These burrs could be a possible source of obstruction for the void free metallization, where these burr will act as a current concentration point.

IV. Chemical Etching for LCP and Copper burr removal:

Rohm & Hass Corporation's (Currently Dow Chemical) PROMOTER 3308A (40% $NaMnO_4$) and PROMOTER 3308B (< 30% NaOH) were used as oxidizing and etching agents, respectively. To activate the functional group during the oxidation and etching process an elevated temperature of 85 ^{0}C was chosen [28-29]. Because the wet chemical treatment is based entirely on oxidizer and hydroxide groups it will leave residual ions inside the through via, which is not desirable. Therefore, there is a need to neutralization these ions using acidic solution, which led to the selection of 3314 Neutralizer (3% H_2SO_4 + 3% H_2O_2). It should be noted that the acidic solution will etch copper, which is not be desirable for this process integration. To address this issue, room temperature treatment of the neutralizer was chosen so that the copper etch rate be reduced at the lower temperatures.

V. Experimental matrix for chemical etching and surface roughness evaluation:

Table 2: Experimental matrices to investigate the effect of oxidization, etching, and neutralizing agent on the via wall roughness process. Samples were of 75 µm with 187.5 µm pitch and 10 x 10 via array

	PROMOTER 3308A (20 – 40 % $NaMnO_4$) @ 85^{0}C	PROMOTER 3308B (NaOH < 30%) @ 85^{0}C	3314 Neutralizer (3% H_2SO_4 + 3% H_2O_2)
Sample 1	5 Min	*1 Min*	5 Min
Sample 2	5 Min	*5 Min*	5 Min
Sample 3	5 Min	*10 Min*	5 Min

Experimental Matrix - 1

	PROMOTER 3308A (20 – 40 % $NaMnO_4$) @ 85^{0}C	PROMOTER 3308B (NaOH < 30%) @ 85^{0}C	3314 Neutralizer (3% H_2SO_4 + 3% H_2O_2)
Sample 4	*1 Min*	5 Min	5 Min
Sample 5	*5 Min*	5 Min	5 Min
Sample 6	*10 Min*	5 Min	5 Min

Experimental Matrix - 2

	PROMOTER 3308A (20 – 40 % $NaMnO_4$) @ 85^{0}C	PROMOTER 3308B (NaOH < 30%) @ 85^{0}C	3314 Neutralizer (3% H_2SO_4 + 3% H_2O_2)
Sample 7	5 Min	5 Min	*1 Min*
Sample 8	5 Min	5 Min	*5 Min*
Sample 9	5 Min	5 Min	*10 Min*

Experimental Matrix - 3

Three different experimental matrices were designed and presented in Table 2. These designed experiments investigate the effect of the oxidizing, etching, and neutralizing agent on the roughness of via wall. In the first experimental matrix, the treatment time for PROMOTER 3308A (etching) varied for 1, 5 and 10 minutes, where the treatment time of PROMOTER 3308B (oxidation) and neutralizer were fixed at 5 minutes. Likewise in the other matrices, one agent was varied for 1, 5 and 10 minutes keeping the other two treatments time fixed for 5 minutes. These experiments aided in examining the effect of shorter and longer etching time, and corresponding roughness on the via wall. Note that the sample 2, 5 and 8 went through the same chemical etching treatments; therefore, we examined only one sample out of these three. It was reported that the 5 minutes of PROMOTER A, 5 Minutes of PROMOTER B and 5 minutes of neutralization give the best cleaned through via [27].

VI. Surface roughness after wet chemical etching:

The surface of the LCP vias gets directly exposed to the chemistry during the chemical etching process. The via surface is roughened to various degrees because of the exposure to the chemistry and the time of exposure. The LCP vias were examined using SEM to determine the roughness of the vias after chemical etching. FEI XL30 ESEM system from Philips was used in these experiments. It should be noted that the system is capable of delivering 30 KeV of power to the electron gun, but only 2 KeV power was used to eliminate the chance of LCP surface texture modification by high power electron gun. In addition, high power concentrates charge and gives a bright spot on the sample. SEM images of via wall were taken by tilting the sample for 30^0 after loading into vacuum chamber. Figure - 3 shows the SEM images of the textured surface due to the variation of the treatment time and chemistry.

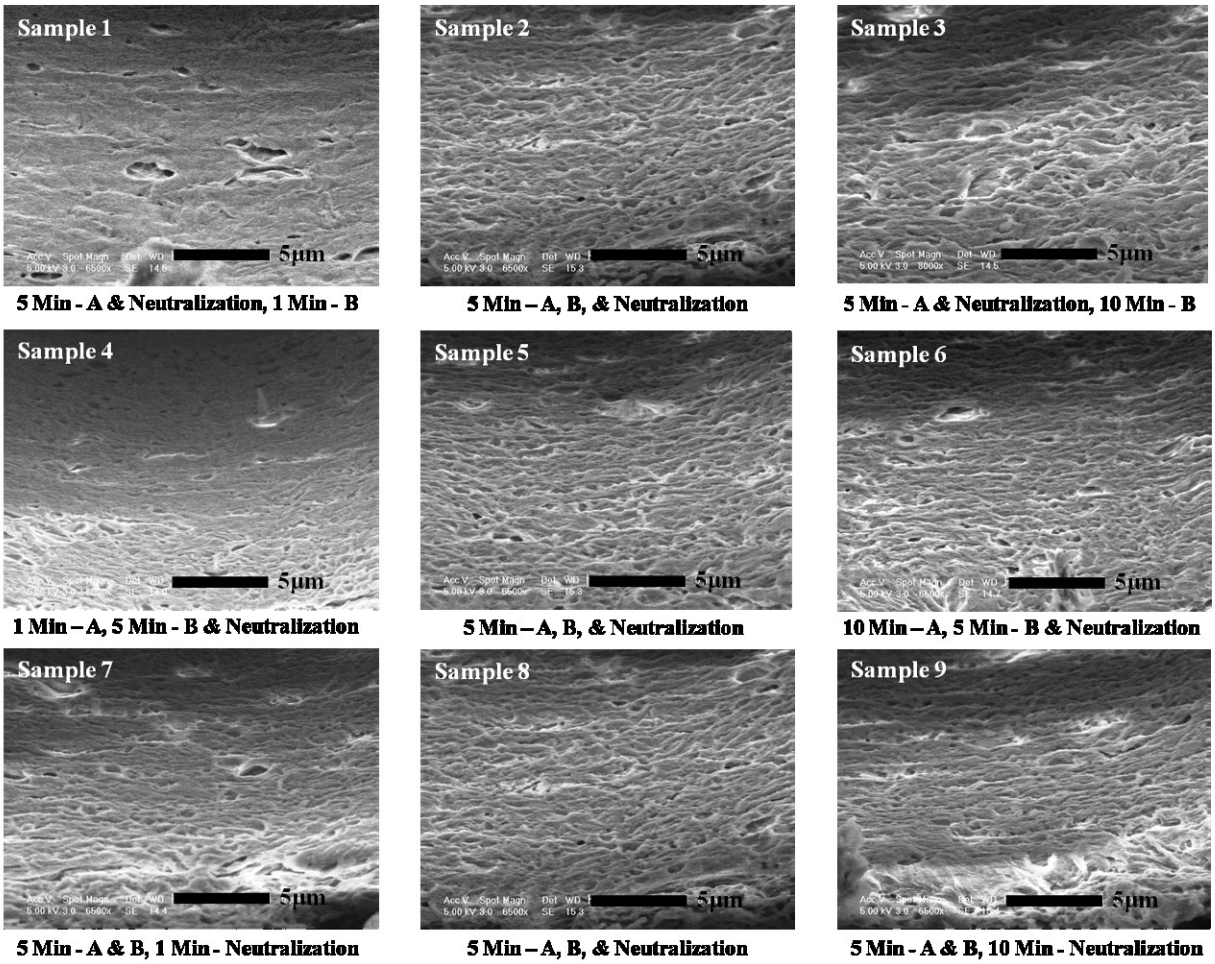

Figure 3: SEM images of the LCP via surfaces after different chemical treatments time as shown in the experimental matrices in Table 1

After examination of the SEM image of sample 1, 2 and 3, it was noticed that the longer etching with promoter B (etching agent) produced the much rougher surface. This is because of the longer interaction time of the LCP with the etchant after being oxidized for 5 minutes. In sample 4, it was noticed that 1 minute of oxidization does not have an effect on the surface roughness although the LCP surface was under treatment with etching agent (Promoter B) and neutralized for 5 minutes. Oxidation agent treatment times longer than 5 minutes does not show increased roughness in sample 6. Looking at the SEM images of sample 7, 8, and 9 it was found that the neutralization treatment time variation does not have an effect on surface roughness for samples which are already treated with the oxidation and etching agent for 5 minutes. Therefore, it was observed that among all three treatments the etchant (Promoter B) has the most influence on surface roughness. It should be noted that there were no quantitative measurements such as atomic force microscopy (AFM) or non contact optical profilometry performed.

VII. DC and reverse pulse plating of the sample:

Metal can be deposited electrochemically by applying constant voltage, constant current or periodic pulsed plating in forward and reverse direction. In electroplating the sample to be plated is connected to the cathode (-Ve) and the desired plating metal to the anode (+Ve). There are two distinct methods of plating that are both considered. First, direct current (DC) plating is where the voltage source remains constant with varied current level depending on the deposition rate and the granular structure of the deposited metal. To obtain a smoother surface, a low current concentration should be used, where the deposition rate will be slower. However, an accelerator could facilitate the process [30]. DC plating is a continuous deposition process where measures should be taken to avoid void formation inside the plated vias.

The second method of plating is the reverse pulse plating (RPP). In RPP, a constant positive current supply is made for specific amount of time. Immediate after the positive current supply, a high current concentration with negative bias is applied to the sample after which a small delay in the current supply is used to stabilize the process. In RPP, the high negative bias acts on the plated sample where it will take off extraneous plated metal specifically from locations where the current concentration is usually higher during the positive current bias. Figure - 4 shows the periodic current wave form for RPP. 10 mA/cm^2 current density was applied for the forward bias, 100 mA/cm^2 for reverse bias, and no current was applied for the off status during the RPP. For DC plating, a constant current supply of 10 mA/cm^2 was applied for the entire plating duration.

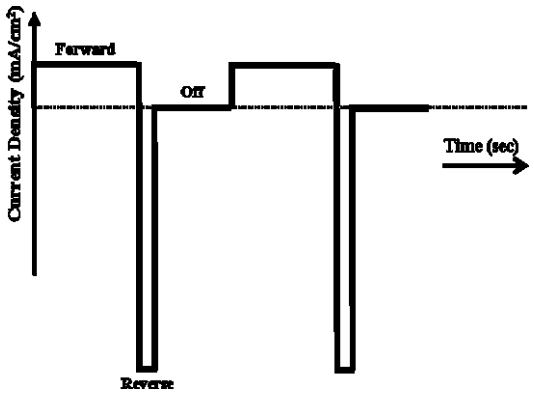

Figure 4: The positive, negative, and off state of the current concentration in reverse pulse plating (RPP)

Before initiating plating, a thin seed layer of few microns needs to be deposited so that plating metal ion can be attracted towards the seed layer and start the electroplating process. Varian XM-8 sputtering tool was used for depositing copper seed layer. The deposition of the seed layer was made in two step process. First, the deposition of the thin titanium layer is made to act as an adhesion layer between the LCP substrate and copper seed layer. A 1000 watt power supply was chosen to supply power to the DC magnetron plasma generator for titanium depostion. This amount of power is capable to deposit 20 Å/sec. Therefore, 2 passes of 20 second duration with 2 minutes interval between passes were chosen to achieve the desire thickness of 800 Å.

After the titanium layer deposition was complete, the wafer was then moved to the next deposition stage for copper seed layer deposition. 800 watt power supply was used to achieve a deposition rate of 120 Å/sec. 10 passes of 20 second duration were made with 2 minute intervals between passes to get the desired thickness of 24000 Å or 2.4 μm. The selected powers are in the lower range of the system capacity to minimize over stress on the substrate due to rapid temperature increase and forced cooling. To make a conformal seed layer deposition same sequential deposition of titanium and copper seed layer were repeated keeping the bottom part of the wafer exposed to target.

After the seed layer deposition, the sample was taken for plating in a modified plating bath

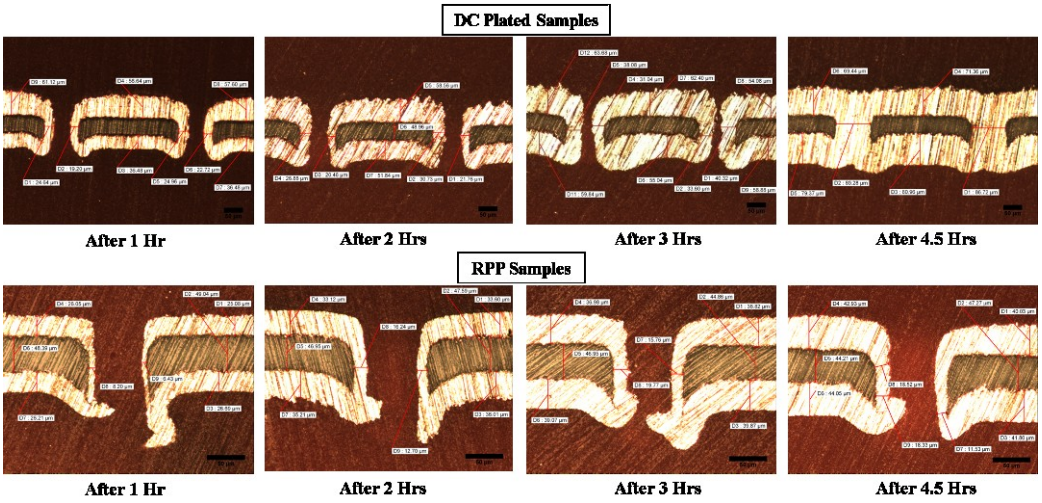

Figure 5: Cross sectional view of the plated sample with DC and reverse pulse plating after 1 Hr, 2 Hrs, 3 Hrs and 4.5 Hrs

fabricated in-house. Because there is need for plating the through vias at the same rate from the top or bottom of the substrate, the plating was done for both sides, simultaneously. The in-house plating bath had two fountains placed with equal spacing from the substrate holder. The fountains spray plating solution perpendicular to the substrate. The substrate holder has opening from both sides and capable of supplying the current all through the circular edges. The current distribution through the circular edges makes it possible to avoid possible current concentration at certain location. MicroFAB DVF 100 was used as the plating chemistry supplied by Cookson electronics.

After electroplating process is complete, the plated samples were molded with pot molding compound from Buehler. Ecomet 3000 polisher was used to polish the sample to get the cross sectional view of the plated sample. Figure 5 shows the cross sectional view of the samples after DC and RPP. For DC plating, it was shown that there was continuous growth of plated copper in the vias from both sides. Because the top and bottom copper film are more exposed to the plating solution compared to the via, faster plating on the top and bottom copper film were observed. DC plating is capable of plating the entire via after 4.5 hours without any void formation. On the other hand, the reverse pulse plating did not produce desired result of via plating avoiding the over burden as explained in the theory. This is a maskless process. The over plating on the top and bottom copper film was observed, which can be eliminated either by polishing, or by chemical etching process.

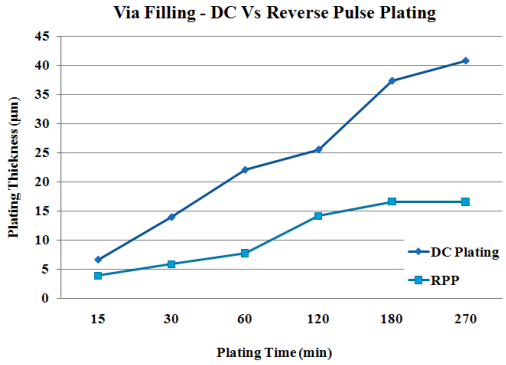

Figure 6: Comparison between the DC and reverse pulse plating in terms of plating time and thickness of the plated vias

Figure 6 shows the relation between the plating time and thickness of the electroplated copper inside the via. From the Figure 6, it can be seen that there is an almost linear correlation between the plating time and the thickness for DC plating. From the linear relationship it was found that DC electroplating gives about 7 micron of plating per hour. On the other hand, the RPP gives a copper electroplating thickness of 2.9 micron per hour.

Figure 7 shows the correlation between the DC and RPP plating on the top and bottom copper film of the ULTRALAM 3850. In DC plating, the top and bottom copper film is getting plated at the rate of 10 µm/hr as compared to the 7 µm/hr plating for the via. On the contrary, the RPP is gives a 4.5 µm/hr

plating for the top and bottom copper film compared to the 2.9 µm/hr plating for the vias.

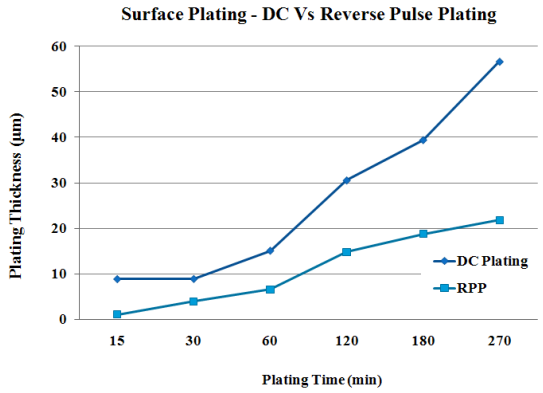

Figure 7: Comparison between the DC and reverse pulse plating in terms of plating time and thickness of the over plating top and bottom copper film of ULTRALAM 3850

VIII. Conclusion:

In this research, a chemical etching process was evaluated where the time dependent chemical etching shows effect on the surface roughness of the LCP vias created using micro mechanical punching process. It was observed that the chemical etchant (Promoter B) used in this three steps process of cleaning LCP and copper burr had the most effect on the roughness of the LCP vias. Longer etching time results a rougher LCP surface which would affect the surface adhesion of electroplated vias. In addition, the chemistry for the oxidation part (Promoter A) of the cleaning did not show any effect on roughness, unless the sample is treated for more than 1 minute. However, the longer oxidation time did not show any effect on the roughness for treatment times beyond 5 minutes. For samples treated with 5 minutes of oxidation and 5 minutes of etching, they did not show increased roughness for the time variant neutralization. DC and reverse pulse plating (RPP) were evaluated where it was demonstrated that DC plating gives the best metalized through vias. For through via filling an electroplating rate of 7 µm/hr was observed by DC plating as compared to 2.9 µm/hr in RPP. A faster plating of the top and bottom copper film was observed as compared to the through via. This is because of the more exposure of the top and bottom copper film compared to the interior of the vias. The conclusion can be made that DC plating is the most suitable candidate for electroplating through vias fabricated on LCP substrate using micro mechanical punching.

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